Inductive Cell Balancer IC with Balancing Current Up to 2A

DESCRIPTION

ETA3000 is an inductive cell balancer based on ETA's patent pending proprietary technology. Unlike conventional passive balancing technique, ETA3000 utilizes a control scheme with an inductor to shuffle currents between two cells until the cells are balanced. Due to the switching nature, the heat and power dissipation generated in conventional linear balance technique are greatly reduced. The balance time is also significantly reduced due to higher balancing current not being limited by package thermal dissipation. ETA3000 consumes only 2μA ultra-low current from batteries in standby mode, extending the battery shelf time. The final balanced voltages of both cells are also highly accurate which enhances the performance and lifetime for the batteries connected in series. ETA3000 can also be used in multiple cells stacking with even number of cells. ETA3000 includes protection features similar to precondition in battery charging, that is when one cell's voltage is grossly lower than the other, the balancing current is reduced to a safe level until the lower voltage cell is charged up.

ETA3000 is available in two type of package, SOT23-6, DFN2x2-8L

FEATURES

- Inductive, Switching control Scheme
- Up to 92% Charger transfer efficiency
- Accurate Balanced voltages down to 30mV
- Auto detect unbalance and auto balance
- Low sleeping supply current, 2μA
- Programmable balancing current up to 2A
- Precondition balancing current
- Status Indications
- Battery Over voltage protection
- Support small size inductor

APPLICATIONS

- Two Cells System
- E-Cigarette
- Battery Pack
- Portable Equipment and Instrumentation
- Battery Backup Systems

TYPICAL APPLICATION

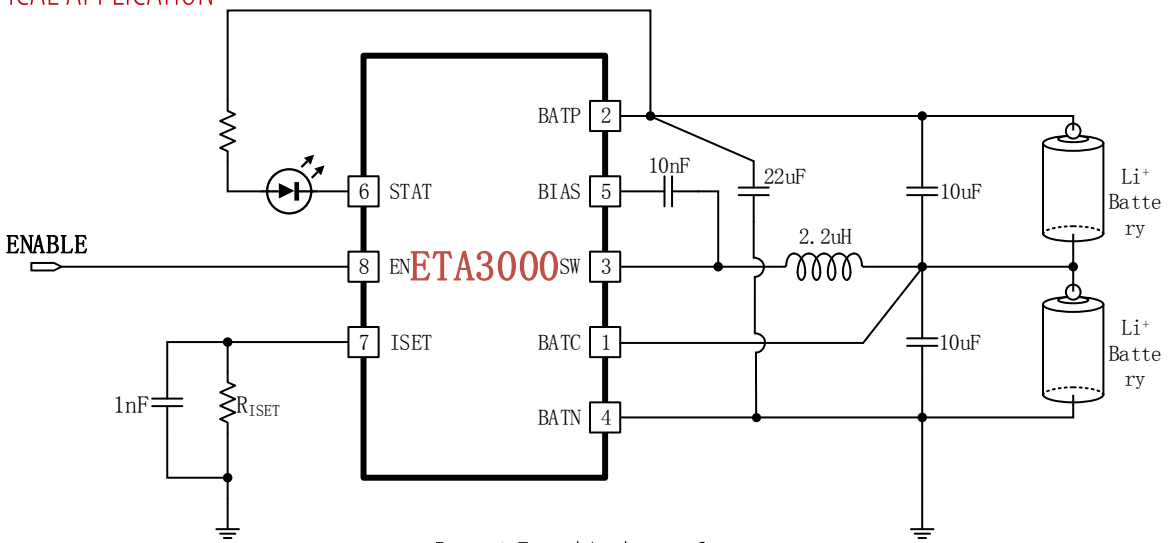
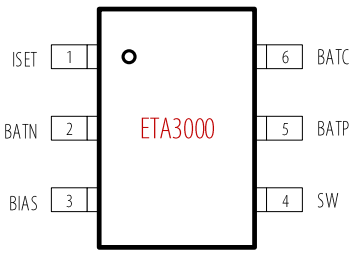


Figure 1: Typical Application Circuit

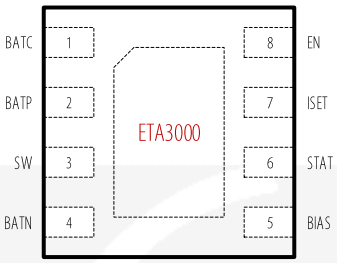
ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA3000S2G	SOT23-6L	GIYW	3000
ETA3000D2I	DFN2x2-8L	GSYW	3000

PIN CONFIGURATION



SOT23-6



DFN2x2-8

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

SW, STAT Voltage to BATN.....-0.3V to 12V
BIAS to SW Voltage.....-0.3V to 6V
BATC to BATN Voltage.....-0.3V to 6V
BATP to BATN Voltage.....-0.3V to 12V
ISET to BATN Voltage.....-0.3V to 6V
SW, BATC, BATP to BATN current.....Internally limited
Operating Temperature Range..... -40°C to 85°C
Storage Temperature Range.....-55°C to 150°C

Thermal Resistance	θ_{JC}	θ_{JA}	
SOT23-6L	90	180	°C/W
DFN2x2-8L	20	75	°C/W

Lead Temperature (Soldering,10sec).....260°C
ESD HBM (Human Body Mode).....2KV
ESD MM (Machine Mode).....200V

ELECTRICAL CHACRACTERISTICS

(T_A=25°C, LX = 1µH, C_{BOT}=C_{TOP}=1µF if not specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{SUPPLY}	Shutdown current	EN is low, V_{BATP}=8V		1		µA
	Quiescent current	EN is high, V_{BATP}=8V, V_{BATP}-V_{BATC}=V_{BATC}-V_{BATN}		2		µA
	Operating supply current	EN is high, V_{BATP}=8V, in balancing mode, No Switching		700		µA
V_{BATP}	VBATP operating voltage				10	V
V_{BATC}	VBATC operating voltage				5	V
UVLO	Under lock-out voltage threshold	V_{BATP} Rising		3.75		V
UVLO_HYS	UVLD hysteresis			200		mV
DETECTION						
T_{SLEEP}	Detection interval timer	Part sleeps during T_{SLEEP}		2		S
T_{ALLOW}	Unbalance detection acknowledgment timer	Unbalance status is accepted after T_{ALLOW} when enter CHECK state.		3.85		mS
T_{CHECK}	Maximum unbalance checking timer	IC get back to sleeping mode if don't detect unbalance after T_{CHECK}		7.68		mS
T_{DONE}	Finishing Timer	Maximum switching skip before enter sleep mode		62		mS

V_{KICK}	Unbalance detection threshold	Balancing only work if OVP>V_{BATP}>UVLO and V_{KICK} Detected between 2 cells	100	mV
V_{ERROR}	Balancing Accuracy	Error voltage between 2 cells after balancing finish	-30 30	mV
BALANCE CONTROLLER				
FREQ	Switching Frequency	PWM Clock	1	MHz
V_{ISET}	ISET pin voltage in Normal	$V_{(BATP-BATC)}$>TOP_PRECOND And $V_{(BATC-BATN)}$ >BOT_PRECOND	1	V
V_{ISET_PRE}	ISET Pin Voltage in Precondition	$V_{(BATP-BATC)}$<TOP_PRECOND Or $V_{(BATC-BATN)}$<BOT_PRECOND	0.1	V
$I_{AVERAGE}$	Average Inductor current Regulation	R_{ISET} = 50kΩ	1	A
$I_{PRECOND}$	Precondition current Regulation	R_{ISET} = 50kΩ	100	mA
BATTERY PROTECTION				
TOP_OVP	Top Cell over voltage protection threshold	$V_{(BATP-BATC)}$ Rising	5	V
TOP_OVP_HYST	TOP_OVP hysteresis	$V_{(BATP-BATC)}$Falling	350	mV
BOT_OVP	Bottom Cell over voltage protection threshold	$V_{(BATC-BATN)}$ Rising	5	V
BOT_OVP_HYST	BATC_OVP hysteresis	$V_{(BATC-BATN)}$ Falling	350	mV
TOP_PRECOND	Top battery precondition threshold	$V_{(BATP-BATC)}$ Rising	2.8	V
TOP_PREC_HYST	TOP_PRECOND hysteresis	$V_{(BATP-BATC)}$ Falling	150	mV
BOT_PRECOND	Bottom battery precondition threshold	$V_{(BATC-BATN)}$ Rising	2.8	V
BOT_PREC_HYST	BOT_PRECOND hysteresis	$V_{(BATC-BATN)}$ Falling	150	mV
BALANCE PROTECTION				
TOP_ILIM	Top cell drive current limit	DOWN direction: $V_{(BATP-BATC)}$> $V_{(BATC-BATN)}$	4.5	A
BOT_ILIM	Lower cell drive current limit	UP direction: $V_{(BATP-BATC)}$< $V_{(BATC-BATN)}$	4.5	A
LOGIC CHARATERISTICS				
VIL	EN low threshold		0.4	V
VIH	EN high threshold		1.2	V
VOL	STAT active low voltage	I_{STAT}=5mA	0.4	V
THERMAL SHUTDOWN				
TSD	Thermal shutdown		160	°C
TSD_HYST	TSD Hysteresis		30	°C

PIN DESCRIPTION

PIN NAME	DESCRIPTION		
	SOT23-6	DFN2x2-8L	
ISET	1	7	Balancing current setting pin. Connect a resistor from ISET to BATN to program the balancing current. Bypass the pin to BATN with 1nF capacitor.
BATN	2	4	Negative terminal Sense voltage input and common Ground pin.
BIAS	3	5	Bias pin. Connect a 10nF capacitor from BIAS to SW
SW	4	3	Switching node. Connected to inductor.
BATP	5	2	Sense voltage input for top cell. Connect 1μF capacitor between BATP and BATC.
BATC	6	1	Sense voltage input for bottom cell. Connect 1μF capacitor between BATC and BATN.
STAT	N/A	6	Open drain output to indicate balancing state. STAT active LOW during balancing
EN	N/A	8	IC Enable Input. EN is internally pulled to Logic High. Driver to a Logic Low to disable IC. EN pin is internally pulled up to Logic High.
EP	N/A	EP	Exposed Pad, connect it to GND

FUNCTIONAL BLOCK DIAGRAM

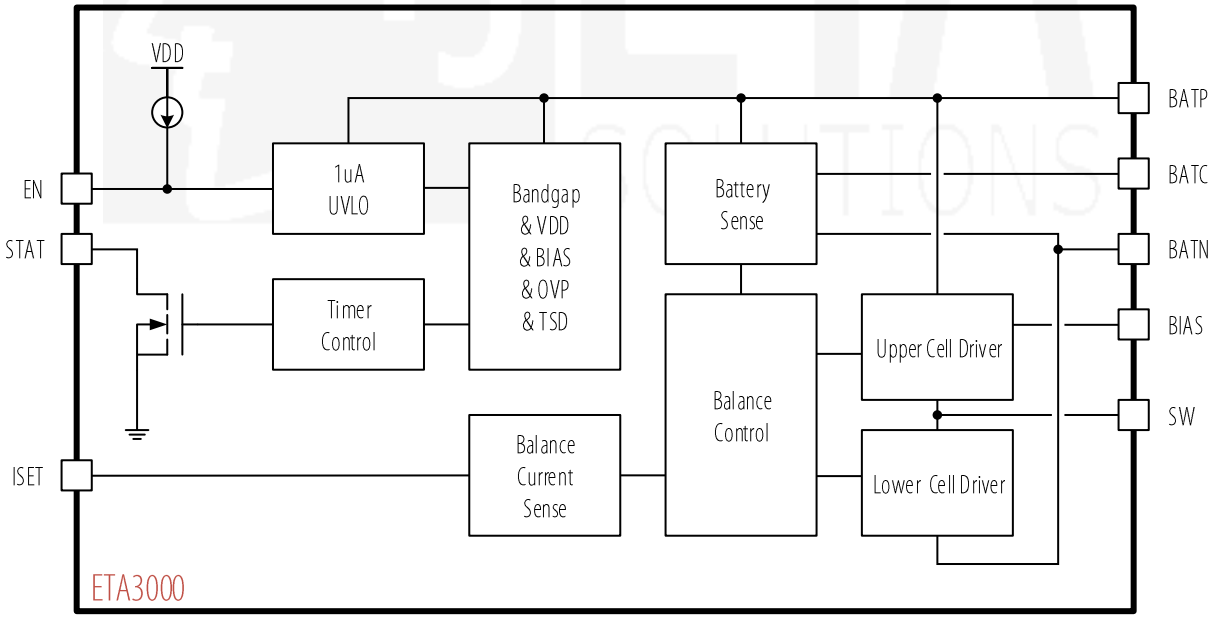
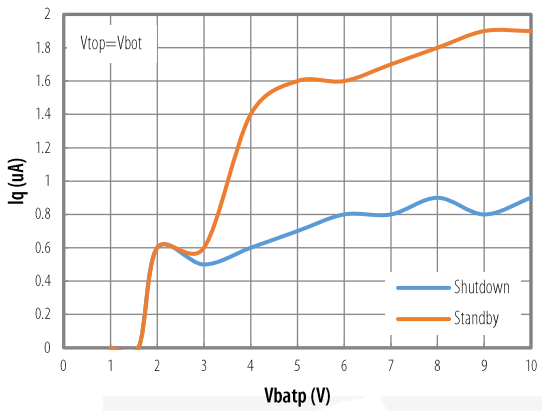


Figure 2: Functional Block Diagram

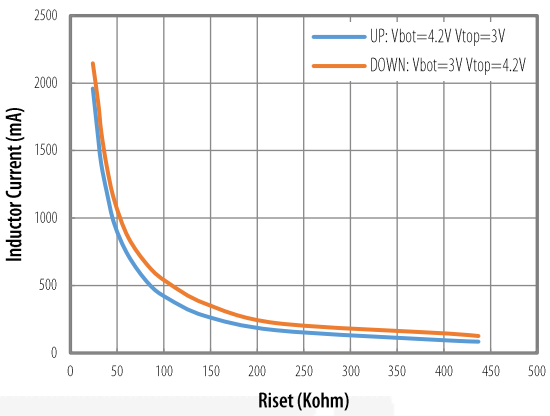
TYPICAL PERFORMANCE CHARACTERISTICS

(TA=25°C, unless otherwise specified)

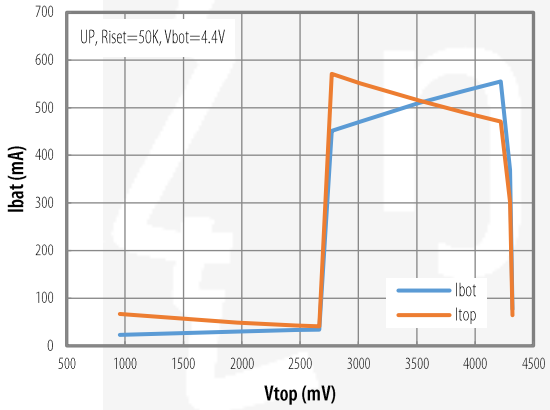
Iq Vs. Vbatp



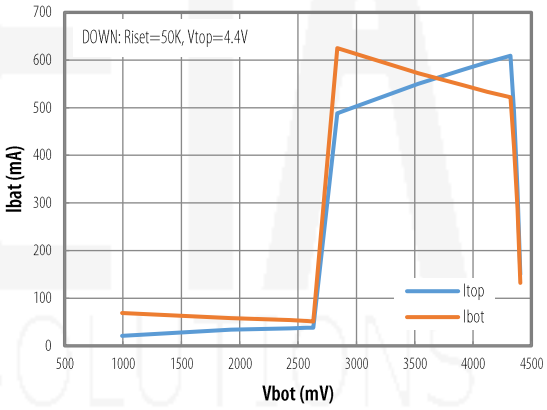
Inductor Current Vs. Riset



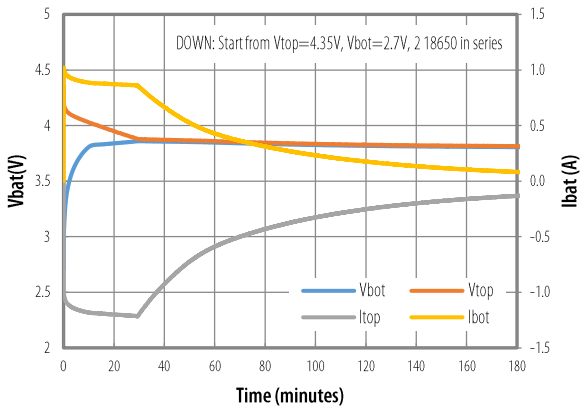
Ibat Vs. Vtop



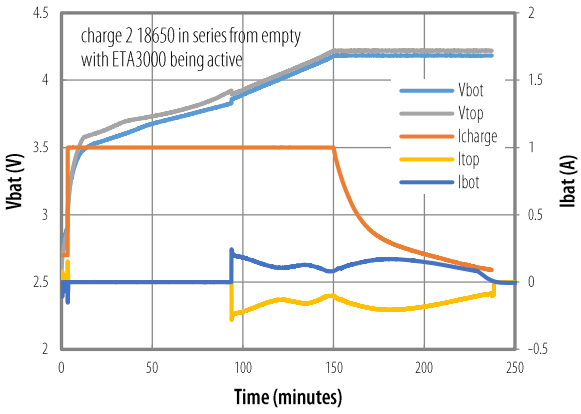
Ibat Vs. Vbot



Balancing Without Charger

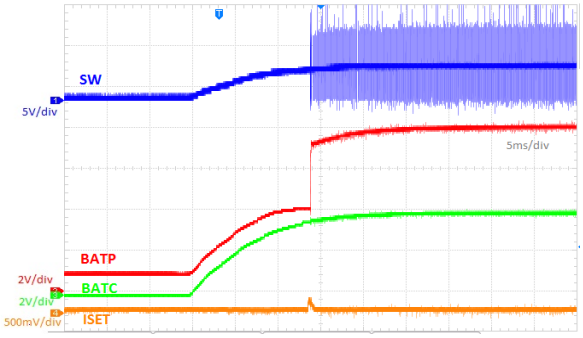


Balancing in Charging

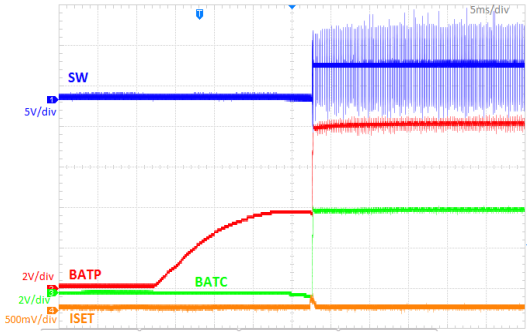


TYPICAL PERFORMANCE CHARACTERISTICS (cont')

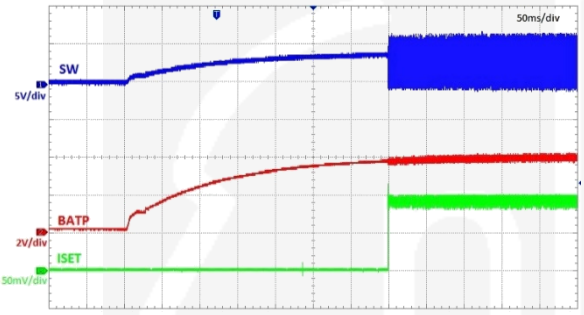
VBOT plug-in Start-Up , VTOP = Floating , RISET = 50k, VBOT = 4.3V



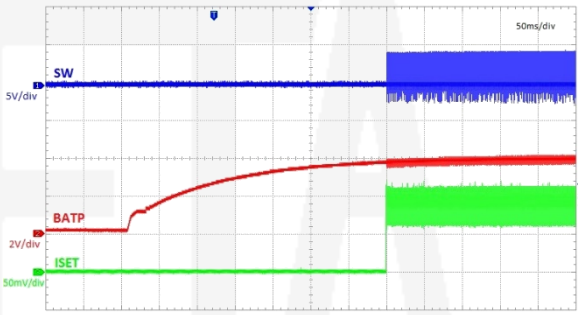
VTOP plug-in Start-Up , VTOP = Floating , RISET = 50k, VBOT = 4.3V



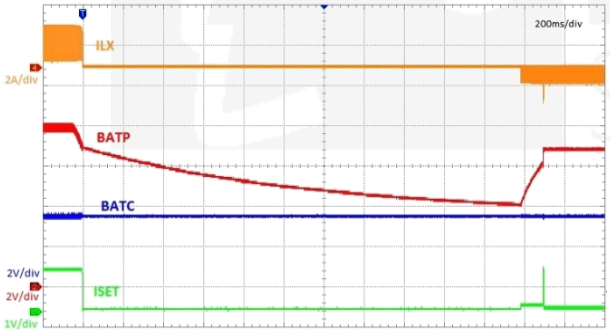
VBOT plug-in Start-Up , VTOP = Shorted , RISET = 50k, VBOT = 4.3V



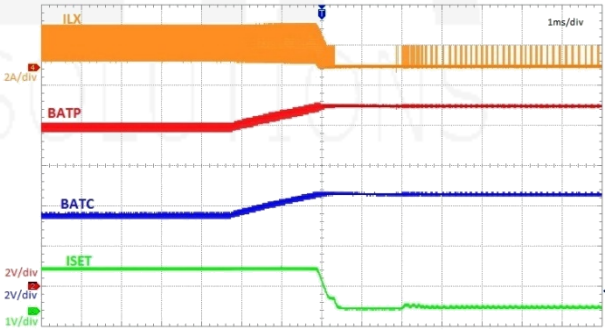
VTOP plug-in Start-Up , VBOT = Shorted , RISET = 50k, VTOP = 4.3V



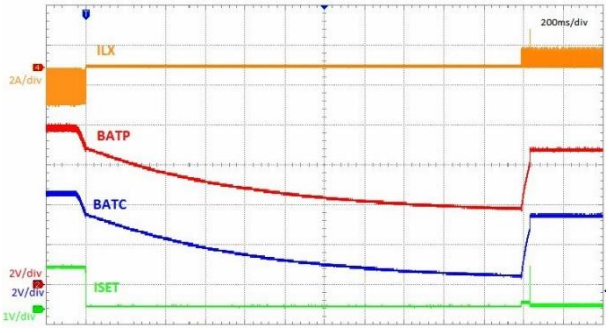
Un-plug Higher VBAT, DOWN Condition, RISET = 50k, VTOP = 4.3V, VBOT = 3.5V



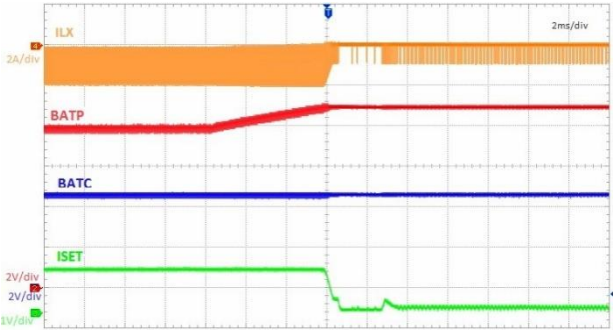
Un-plug Lower VBAT, DOWN Condition, RRISET = 50k, VTOP = 4.3V, VBOT = 3.5V



Un-plug Higher VBAT, UP Condition, RISET = 50k, VTOP = 4.3V, VBOT = 3.5V



Un-plug Lower VBAT, UP Condition, RISET = 50k, VTOP = 4.3V, VBOT = 3.5V



FEATURE DESCRIPTION

The ETA3000 is a battery cell balancer with lossless inductive architecture based on ETA's proprietary technology. The technology is developed by ETA Solutions and any copy without ETA's agreement will be forbidden.

During operation, ETA3000 detects the difference between 2 cells then start balancing if the difference exceeds V_{KICK}. Once detected V_{KICK}, ETA3000 will discharge the higher voltage cell, store that discharging energy in the inductor then charge that energy to the lower voltage cell. ETA3000 keeps balancing until there is no difference between 2 cells.

ETA3000 technology allows balancing in either charge or discharge phases of the battery with minimized loss.

Without unbalanced condition, ETA3000 operates in sleep mode with low supply current. This is an advantage to extend battery pack life time.

STATE MACHINE

The ETA3000 provides a completed state machine that controls whole operation intelligently. With this state machine, ETA3000 is equipped with self-protection from any accident during balancing. It also keeps the part stay asleep as much as possible until unbalance detected.

ETA3000 always starts from CHECK state when battery is plugged in.

Any fault always forces ETA3000 back to SLEEP State where ETA3000 burns only 2μA (typically) from BATP.

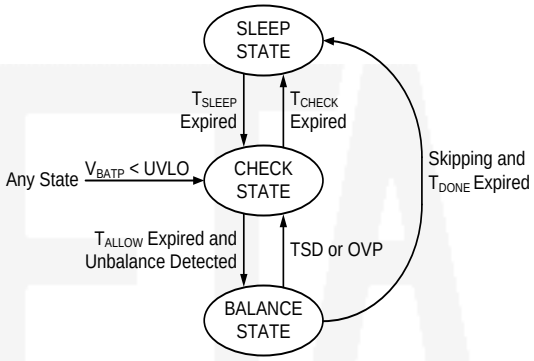


Figure 3: State Machine Diagram

The ETA3000 timing diagram for state machine is shown in following figure.

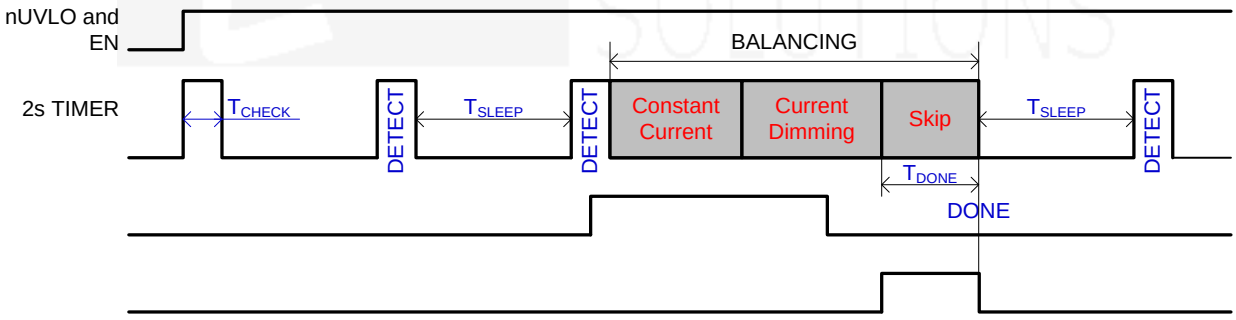


Figure 4: Timing Profile

UNBALANCE DETECTION

When state is in CHECK State, ETA3000 detects V_{KICK} difference between 2 cells to enter BALANCE State. If the top cell voltage is higher, balancing will be "DOWN", meaning discharge the top cell to charge to bottom cell. And if the bottom cell voltage is higher, balancing will be "UP", meaning discharge the bottom cell to charge to top cell.

BALANCING PROFILE

ETA3000 balancing always starts with "Constant Current Regulation" phase since it is always with high voltage difference. Constant current is set by R_{ISET}.

When the detected difference at IC pin is almost zero, but due to battery equivalent series resistance, real difference is not zero, then current is not immediately zero but reduced slowly depend on battery capacitance. This condition is called "Current Dimming" phase.

When two cell voltages are equal, balancing current becomes almost zero, when this persist for a time period of T_{DONE}, the balancing finishes one cycle, and ETA3000 goes back to SLEEP State.

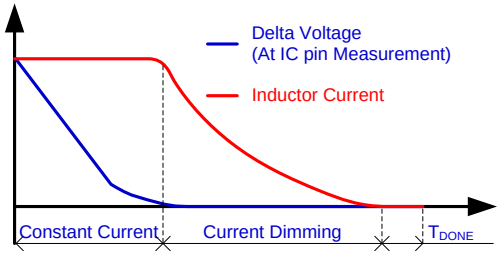


Figure 5: Balancing Profile

PROTECTION

ETA3000 provides full protection to batteries that extend the life time of the batteries:

- Short and Low Voltage Protection: When either of the cell voltage below $V_{PRECOND}$, maximum balancing current will be re-defined to 10% of the level set by ISET pin resistor.
- Open and Over Voltage Protection: When either of the cell voltage is greater than V_{OVP}, ETA3000 will stop balancing, and go back to SLEEPING. Part will wake up after T_{SLEEP}.
- Thermal Shutdown: When part gets hotter than 160°C, ETA3000 will stop balancing, and go back to SLEEPING. Part will wake up after T_{SLEEP}.
- Current Limit Protection: Maximum of the peak of inductor current is allowed to 5.5A.

APPLICATION INFORMATION

BALANCING CURRENT SETTING

Balancing current is defined as the half of average inductance current. Average inductance current is regulated following ISET resistor configuration.

AVERAGE INDUCTION CURRENT	RECOMMENDED COMPONENT			
	ISET RESSITOR	ISET CAPACITOR	INDUCTOR	BATTERY CAPACITOR
100mA	500kΩ	500pF – 10nF	0.33-0.6μH	0.47μF – 3.3μF
250mA	200kΩ	500pF – 10nF	0.47-1μH	0.47μF – 3.3μF
400mA	125kΩ	500pF – 10nF	0.47-1μH	0.47μF – 3.3μF
500mA	100kΩ	500pF – 10nF	0.47-1μH	0.47μF – 3.3μF
625mA	80kΩ	500pF – 10nF	0.68-1μH	0.47μF – 3.3μF
800mA	62.5kΩ	500pF – 10nF	0.68-1μH	0.47μF – 3.3μF
1000mA	50kΩ	500pF – 10nF	0.68-1μH	0.47μF – 3.3μF
1250mA	40kΩ	500pF – 10nF	0.68-1μH	0.47μF – 3.3μF
1515mA	33kΩ	500pF – 10nF	0.68-1μH	0.47μF – 3.3μF
1667mA	30kΩ	500pF – 10nF	1-2μH	0.47μF – 3.3μF
2000mA	25kΩ	500pF – 10nF	1-2μH	0.47μF – 3.3μF

Balancing current is defined as average of inductor current.

RESTRICTED CONDITIONS

ETA3000 does not allow following restricted conditions:

- Reverse battery connection
- Short SW to any of BATN, BATP, BATC
- Not exceed the absolute maximum rating of each IC pin

MULTI-COUPLE CELL BALANCING SOLUTION

It is also possible to use several ETA3000 ICs in application to balance multi-cell series battery such as balancing for laptop battery pack.

Figure 7 shows a typical solution for 4-cell-battery in battery pack.

Each ETA3000 manages balancing of 2 neighbor cells. And without enable control, each ETA3000 operates independently. Positive terminal of the pack is connected to BATP of Cell 4 and Negative terminal of the pack is connected to BATN of Cell 1.

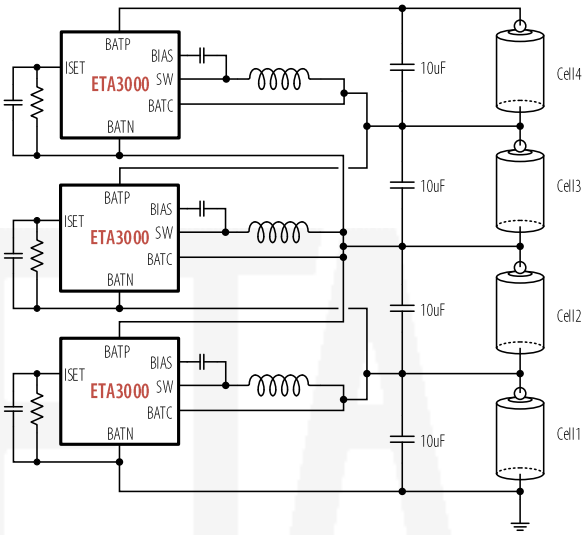


Figure 6: Multi-Cell Balancing Solution

PCB DESIGN GUIDELINE

In an UP case that bottom cell voltage is greater than top cell voltage, bottom cell becomes input and top cell becomes output of the switching regulation. In a DOWN case that top cell voltage is greater than bottom cell voltage, top cell becomes input and bottom cell becomes output. These mean parallel battery capacitors are always output capacitor or input capacitor for regulator. So please require to locate as close as possible to IC pins to minimize series resistance.

Please try to get the order of battery pins are BATP – BATC – BATN to make an easy battery connection.

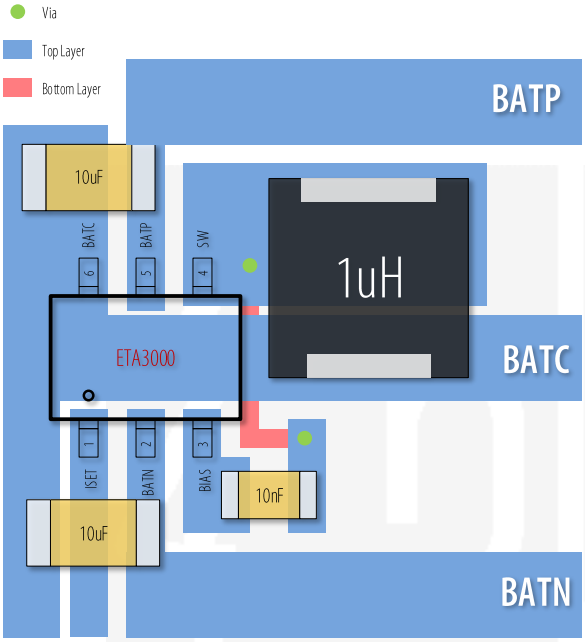


Figure 7: PCB Recommendation, SOT23-6

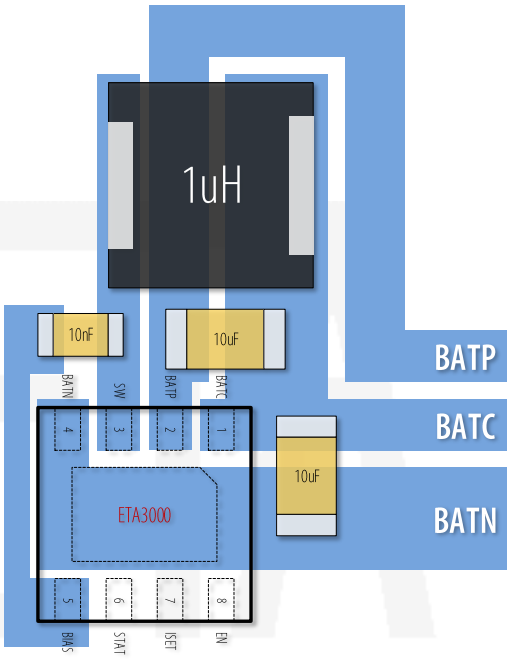
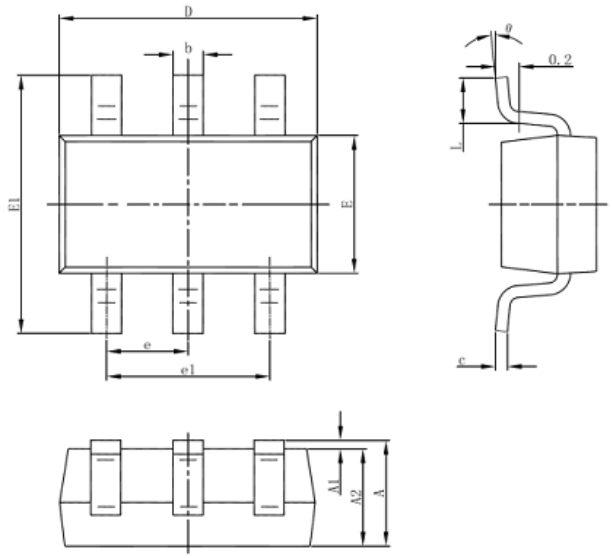


Figure 8: PCB Recommendation, DFN2X2-8L

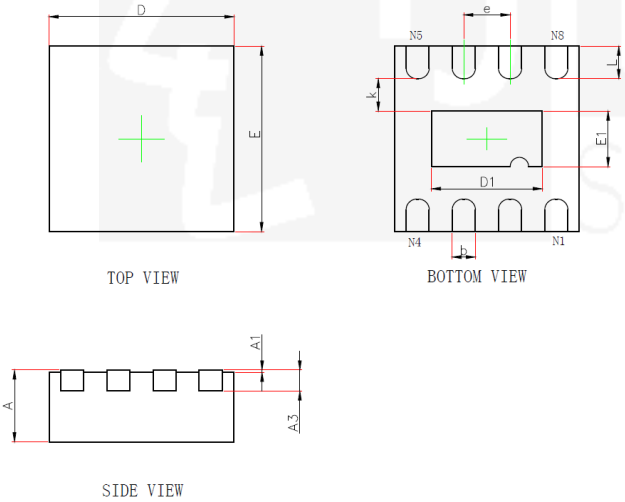
PACKAGE OUTLINE

Package: SOT23-6L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.00	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package: DFN2x2-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	1.100	1.300	0.043	0.051
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.200	0.300	0.008	0.012
e	0.500 TYP		0.020 TYP	
L	0.274	0.426	0.011	0.017