Infrared Filter Switch Driver

Features

- 1.8V to 5.5V operation voltage range
- 1.8V input pulse driving
- Ultra low saturation voltage
  - 0.36V@200mA, VDD=5V
  - 0.57V@300mA, VDD=5V
- Ultra-low standby current
- Build-in MOSFET shoot through protection circuit to prevent from device damage by fast output transient
- SOT23-6L package
- A/B versions selectable
  - Ver. A in dual-wire control
  - Ver. B in one-shot mode control

Applications

- IR surveillance camera filter driver
- Body worn video
- Wearable IR camera
- Smart locker

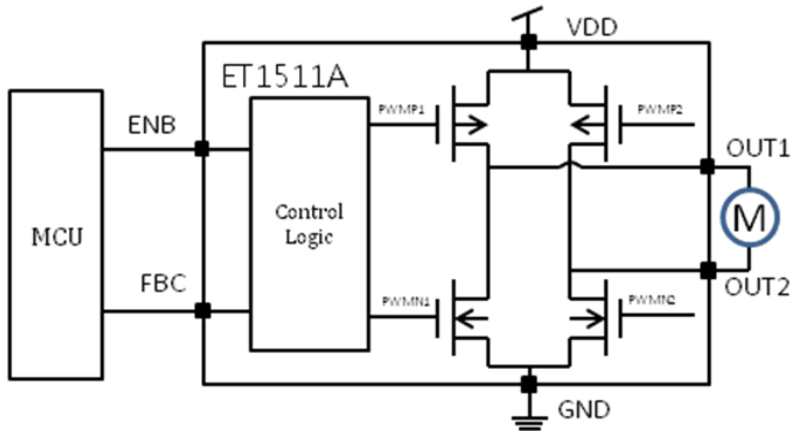
Description

ET1511A/B is an infrared filter switch driver IC which designed for filter control driving in IR cut module in camera. ET1511A/B could functions as a one-channel, low output headroom voltage, bi-directional H-bridge driver by appropriate input controls. Build-in protection diode circuit can minimize the disturbance caused by the feedback current when IR cut is shutdown or ESD transient pulses appeared.

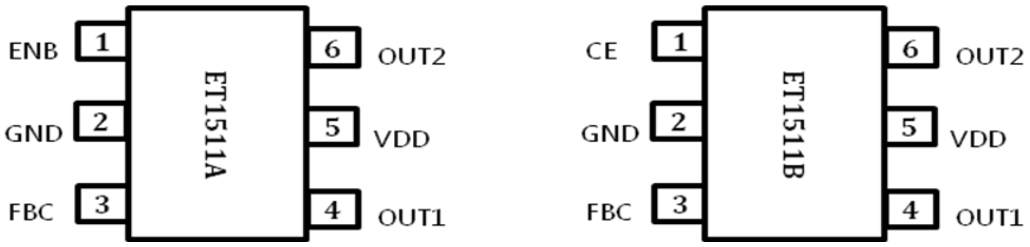
The output driver impedance of ET1511A/B is 2Ω in typical. The current driven through the actuator is determined by the impedance of the IR cut. In case of 5V power supply, the 300mA driving current through actuator is around 300mA with 0.48V output voltage headroom.

There are 2 versions (Ver. A and Ver. B) of ET1511, which offers to support single-wire input control, dual-wire input control, and one-shot control. In one-shot control mode, the on time could be configured by external capacitor.

Simplified Application Circuit



Pin Assignments



Pin Description

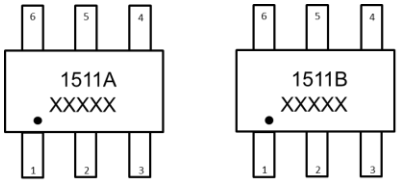
Pin Name	Pin No.	I/O	DESCRIPTION
ENB	1 (ET1511A)	I	ENB input. - Single-wire control mode, ENB is active low. - Dual-wire control mode, ENB and FBC are used for 2-wire control.
CE	1 (ET1511B)	I	Connect to external capacitor. (One-shot mode control only.)
GND	2	P	System ground.
FBC	3	I	Forward/Backward control
OUT1	4	O	Half-bridge driver output 1
VDD	5	P	Power supply
OUT2	6	O	Half-bridge driver output 2

Ordering Information

Product ID	Package	Packing / MPQ	Comments
ET1511A	SOT23-6L	3000 Units / Reel 3000 Units / Small Box	Green
ET1511B	SOT23-6L	3000 Units / Reel 3000 Units / Small Box	Green

Marking Information

Marking Information
Line 1：Product Name
Line 2：Tracking Number



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage	VDD	-0.3	7.0	V
V_{IN}	Input pin voltage	ENB, FBC, CE	-0.3	7.0	V
IOUT	Output current	Continuous operation	–	500	mA
		50% duty pulse output	–	600	
T_A	Operating ambient temperature range		-40	85	°C
T_{stg}	Storage temperature range		-55	150	°C
ESD	Human Body Model		–	±2K	V
	Charged Device Model		–	±1K	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratingsonly, which do not imply functional operation of the device at these or any other conditions beyond those indicated under RecommendedOperating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage	VDD	1.8	5.5	V
V_{IN}	Input pin voltage	ENB, FBC, CE	0	5.5	V
IOUT	Output current	Continuous operation	–	400	mA

Thermal Information

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JC}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
SOT23-6L	ET1511A/B	210.3	105	6.1	None

Note 1.1: θ_{JA} is simulatedon a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

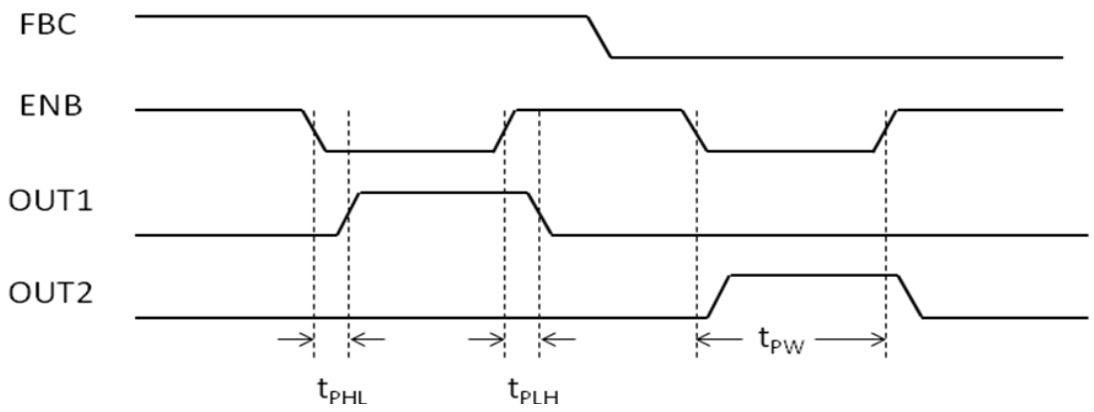
Note 1.2: θ_{JC} represents the thermal resistance for the heat flow between the chip junction and the package`stop surface. It`s extracted from the simulation data with obtaining a cold plate on the package top.

Note 1.3: Ψ_{JT}represents the thermal parameterfor the heat flow between the chip junction and the package`s top surface center. It`s extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-5.

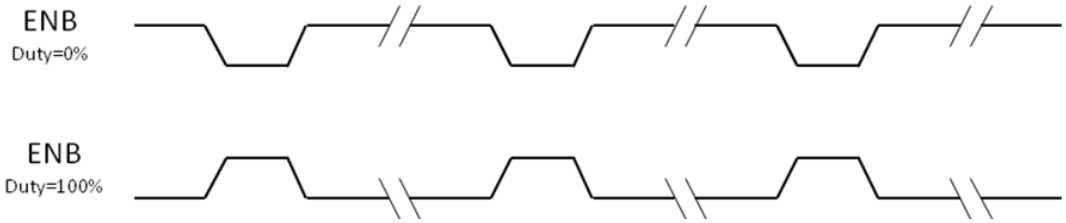
Electrical Characteristics

- VDD=5V, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VDD	Supply voltage	Normal operation	1.8	5.0	5.5	V
I_{VDD}	Quiescent supply	ET1511A (No load)	–	–	12	uA
		ET1511B (No load)	–	–	45	uA
I_{TRAN}	Transient current	Output transit state	0.5	0.8	1	mA
Input control ENB/FBC						
V_{IH}	Input logic "H"	–	1.6	–	5.5	V
V_{IL}	Input logic "L"	–	0	–	0.2VDD	V
R_{PL}	Input pull-low resistor	ENB & FBC pins	120	160	200	kΩ
Driver output OUT1/OUT2						
V_{OUT}	Output voltage headroom (upper + lower)	Voltage	3V	3.3V	5V	
		I_{OUT}=200mA	0.48	0.47	0.36	V
		I_{OUT}=300mA	0.83	0.76	0.57	V
		I_{OUT}=400mA	1.34	1.15	0.81	V
T_R	Rising transit time	From 0.1VDD to 0.9VDD	–	2.5	5	ns
T_F	Falling transit time	From 0.9VDD to 0.1VDD	–	2	4	ns
Propagation delay time						
T_{PLH}	ENB (L to H) → OUT1/2	VDD=5V, R_{LOAD}=18Ω	–	13	16	ns
T_{PHL}	ENB (H to L) → OUT1/2		–	24	40	ns
T_{PW}	Pulse width of ENB		100	–	–	ns
F_{MAX}	Max. frequency of ENB		–	–	5	MHz



(a) Propagation delay time between ENB and OUT1/OUT2



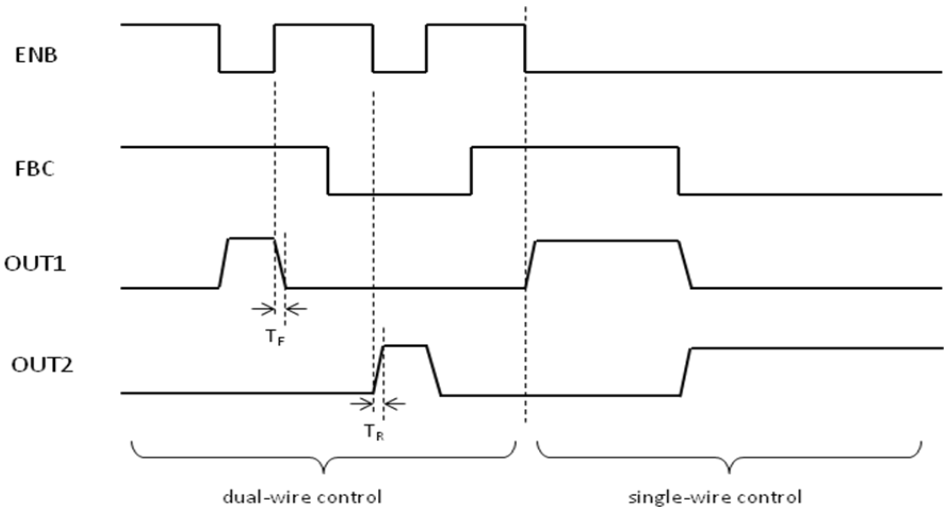
(b) PWM waveform for ENB

Figure1. Waveform timing definition

Truth Table and Diagram Controls

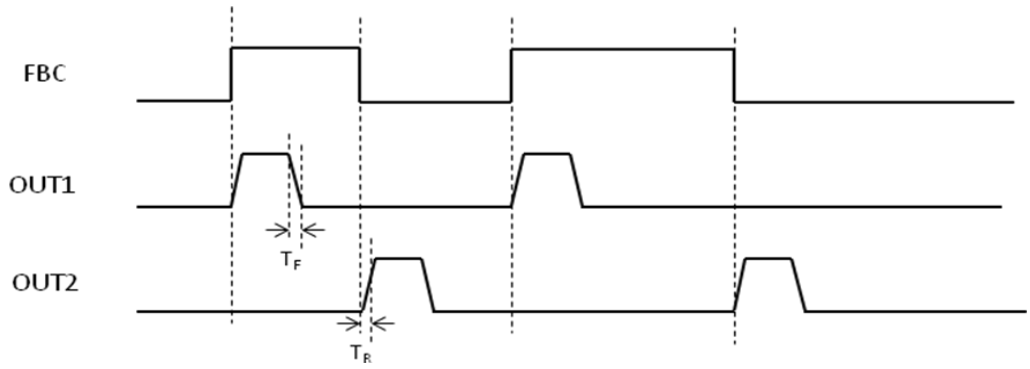
(1) ET1511A

Input		Output	
ENB	FBC	OUT1	OUT2
H	—	L	L
L	H	H	L
L	L	L	H



(2) ET1511B

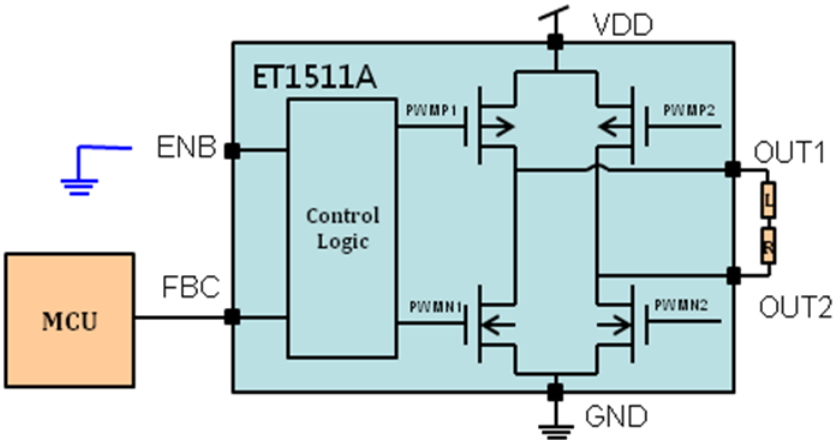
Input	Output	
FBC	OUT1	OUT2
⎍	⎍	L
⎎	L	⎍



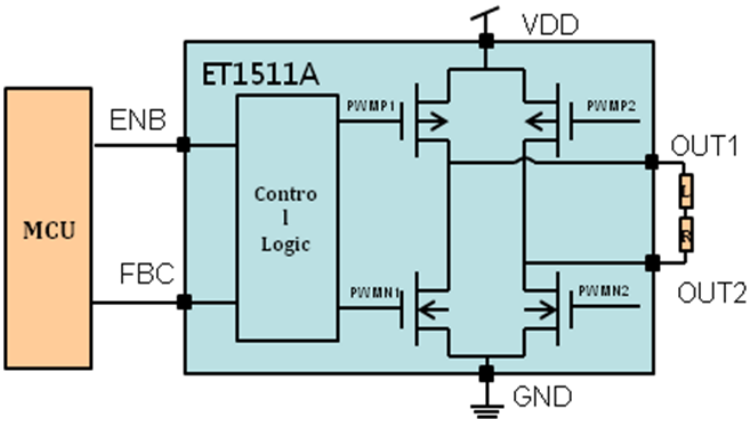
The one-shot period is determined by external capacitor which connected to CE pin of ET1511B.

$$T_{OS} = 1.6 \times 10^6 \times C_{CE} \text{ (sec.)}$$

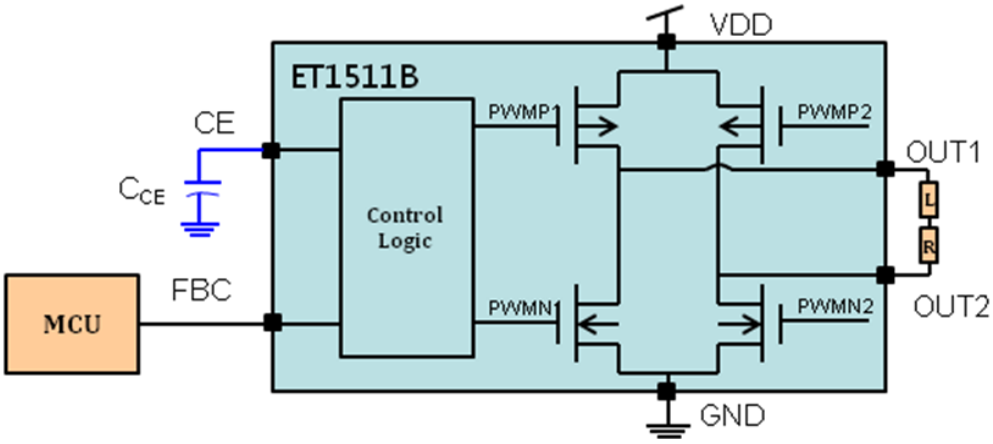
Application Circuits



(a) Single-wire control by FBC



(b) Dual-wire control by ENB and FBC



(c) One-shot control by FBC and external capacitor C_{CE} connect to CE pin

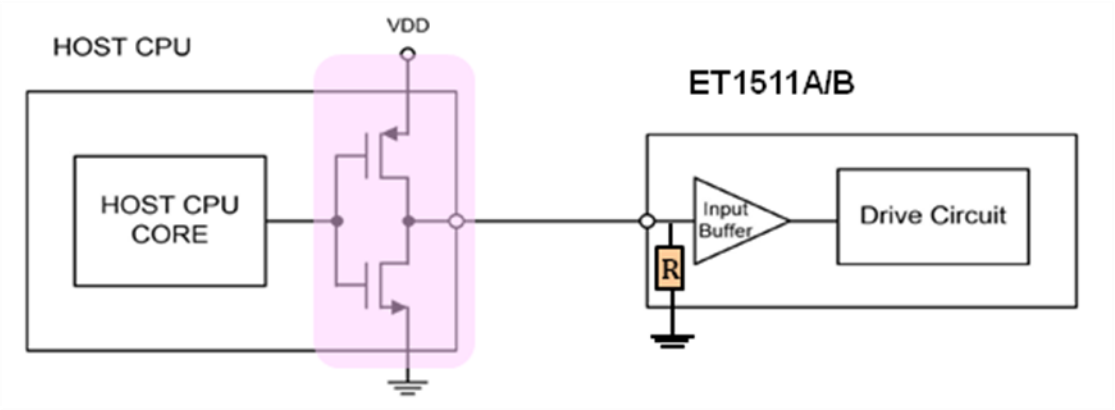
Figure3. Typical application circuit of ET1511A/B

MCU control

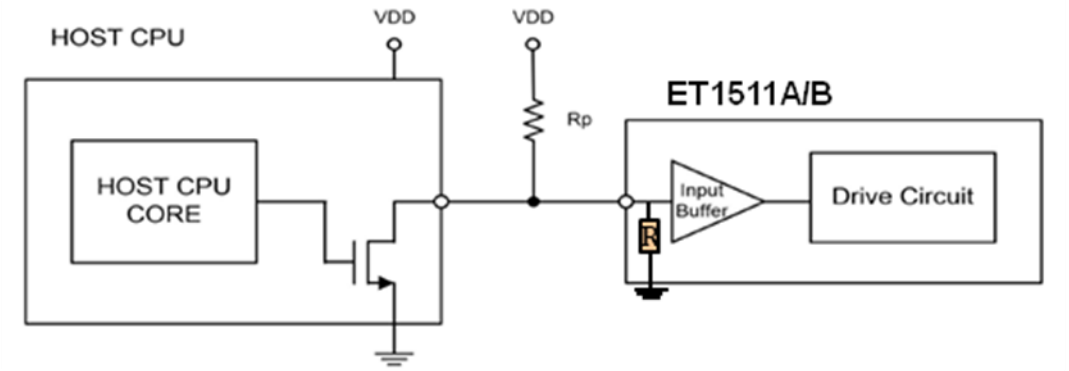
The ENB and FBC pins of ET1511A/B are internal pull-low to ground, which is in safety if input port are floating from unknown output states. The input voltage of input pins must higher than V_{IH} or small than V_{IL} to ensure the logic states of the input buffers are stable.

In most cases, ET1511A/B is controlled by GPIO ports of host microcontroller. In general, MCU has 2 types of GPIO ports, open-drain output and buffer output.

The output level of buffer output is VDD in high level and VSS in low level, the GPIO port could connect to ENB and FBC pins directly.

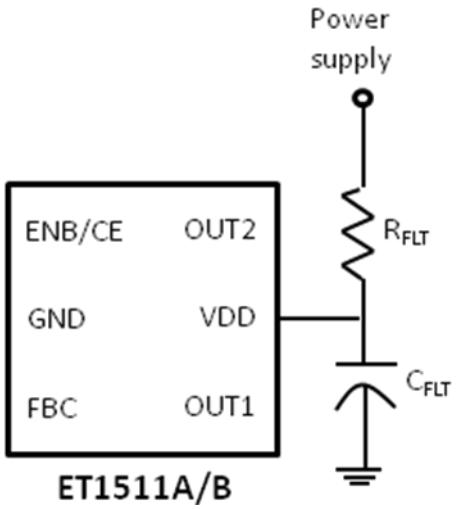


The open-drain output of GPIO port should external pull-up resistor, which does not have pull up driving capability. Because of 150KΩ internal pull-low resistor, the external pull up resistor could be setup to 100KΩ maximum. The smaller external pullup resistor will result in faster rise time of output stage but more current consumption when open-drain driven device turns on.



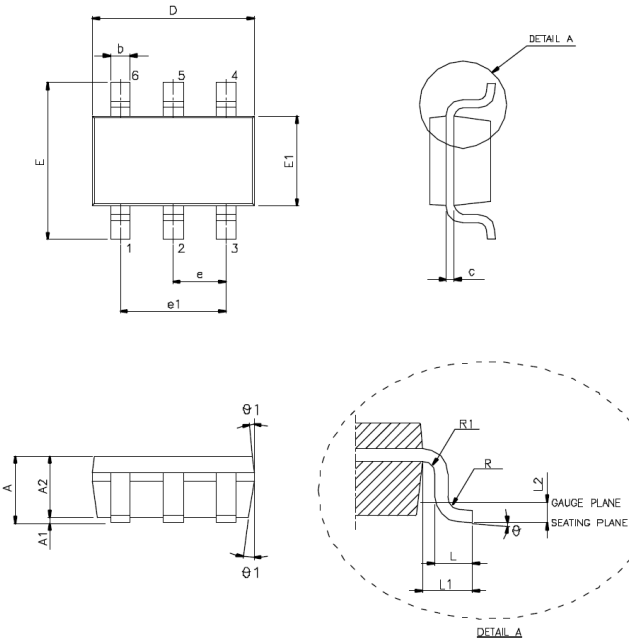
Layout Guidelines

The output coil motor will actuate back EMF voltage, an unexpected high and low voltage level may force on OUT1 and OUT2 pins during output transient. It is recommended to place a R_{FLT}-C_{FLT} filter on VDD pin to protect ET1511A/B from higher extreme transient voltage stress.The resistor R_{FLT} and capacitor C_{FLT} should place as close to VDD pin as possible.



Package Dimensions

SOT23-6L



SYMBOL	MIN.	NOM.	MAX.
A	–	–	1.45
A1	–	–	0.15
A2	0.90	1.15	1.30
b	0.30	–	0.50
c	0.08	–	0.22
D	2.90 BSC.		
E	2.80 BSC.		
E1	1.60 BSC.		
e	0.95 BSC.		
e1	1.90 BSC.		
L	0.30	0.45	0.60
L1	0.60		
L2	0.25		
R	0.10	–	–
R1	0.10	–	0.25
θ	0	4^o	8^o
θ 1	5^o	10^o	15^o

Revision History

Revision	Date	Description
1.0	2022.10.05	Original.

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