

ESD Protection Diodes

Micro-packaged Diodes for ESD Protection

ESDM1053

The ESDM1053 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in smartphone, smart-watch, or many other portable / wearable applications where board space comes at a premium.

Features

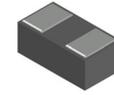
- Low Capacitance (5.5 pF Typ, I/O to GND)
- Small Body Outline Dimensions: – 01005 Size: 0.435 x 0.230 mm
- Protection for the Following IEC Standards:
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T _J	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T _L	260	°C
ESDM1053: IEC 61000-4-2 Contact IEC 61000-4-2 Air	ESD	±18 ±18	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.



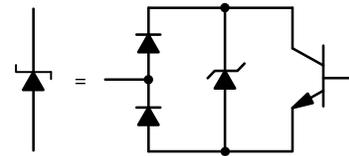
DSN2
CASE 152BB

MARKING DIAGRAM



• = Specific Device Code

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ESDM1053

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V _{RWM}	I/O Pin to GND			5.5	V
Breakdown Voltage	V _{BR}	I _T = 1 mA, I/O Pin to GND	5.8	6.7	9.0	V
Reverse Leakage Current	I _R	V _{RWM} = 5.5 V, I/O Pin to GND			0.05	μA
Clamping Voltage TLP (Note 1)	V _C	I _{PP} = 8 A I _{PP} = 16 A I _{PP} = 30 A		6.7 7.5 9.0		V
Dynamic Resistance	R _{DYN}	I/O Pin to GND, 100 ns TLP		0.10		Ω
Reverse Peak Pulse Current	I _{PP}	IEC61000-4-5 (8x20 μs)	5.0	6.0		A
Clamping Voltage (8x20 μs)	V _C	I _{PP} = 1.0 A I _{PP} = 5.0 A		6.0 7.0	8.5	V
Junction Capacitance	C _J	V _R = 0 V, f = 1 MHz		5.5	7.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.

TLP conditions: Z₀ = 50 Ω, t_p = 100 ns, t_r = 1 ns, averaging window; t₁ = 70 ns to t₂ = 90 ns.

ORDERING INFORMATION

Device	Package	Shipping [†]
ESDM1053FCT5G	DSN2 (Pb-Free)	10,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

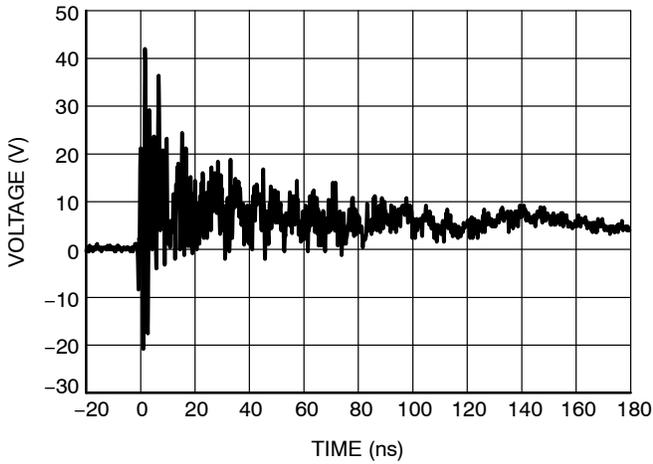


Figure 1. ESD Clamping Voltage Positive 8 kV Contact per IEC61000-4-2

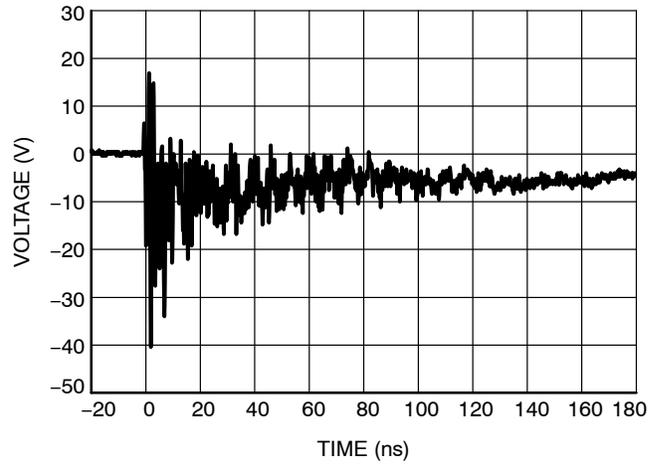


Figure 2. ESD Clamping Voltage Negative 8 kV Contact per IEC61000-4-2

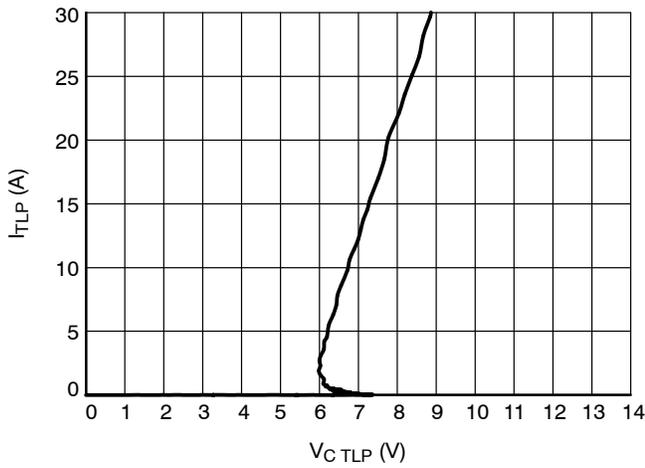


Figure 3. Positive 100 ns TLP I-V Curve

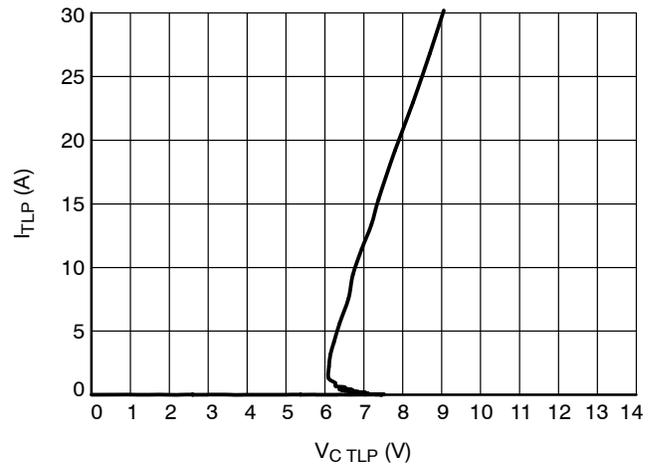


Figure 4. Negative 100 ns TLP I-V Curve

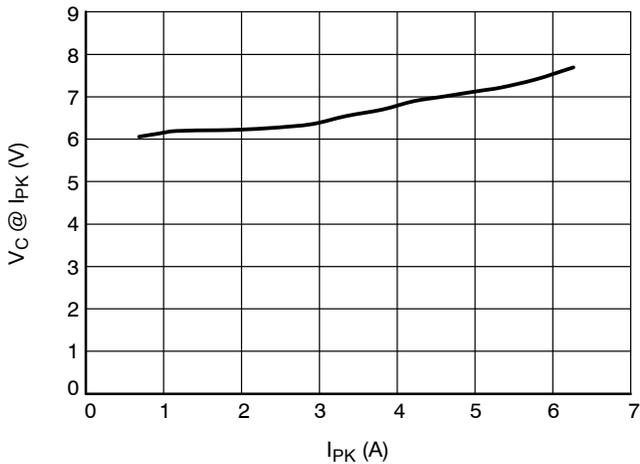


Figure 5. Clamping Voltage vs. Peak Pulse Current - Pin 1 to Pin 2 (tp = 8/20 μs)

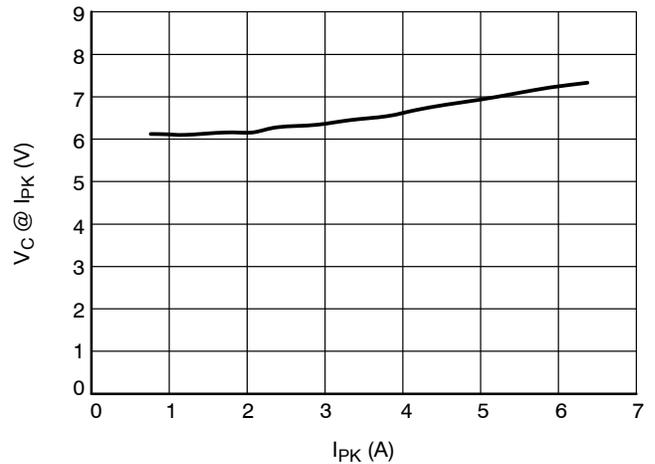


Figure 6. Clamping Voltage vs. Peak Pulse Current - Pin 2 to Pin 1 (tp = 8/20 μs)

TYPICAL CHARACTERISTICS

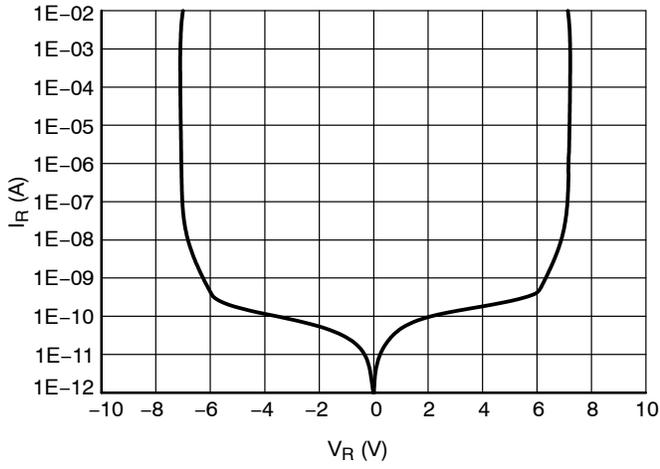


Figure 7. Breakdown Voltage

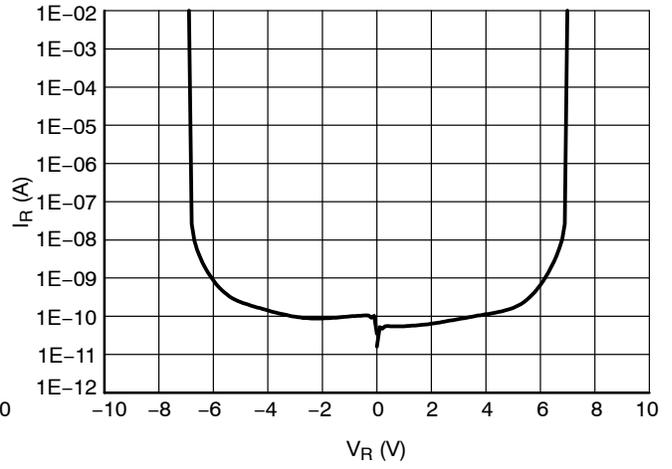


Figure 8. Reverse Leakage Current

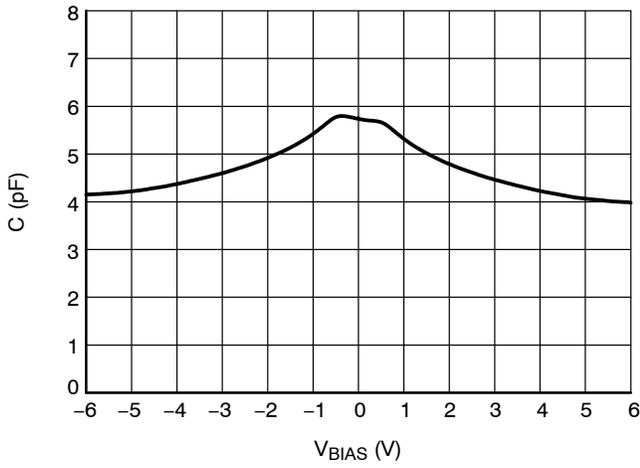


Figure 9. Line Capacitance, $f = 1$ MHz

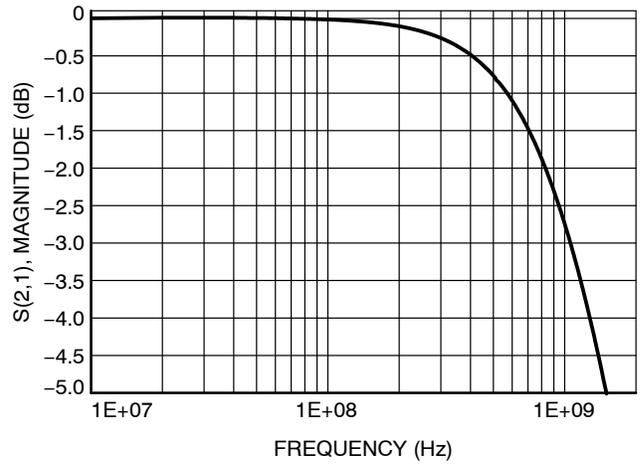


Figure 10. Insertion Loss

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

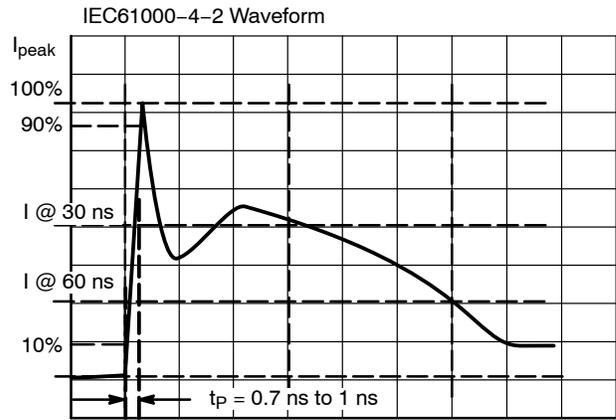


Figure 11. IEC61000-4-2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 12. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 13 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

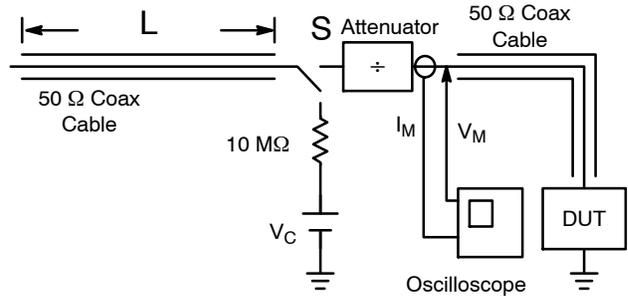


Figure 12. Simplified Schematic of a Typical TLP System

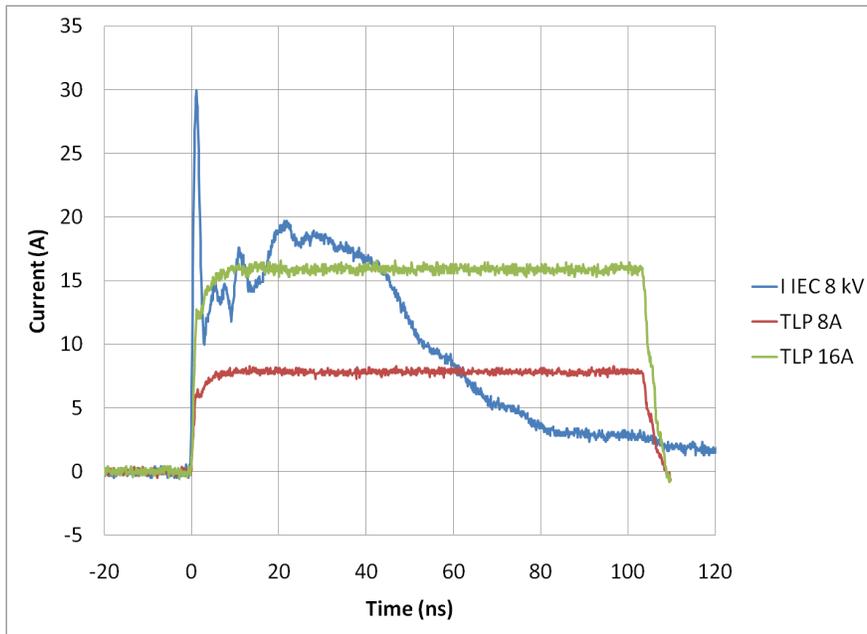
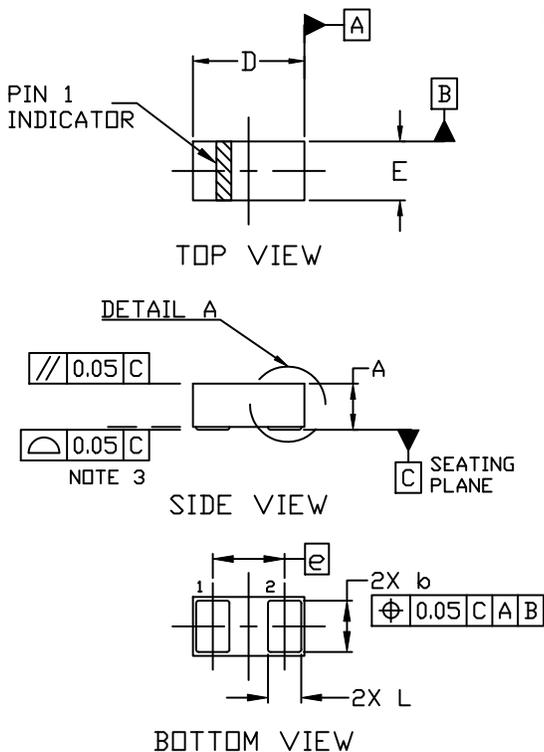


Figure 13. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

ESDM1053

PACKAGE DIMENSIONS – ESDM1053 (01005)

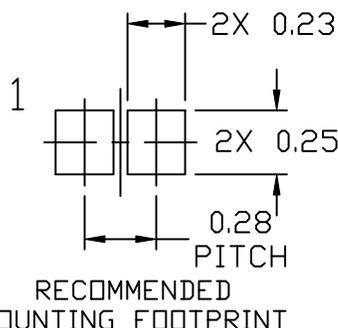
DSN2, 0.435x0.23, 0.28P
CASE 152BB
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO ALL PADS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.165	0.180	0.195
A1	0.008	0.011	0.014
A2	0.157	0.169	0.181
b	0.192	0.200	0.208
D	0.415	0.435	0.455
E	0.210	0.230	0.250
e	0.28 BSC		
L	0.122	0.130	0.138



* For additional information on our Pb-Free strategy and soldering details, please download the [DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D](#).

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