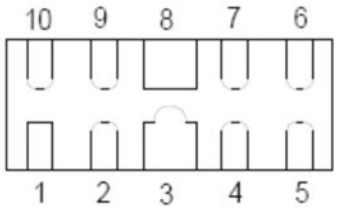
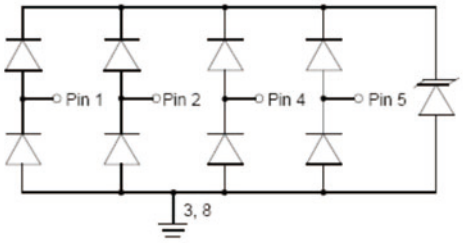
Ultra Low Capacitance TVS Arrays

ESDF5V4

The ESDF5V4 are ultra low capacitanceTVS arrays designed to protect high speed data interfaces.This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines form overvoltage caused by ESD(electrostatic discharge),CDE(Cable Discharge Events),and EFT(electrical fast transients).

DFN-10





Pin	Identification
1、2、4、5	Input Lines
6、7、9、10	Output Lines (No Internal Connection)
3、8	Ground

FEATURES

- Package design optimized for high speed lines
- Flow-Through design
- Protects four I/O lines
- Low capacitance: 0.3pF typical (I/O to I/O)
- Low clamping voltage
- Low operating voltage: 5V
- Solid-state silicon-avalanche technology

APPLICATION

- High Definition Multi-Media Interface (HDMI).
- Digital Visual Interface (DVI)
- DisplayPortTM Interface
- MDDI Ports
- LVDS
- Serial ATA
- PCI Express

Complies with the following standards

IEC61000-4-2

Level 4 15 kV (air discharge)

8 kV(contact discharge)

MIL STD 883E - Method 3015-7 Class 3

25 kV HBM (Human Body Model)

Maximum ratings (limiting value)

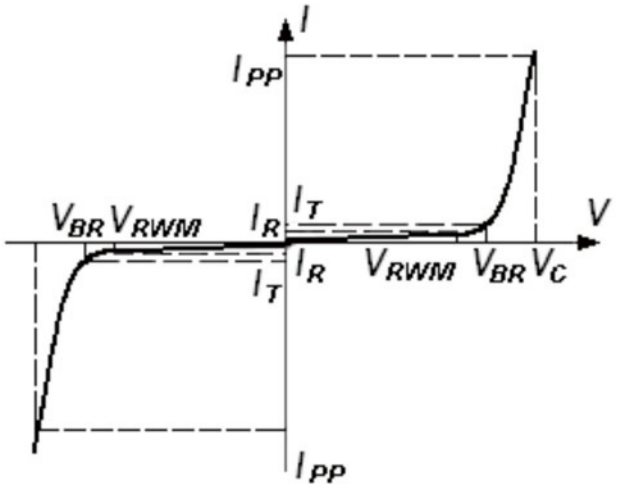
Parameter	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20μs) @ TA=25℃	PD	150	W
Peak Pulse Current (tp = 8/20□s)	IPP	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V ESD	+/- 17 +/- 12	KV
Junction and Storage Temperature Range	TJ,TSTG	-55 to 150	℃

Electrical Characteristics

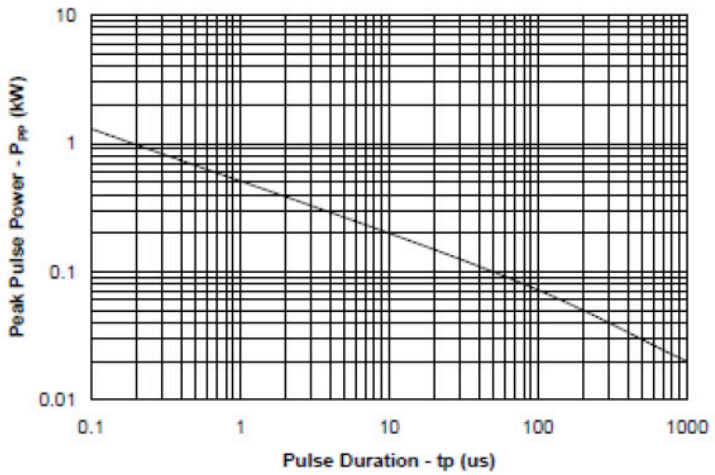
Part Numbers	VBR min	VC	VRWM	VF Max	IRWM.	Cj TYP
	V	V	V	V	uA	PF
ESDF5V4	6	15	5	1	1	0.3

1. Capacitance is measured at f=1MHz, VR=0V
2. VBR is measured with a pulse test current IT at an ambient temperature of 25°C.

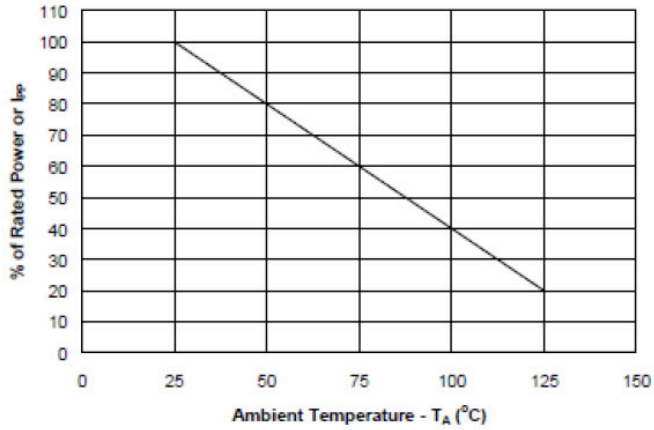
Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
I_T	Test Current
V_{BR}	Breakdown Voltage @ I_T

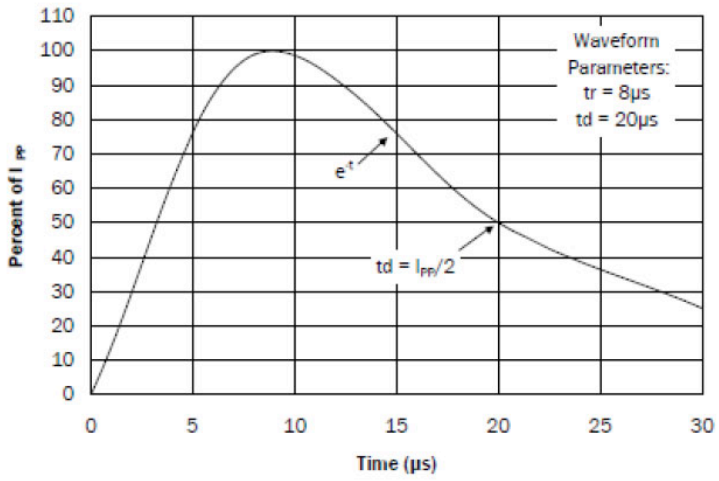


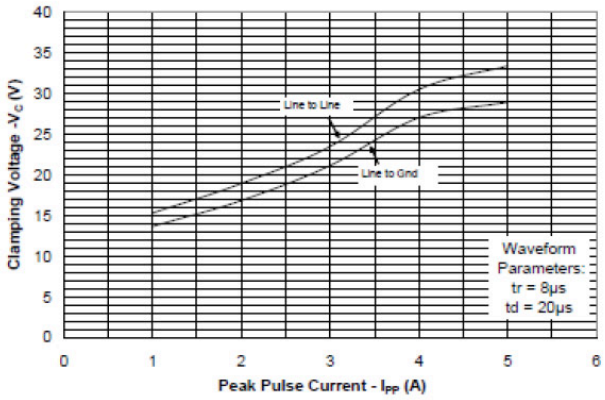
Non-Repetitive Peak Pulse Power vs. Pulse Time



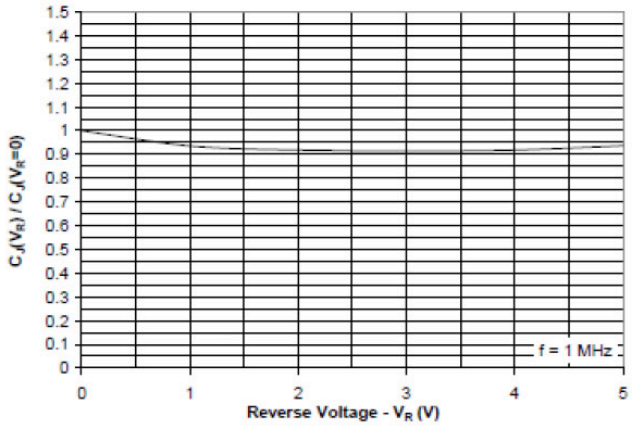
Power Derating Curve

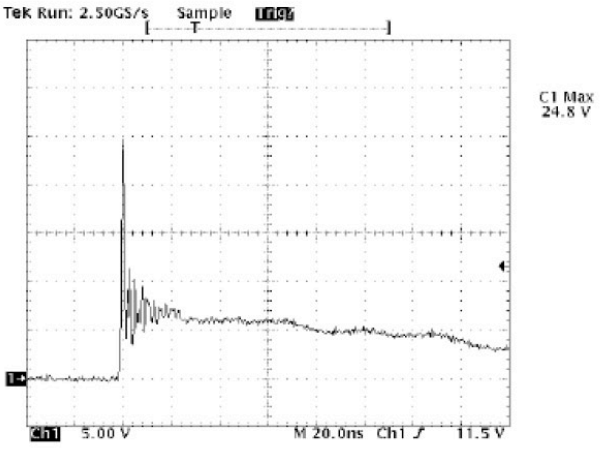




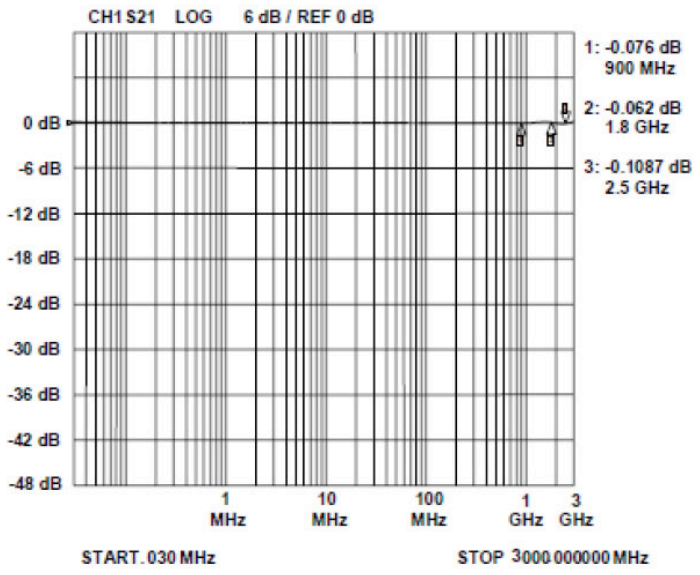


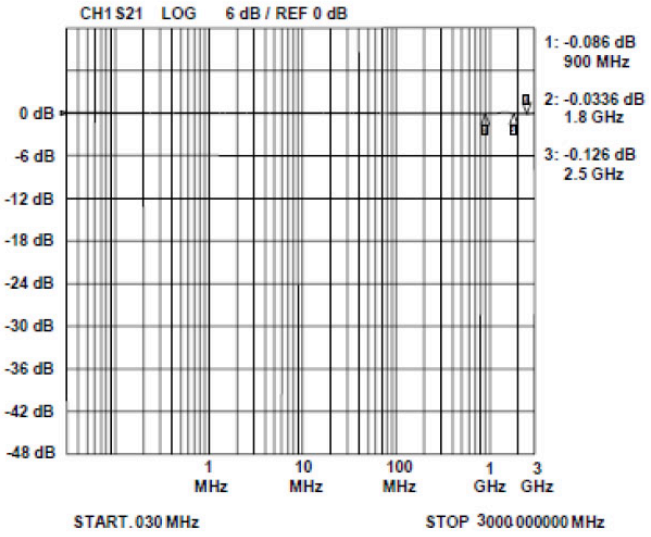
Normalized Capacitance vs. Reverse Voltage



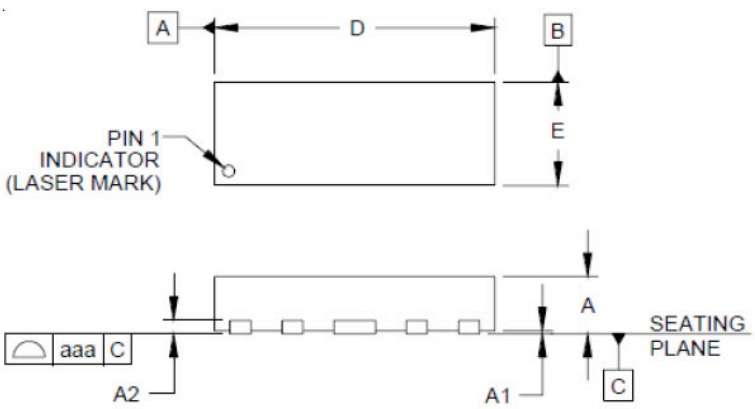


Insertion Loss S21 - I/O to GND





DFN-10 package Information



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	.023	.026	0.50	0.58	0.65
A1	0.00	.001	.002	0.00	0.03	0.05
A2		(.005)			(0.13)	
b	.006	.008	.010	0.15	0.20	0.25
b1	.014	.016	.018	0.35	0.40	0.45
D	.102	.106	.110	2.60	2.70	2.80
E	.035	.039	.043	0.90	1.00	1.10
e	.020 BSC			0.50 BSC		
e1	.024 BSC			0.60 BSC		
L	.012	.015	.017	0.30	0.38	0.425
N	10			10		
aaa	.003			0.08		
bbb	.004			0.10		