ESDALC6V1C2

Quad low capacitance TRANSIL™ array for ESD protection

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

This device is particularly adapted to the protection of symmetrical signals

Features

- 4 unidirectional TRANSIL functions.
- Breakdown voltage V_{BR} = 6.1 V min.
  - Low diode capacitance (12 pF @ 0 V)
  - Low leakage current (< 500 nA @ 3 V)
  - very small PCB area (1.33 mm^2)
- Coated lead free package

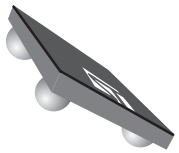
Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

Description

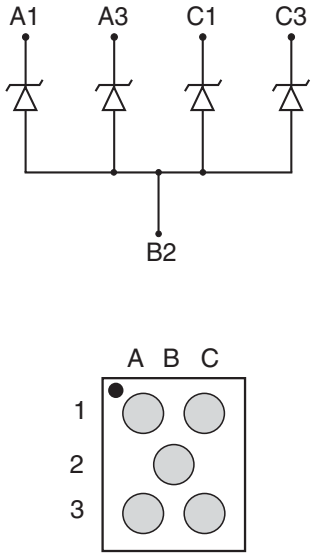
The ESDALC6V1C2 is a monolithic array designed to protect up to 4 lines against ESD transients. The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: TRANSIL is a trademark of STMicroelectronics



Coated lead free Flip-Chip (5 bumps)

Functional diagram



Order code

Part number	Marking
ESDALC6V1C2	ED

Complies with the following standards:

IEC 61000-4-2 15 kV (air discharge)

8 kV (contact discharge)

MIL STD 883E - Method 3015-7: class 3

25 kV (Human body model)

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25° C)

Symbol	Parameter			Value	Unit
V_{PP}	ESD discharge	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge		± 15 ± 8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs. (1)		$T_{j\ initial} = T_{amb}$	25	W
T_j	Junction temperature			125	°C
T_{stg}	Storage temperature			- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm for case			260	°C
T_{OP}	Operating temperature range			- 40 to + 125	°C

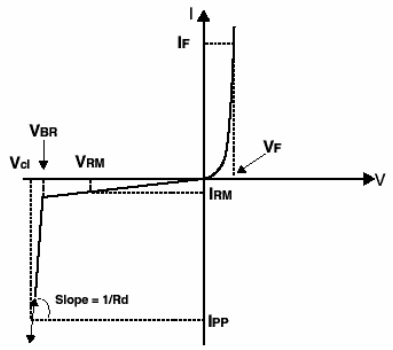
1. For a surge greater than the maximum values, the diode will fail in short-circuit

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient on printed circuit on recommended pad layout	150	°C/W

Table 3. Electrical characteristics

Symbol	Parameter
V_{RM}	Stand-of voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop



Type	I_{RM} @ V_{RM}		V_{BR} @ I_R			R_D	αT	C
	µA max	V	Vmin	Vmax	mA	Typ	10-4/°C max	pFtyp @0 V
ESDALC6V1C2	0.5	3	6.1	7.2	1	1	5	12

Figure 1. Peak power dissipation versus initial junction temperature

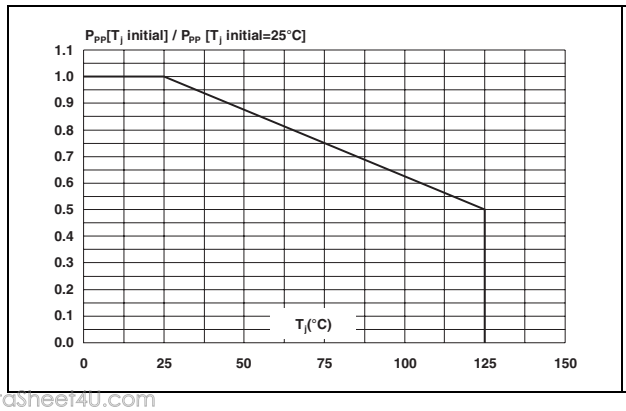


Figure 2. Peak pulse power versus exponential pulse duration (T_j initial = 25°C)

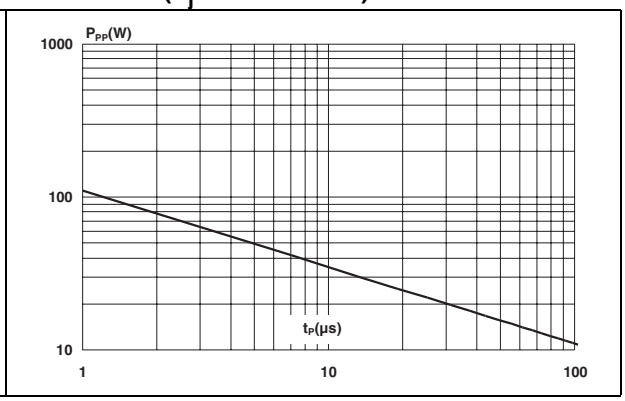


Figure 3. Clamping voltage versus peak pulse current (T_j initial = 25°C), rectangular waveform t_p = 2.5 µs).

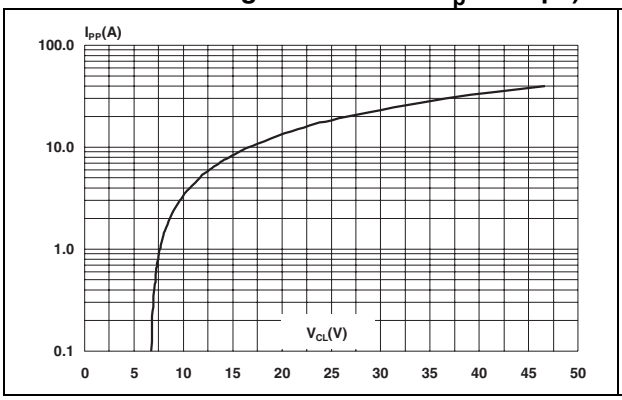


Figure 4. Capacitance versus reverse applied voltage (typical values)

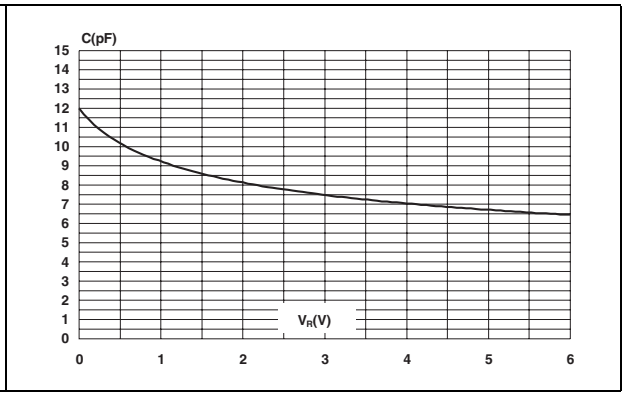
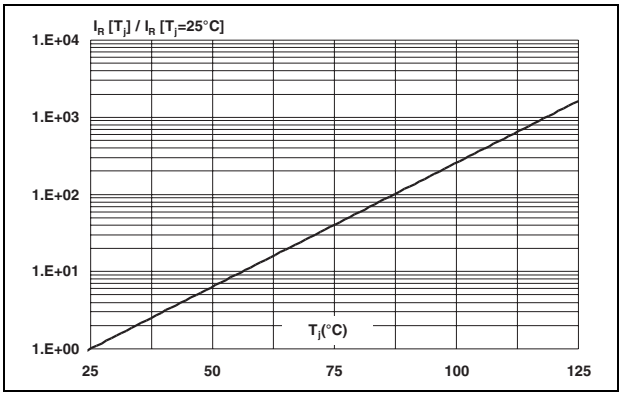


Figure 5. Relative variation of the leakage current versus junction temperature (typical values)



2 Ordering information scheme

ESDA LC - 6V1 C2

ESD Array

Low capacitance

V_{BR} min = 6.1 V

Package

C = Coated Flip-Chip

2 = Leadfree Pitch = 500µm, Bump = 315µm

3 Package information

Figure 6. Flip-Chip dimensions

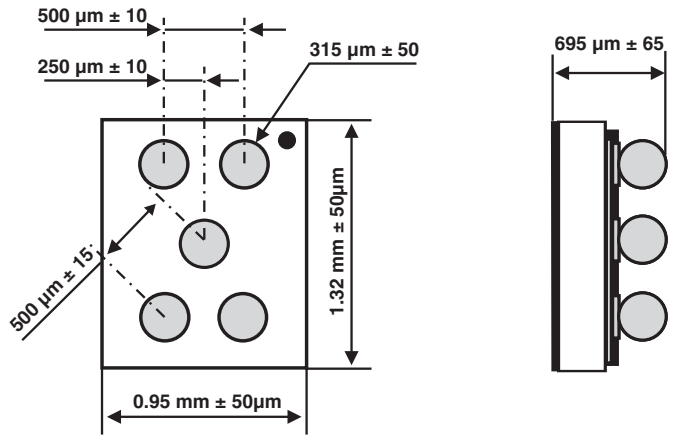


Figure 7. Flip-Chip footprint

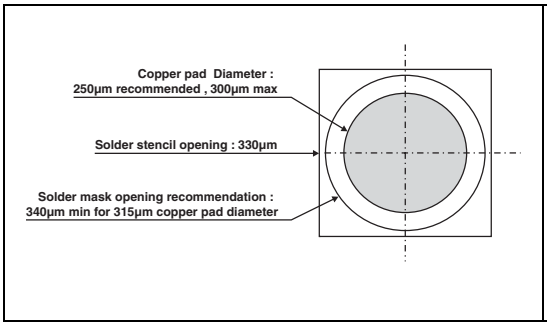


Figure 8. Marking

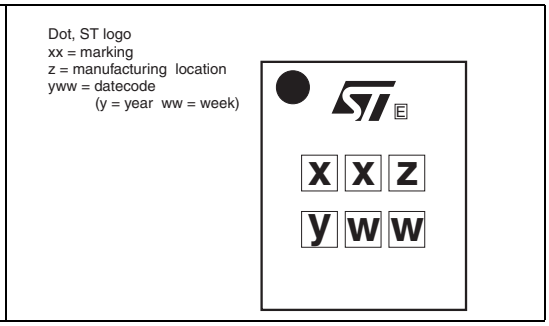
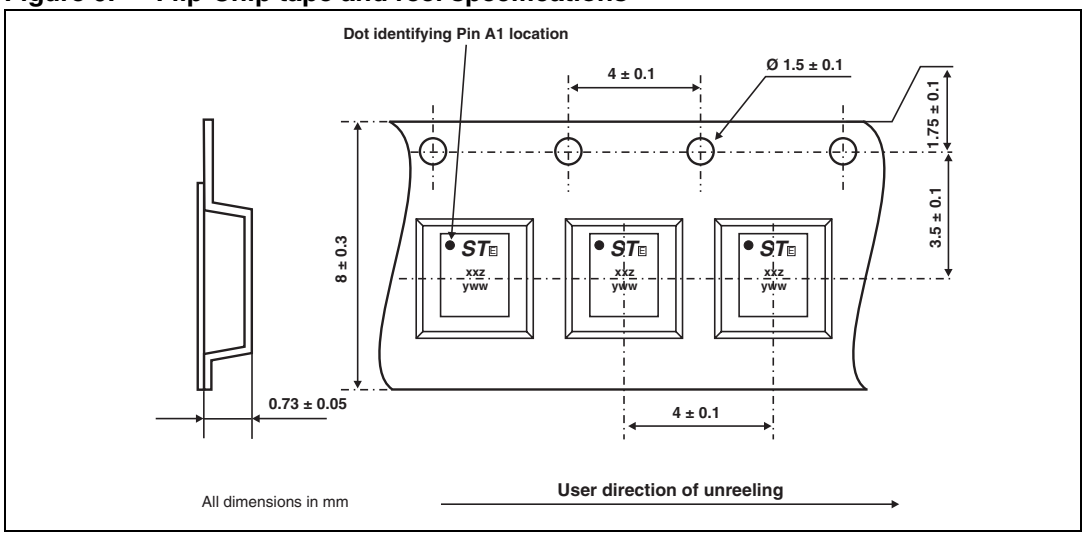


Figure 9. Flip-Chip tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1C2	ED	Flip-Chip	2.1 mg	5000	Tape and reel

5 Revision history

Date	Revision	Changes
07-Aug-2006	1	Initial release.

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