WEITRON

ESD9L5.0

Surface Mount TVS For ESD Protection Diode with Ultra-Low Capacitance

TRANSIENT VOLTAGE SUPPRESSORS
150m WATTS
5.0 VOLTS

Pb Lead(Pb)-Free

General Description:

The ESD9L5.0 is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events.Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

SOD-923

Features:

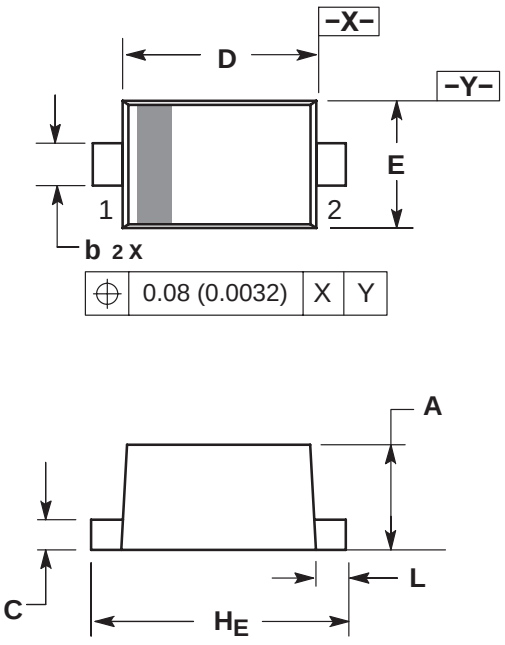
*Small Body Outline Dimensions:0.039" x 0.024" (1.0 mm x 0.60 mm)
*Low Body Height: 0.016" (0.4 mm)
*Stand–off Voltage: 5.0 V
*Low Leakage
*Response Time is Typically < 1 ns
*IEC61000–4–2 Level 4 ESD Protection
*This is Pb–Free Devices

Characteristics:

*CASE: Void-free, Transfer-molded, Thermosetting Plastic Epoxy Meets UL 94 V-0
*LEAD FINISH:100% Matte Sn (Tin)
*QUALIFIED MAX REFLOW TEMPERATURE:260˚C Device Meets MSL 1 Requirements

SOD-923 Outline Dimensions

Unit:mm



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.36	0.40	0.43
b	0.15	0.20	0.25
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
H_E	0.95	1.00	1.05
L	0.05	0.10	0.15

Maximum Ratings(T_A=25°C Unless Otherwise Noted)

Characteristic	Symbol	Value	Unit
Total Power Dissipation on FR-5 Board (Note1) @ Ta=25°C	PD	150	mW
IEC61000-4-2(ESD) air discharge contact discharge		±15 ±10	KV
Lead Solder Temperature -Maximum (10 second Duration)	T_L	260	°C
Junction and Storage Temperature Range	T_J ,T_{stg}	-55 to +150	°C

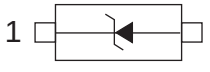
Stresses exceeding Maximum Ratings may damage the device. Maximum Rating are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. FR-5 = 1.0*0.75*0.62 in.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.0 V Max. @ I_F = 10 mA for all types)

Device	Device Marking	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	C (pF)		V_C (V) @ I_{PP} = 1 A (Note 3)	V_C
		Max	Max	Min	mA	Typ	Max	Max	Per IEC61000–4–2 (Note 4)
ESD9L5.0	D	5.0	1.0	5.4	1.0	0.5	0.9	9.8	Figures 1 and 2 See Below

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. Surge current waveform per Figure 5.
4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

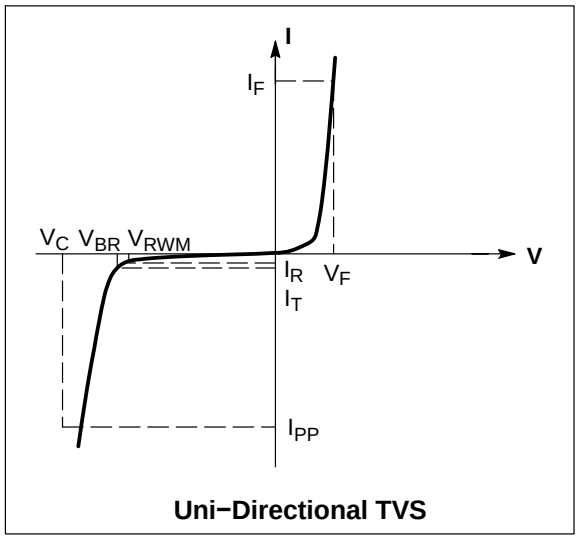
Eqivalent Circuit Diagram



Pin 1. CATHODE
2.ANODE

Typical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{PK}	Peak Power Dissipation
C	Max. Capacitance @V_R = 0 and f = 1 MHz



Uni−Directional TVS

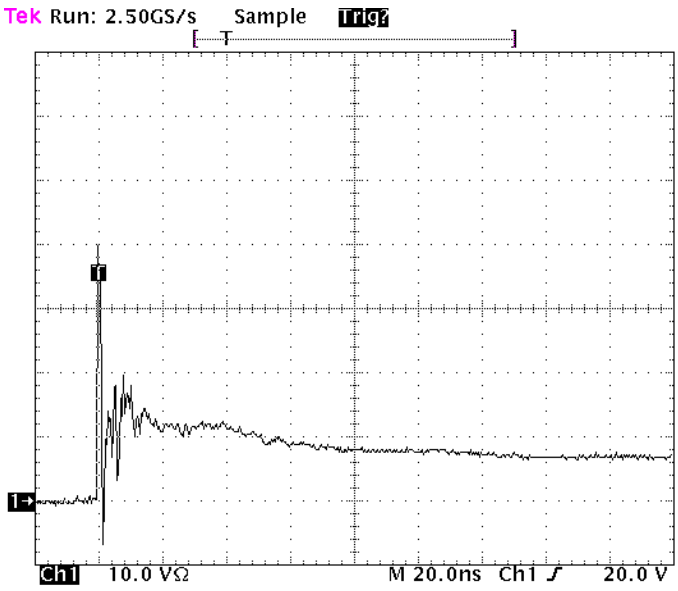


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

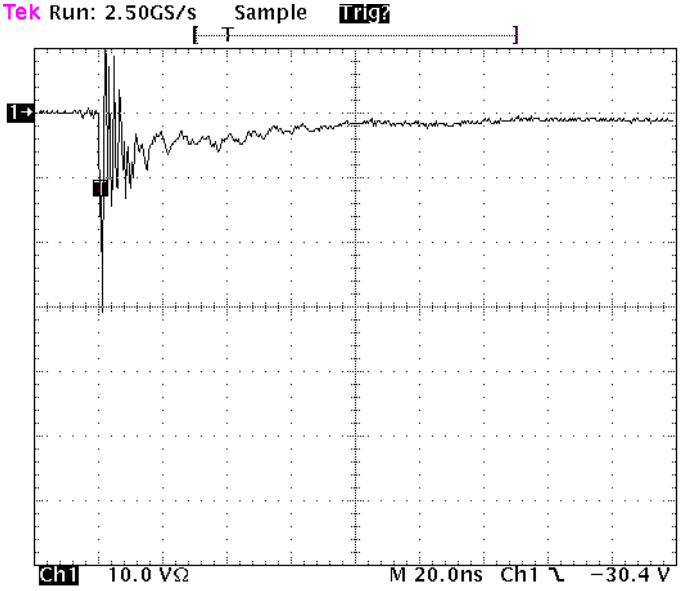


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000–4–2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

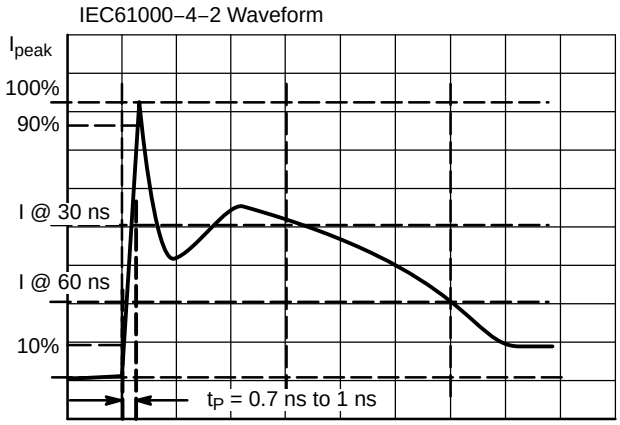


Figure 3. IEC61000–4–2 Spec

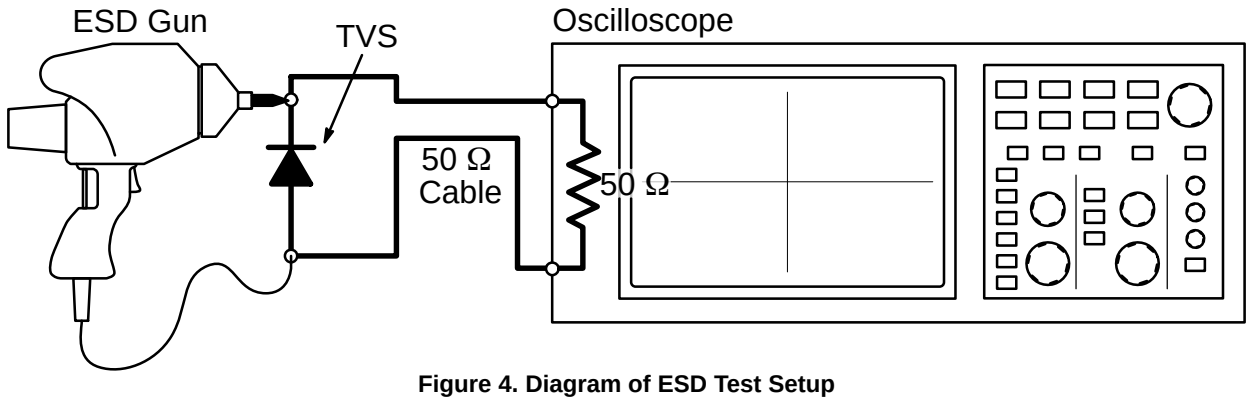


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

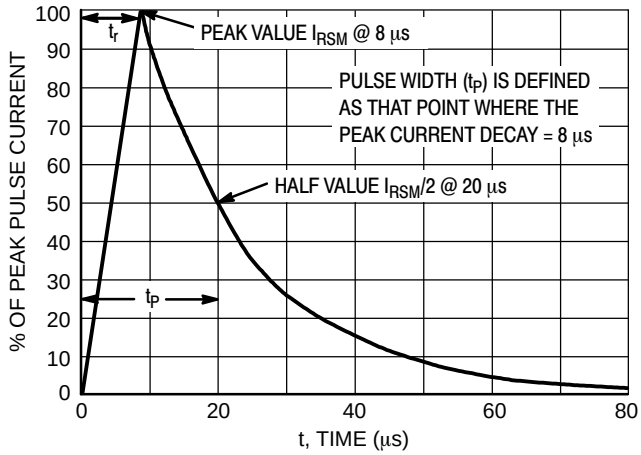


Figure 5. 8 X 20 μs Pulse Waveform