# ESD11A3.3DT5G SERIES

# Transient Voltage Suppressors

## ESD Protection Diodes in Ultra Small SOT−1123 Package

The ESD11A Series is designed to protect voltage sensitive components from damage due to ESD. These parts provide excellent ESD clamping capability and fast response time to enhance the immunity of the end application from system level ESD stress such as IEC61000−4−2. Two uni−directional TVS diodes are housed in the ultra small SOT−1123 package, making these parts ideal for ESD protection on designs where board space is at a premium, such as cell phones, MP3 players and many other portable handheld electronic devices.

**Specification Features:**

- Low Clamping Voltage
- Small Body Outline Dimensions:
  0.039” x 0.024” (1.0 mm x 0.6 mm)
- Low Body Height: 0.016″ (0.4 mm)
- Stand−off Voltage: 3.3 V − 5 V
- Low Leakage
- Response Time is Typically < 1 ns
- IEC61000−4−2 Level 4 ESD Protection
- These are Pb−Free Devices

**Mechanical Characteristics:**

**CASE:** Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V−0
**LEAD FINISH:** 100% Matte Sn (Tin)
**MOUNTING POSITION:** Any
**QUALIFIED MAX REFLOW TEMPERATURE:** 260°C
Device Meets MSL 1 Requirements

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| IEC 61000−4−2 (ESD) Contact | | ±15 | kV |
| Total Power Dissipation on FR−5 Board (Note 1) @ $T_A$ = 25°C | $P_D$ | 150 | mW |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Junction Temperature Range | $T_J$ | −55 to +125 | °C |
| Lead Solder Temperature − Maximum (10 Second Duration) | $T_L$ | 260 | °C |

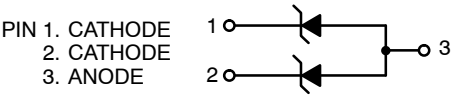
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. FR−5 = 1.0 x 0.75 x 0.62 in.

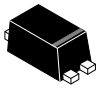
See Application Note AND8308/D for further description of ESD maximum ratings.

**ON Semiconductor®**

**http://onsemi.com**

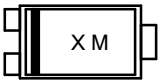
PIN 1. CATHODE
2. CATHODE
3. ANODE



**SOT−1123**
**CASE 524AA**

**MARKING DIAGRAM**




X = Specific Device Code
M = Date Code

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| ESD11AxxDT5G | SOT−1123 (Pb−Free) | 8000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

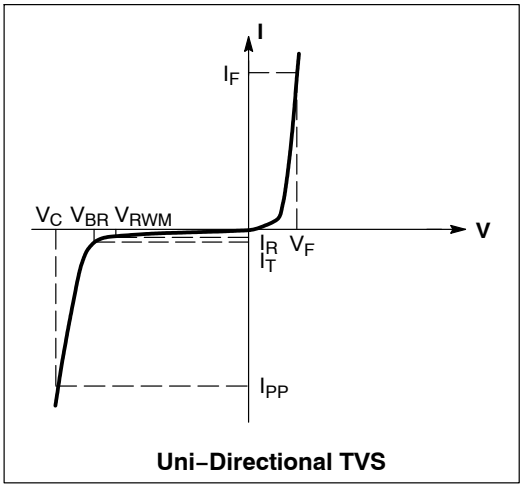
**DEVICE MARKING INFORMATION**

See specific marking information in the device marking column of the table on page 2 of this data sheet.

## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Reverse Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Working Peak Reverse Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $I_F$ | Forward Current |
| $V_F$ | Forward Voltage @ $I_F$ |
| $P_{pk}$ | Peak Power Dissipation |
| C | Capacitance @$V_R$ = 0 and f = 1 MHz |




**Uni−Directional TVS**

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted, $V_F$ = 0.9 V Max. @ $I_F$ = 10 mA for all types)

| Device | Device Marking | $V_{RWM}$ (V) | $I_R$ (μA) @ $V_{RWM}$ | $V_{BR}$ (V) @ $I_T$ (Note 2) | $I_T$ | C (pF), uni−directional (Note 3) | | $V_C$ (V) @ $I_{PP}$ = 1 A (Note 5) | $V_C$ (V) IEC61000−4−2 (Note 6) |
|---|---|---|---|---|---|---|---|---|---|
| | | Max | Max | Min | mA | Typ | Max | Max | Typ |
| ESD11A3.3DT5G | 2* | 3.3 | 1.0 | 5.2 | 1.0 | 25 | 35 | 7.8 | Figures 1 thru 4 |
| ESD11A5.0DT5G | 3* | 5.0 | 0.1 | 6.2 | 1.0 | 20 | 30 | 9.5 | Figures 1 thru 4 |

*Rotated 90° clockwise.

2. $V_{BR}$ is measured with a pulse test current $I_T$ at an ambient temperature of 25°C.
3. Uni−directional capacitance at f = 1 MHz, $V_R$ = 0 V, $T_A$ = 25°C (pin1 to pin 3; pin 2 to pin 3).
4. Bi−directional capacitance at f = 1 MHz, $V_R$ = 0 V, $T_A$ = 25°C (pin1 to pin 2).
5. Surge current waveform per Figure 7.
6. Typical waveform. For test procedure see Figures 5 and 6 and Application Note AND8307/D.

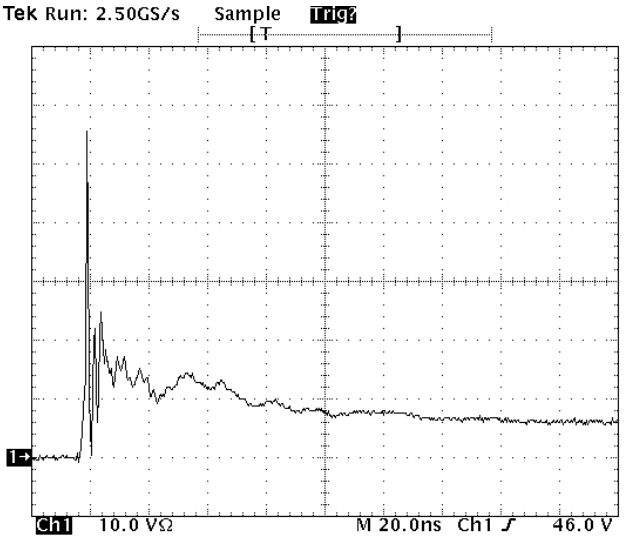



**Figure 1. ESD11A3.3D Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000−4−2**

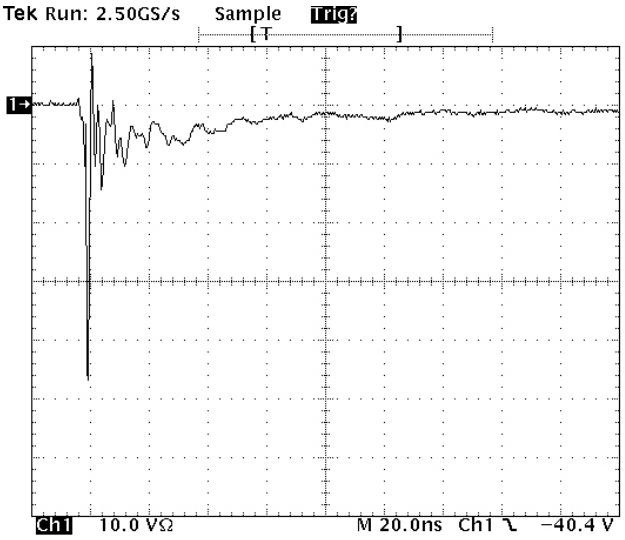



**Figure 2. ESD11A3.3D Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000−4−2**

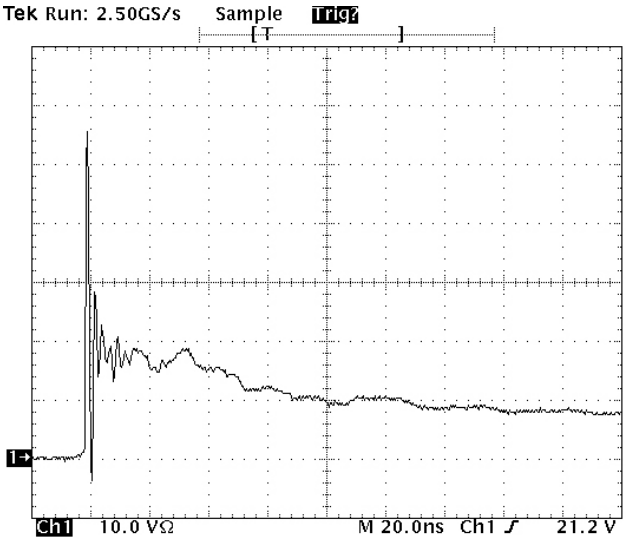



**Figure 3. ESD11A5.0D Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000−4−2**

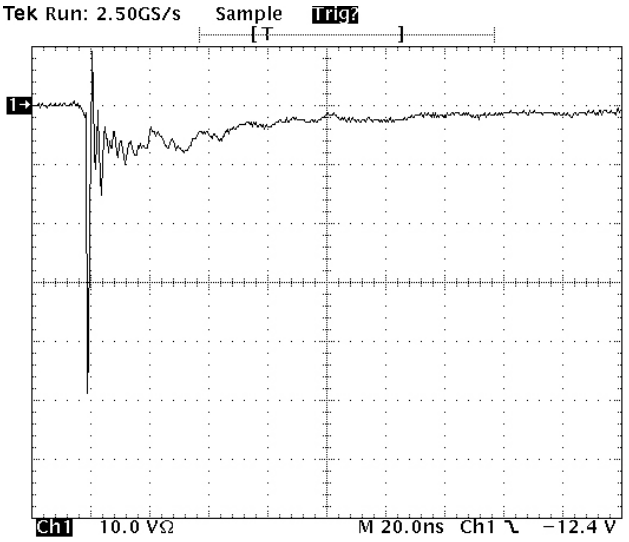



**Figure 4. ESD11A5.0D Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000−4−2**

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

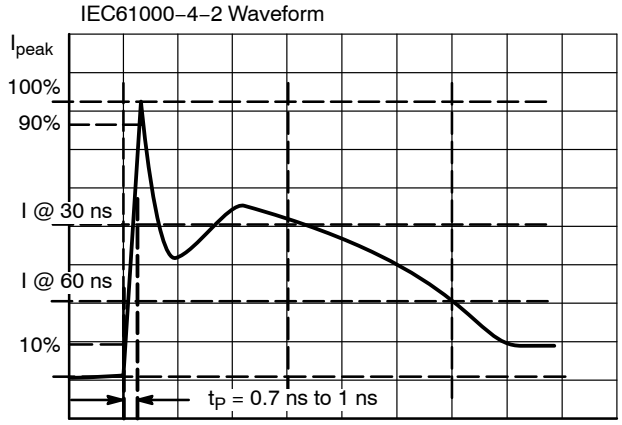



**Figure 5. IEC61000−4−2 Spec**

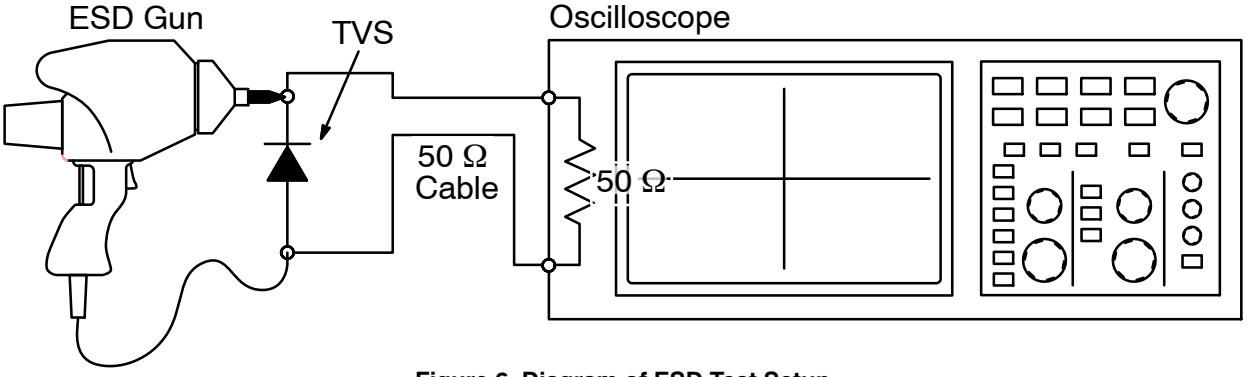



**Figure 6. Diagram of ESD Test Setup**

**The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.**

**ESD Voltage Clamping**

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

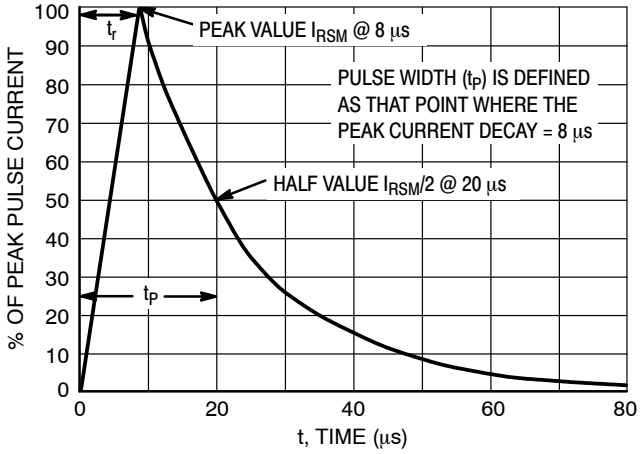
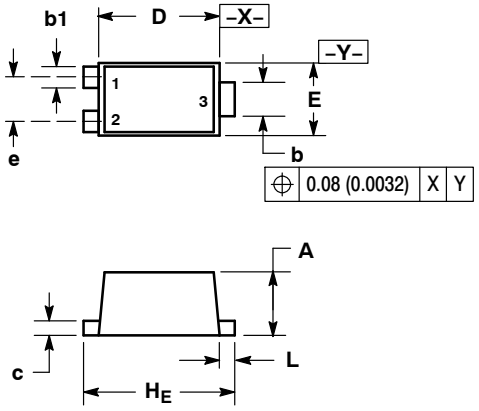



**Figure 7. 8 X 20 μs Pulse Waveform**

## PACKAGE DIMENSIONS

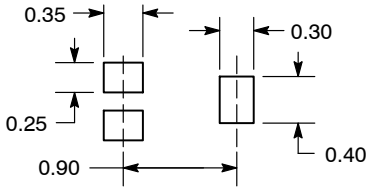
**SOT−1123**
CASE 524AA−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.34 | 0.37 | 0.40 | 0.013 | 0.015 | 0.016 |
| b | 0.15 | 0.22 | 0.28 | 0.006 | 0.009 | 0.011 |
| b1 | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| c | 0.07 | 0.12 | 0.17 | 0.003 | 0.005 | 0.007 |
| D | 0.75 | 0.80 | 0.85 | 0.030 | 0.031 | 0.033 |
| E | 0.55 | 0.60 | 0.65 | 0.022 | 0.024 | 0.026 |
| e | 0.35 | --- | 0.40 | 0.014 | ---- | 0.016 |
| $H_E$ | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| L | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |

## SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
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