Analog Reinvented

ES9601C
SABRE Headphone Driver
Datasheet

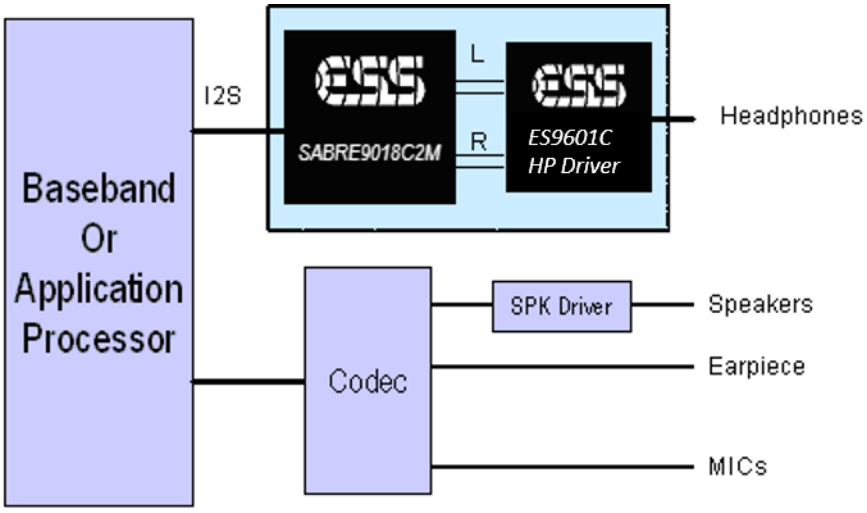
The ***ES9601C Headphone Driver*** is the industry's highest performance, standalone headphone driver targeted for audiophile-grade portable applications such as mobile phones, tablets and digital music players.

The ***ES9601C Headphone Driver*** delivers 122dB SNR and –117dB THD+N, a new benchmark in standalone headphone driver performance that will satisfy the most demanding audio enthusiasts.

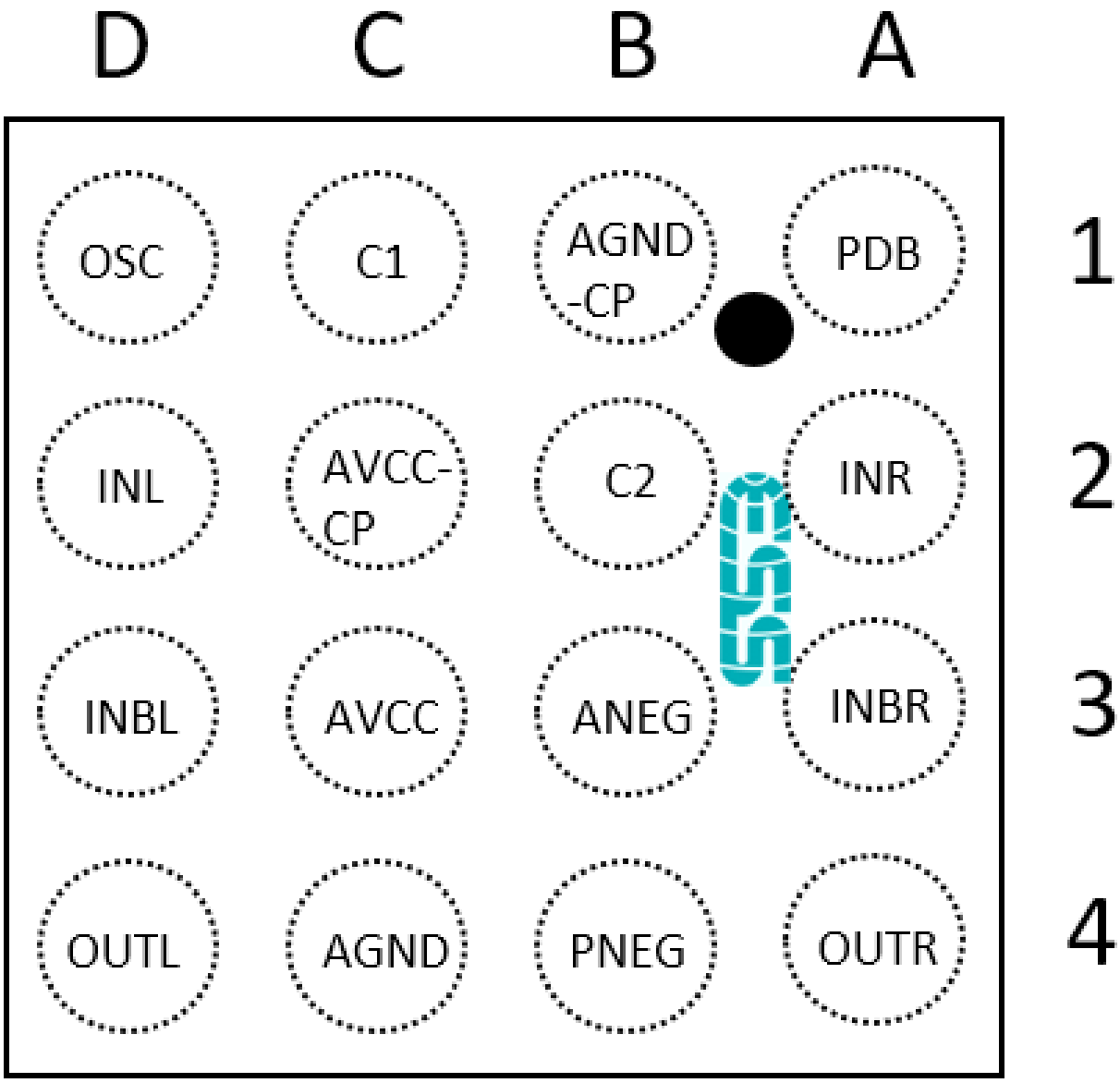
The ***ES9601C Headphone Driver*** is available in a 16-pin CSP package.

Like ESS' high-quality SABRE^{32} Reference DACs, the ***ES9601C Headphone Driver*** sets the standard for HD Audio performance with **SABRE SOUND**® for today's most demanding audio applications.

FEATURE	DESCRIPTION
Unmatched performance ○ +122dB SNR ○ –117dB THD+N: 2Vrms @ 600Ω load ○ –100dB THD+N: 30mW into 32Ω load	○ Industry's highest performance audio headphone or line-out driver for mobile applications ○ Delivers SABRE SOUND® all the way to the headphones
Ground referenced output	○ Eliminates large DC blocking capacitors
Pop-noise suppression	○ Powers up and down without any clicks or pops
Charge pump for negative supply	○ Single AVCC operation simplifies power supply
16-Pin CSP package	○ Minimizes PCB footprint
< 9mA / 5μA, quiescent / standby current	○ Maximizes battery life



PIN LAYOUT



CSP View (Top View)
Detailed Package Dimensions on page 15

PIN DESCRIPTIONS

PIN	Name	I/O	Description
A1	PDB	I	Active-low Power Down (High for normal operation)
A2	INR	I	Differential Positive Analog Input (Right Channel)
A3	INBR	I	Differential Negative Analog Input (Right Channel)
A4	OUTR	O	Analog Right Channel Output. A 4.7Ω resistor should be placed between OUTR and the load to provide amplifier short-circuit protection
B1	AGND_CP	-	Analog Ground (Charge Pump)
B2	C2	-	Analog Flying Capacitor. Connect a 2.2μF X5R ceramic capacitor between C1 and C2, the capacitor value may be increased up to 4.7μF to improve regulation. If a polarized capacitor is used, the +ve terminal must be connected to C1.
B3	ANEG	I	Negative Amplifier Supply Input. Connect to PNEG when the internal charge pump is being used, and connect a 22μF minimum X5R ceramic hold capacitor to ground. Increasing the hold capacitor value will improve supply regulation but increases start-up time. If a polarized capacitor is used, the +ve terminal must be connected to AGND.
B4	PNEG	O	Negative Charge Pump Output. Connect to ANEG when the internal charge pump is being used, and connect a 22μF minimum X5R ceramic hold capacitor to ground. Increasing the hold capacitor value will improve supply regulation but increases start-up time. If a polarized capacitor is used, the +ve terminal must be connected to AGND. PNEG is left open when an external –3.3V supply is used.
C1	C1	-	Analog Flying Capacitor. Connect a 2.2μF X5R ceramic capacitor between pins C1 and C2, the capacitor value may be increased up to 4.7μF to improve regulation. If a polarized capacitor is used, the +ve terminal must be connected to C1.
C2	AVCC_CP	-	Analog Power (Charge Pump)
C3	AVCC	-	Analog Supply for the Left and Right Channels
C4	AGND	-	Analog Ground
D1	OSC	I/O	Oscillator Input/Output pin. In normal operation, 1D outputs the charge-pump clock. When there is more than one ES9601C, the OSC pins may be shorted together to synchronize the clocks and minimize potential “beat frequency effects”. If the OSC pin is grounded the charge-pump clock stops. Stopping the clock reduces current drain and allows an external –3.3V supply to be connected to ANEG so low impedance loads can be driven (PNEG should be left open). An external clock can also be connected to the OSC pin and should be in the range 100kHz to 150kHz
D2	INL	I	Differential Positive Analog Input (Left Channel)
D3	INBL	I	Differential Negative Analog Input (Left Channel)
D4	OUTL	O	Analog Left Channel Output. A 4.7Ω resistor should be placed between OUTL and the load to provide amplifier short-circuit protection

FUNCTIONAL DESCRIPTION

The ES9601C has a pair of CMOS FET input amplifiers that exhibit a total A-weighted SNR of better than 122dB when driving 2Vrms into a 600Ω load. The ES9601C has an open-loop gain in excess of 120dB which together with the input stage linearity is the key to its unparalleled –117dB distortion performance. Please note that the amplifier distortion performance far exceeds that of typical external passive components. Therefore, to achieve the THD performance specified for the ES9601, ensure that the external resistors have a very low, voltage coefficient of resistance, e.g. thin film resistors. Close tolerance ±0.1% thin-film resistors are recommended for all gain-defining components.

Charge Pump

The ES9601 features a low-noise charge pump. The 120kHz switching frequency is above the audio band and, thus, does not interfere with audio signals. The switches are controlled by turn-on and turn-off transistors in a particular sequence that minimizes pops and clicks. The IC requires a 2.2μF minimum X5R ceramic flying capacitor between pins C1 and C2 and a 22μF minimum X5R ceramic hold capacitor from PNEG_CP to AGND_CP. The chip's OSC pin offers three connection options; capacitance may be added from OSC to ground to slow down the oscillator (100kHz minimum), a logic signal can drive the OSC pin to set a fixed frequency, or the OSC pins of several ES9601C chips may be connected together to force them to run synchronously.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range select capacitors with a minimum X5R dielectric, the X7R dielectric is preferred. The charge pump can be disabled by grounding pin 1D which reduces quiescent current from the +3.3V supply. Disabling the charge pump is recommended when using an external –3.3V supply.

Flying Capacitor (C4, see Figure 2)

The value of the flying capacitor (C4) affects the charge pump's load regulation and output resistance. A C4 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C4 improves load regulation and reduces the charge-pump output resistance to an extent. With a 2.2μF flying capacitor, the on-resistance of the switches dominates. Use a low-ESR ceramic or electrolytic capacitor for C4. If an electrolytic capacitor is used the correct polarity must be observed, see Figure 2. The flying capacitor C4 can be eliminated when an external –3.3V supply is used and the internal oscillator is disabled by grounding the OSC pin.

Hold Capacitor (C2, see Figure 2)

The hold capacitor value and ESR directly affect the ripple at PNEG. Use a low-ESR 22μF minimum capacitor for C2 and also choose the correct voltage rating. C2 can be a ceramic or electrolytic capacitor, if an electrolytic capacitor is used, the correct polarity must be observed, see Figure 2. Increasing the value of the hold capacitor will improve regulation but increases start-up time.

Amplifier Gain

The recommended gain setting for ES9601C is 0dB. When working with ES901xK2M, only RF is needed. Since the RIN is the equivalent DAC output impedance, the recommend value for RF is 806Ω which gives the best DNR.

Driving a Low Impedance Load

In order to drive a 32Ω load or lower it is necessary to use an external –3.3V supply and disable the internal charge pump. An external low-noise supply is required to source the high current drawn by the 32Ω load. Pin 20 should be grounded to stop the oscillator, PNEG is left open, and the external –3.3V supply is connected to ANEG with a 22μF minimum X5R ceramic hold capacitor. To prevent clicks/pops at startup and shutdown the +3.3V and –3.3V supplies should be sequenced. The +3.3V must be ON and stay ON before connecting or disconnecting the –3.3V external supply.

Compensation Components (see Figure 2)

For optimum performance, the following capacitors and resistors should be included in all configurations of the ES9601C. R1/C1 and R13/C8 control the bandwidth of the ES9601C, along with the matching networks R6/C2 and R7/C7. All these compensation capacitors should have a low temperature coefficient. NP0/C0G types are recommended.

Short-Circuit Protection (see Figure 2)

To protect the ES9601C under short-circuit conditions series 4.7Ω resistors should be placed in series with each output, OUTL and OUTR.

ES9601C Block Diagram

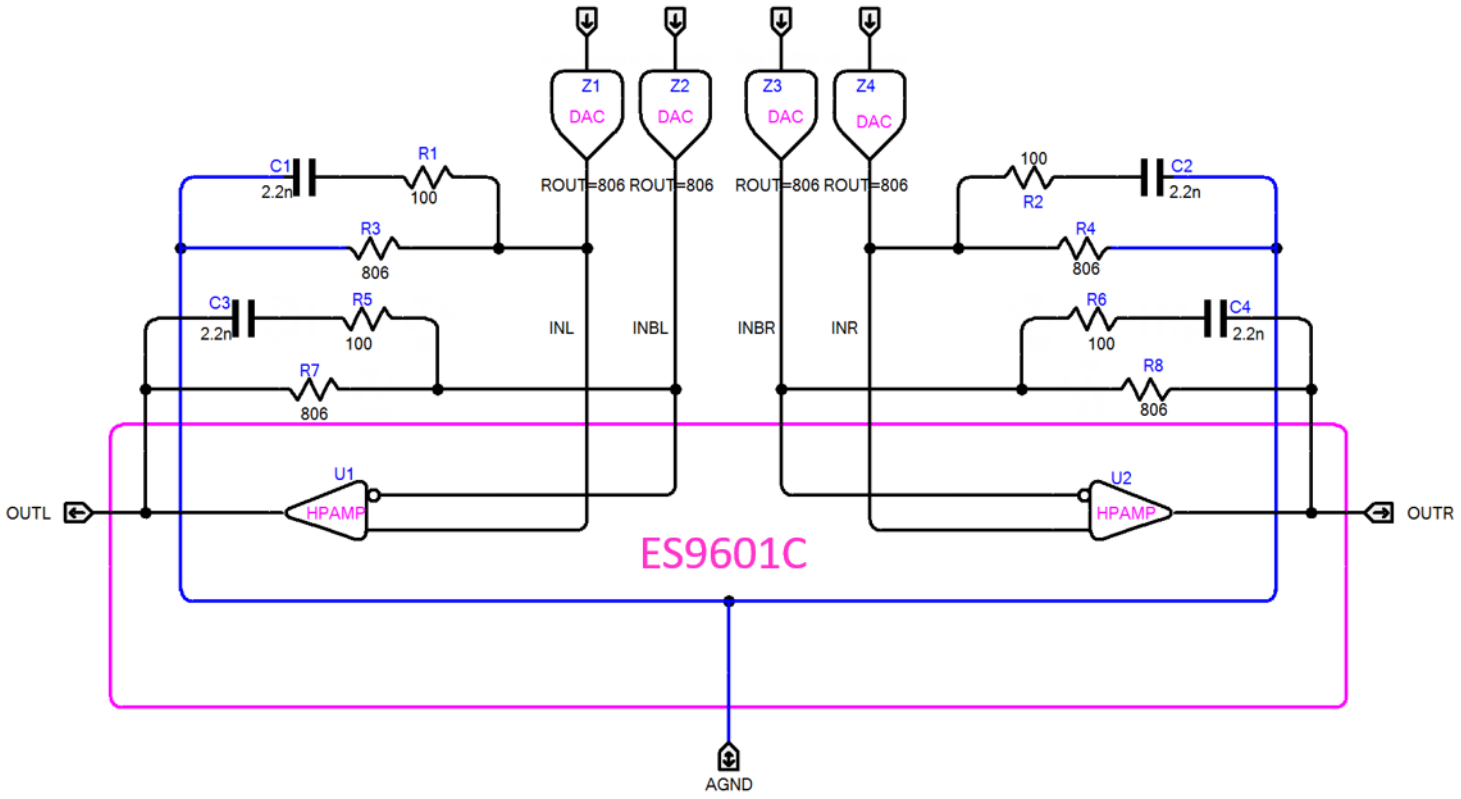


Figure 1. Block Diagram of the ES9601C plus external Gain Setting and Compensation components.

APPLICATION DIAGRAM

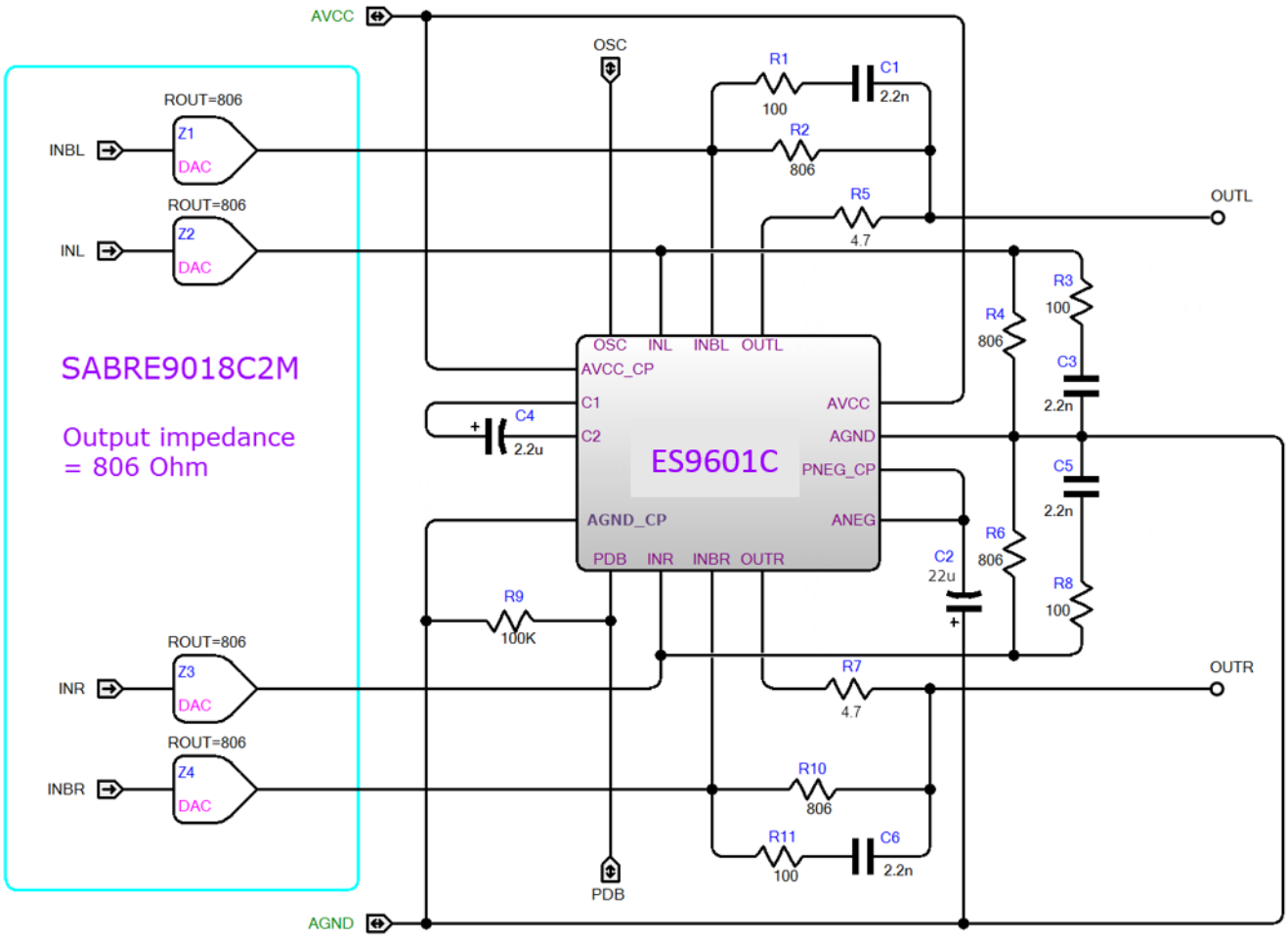


Figure 2. SABRE9018C2M (CSP) Dual SABRE DAC driving the ES9601C Headphone Amplifier.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Positive Supply Voltage (AVCC, AVCC_CP)	+4.7V with respect to GND
Negative Supply Voltage (ANEG & PNEG)	–4.7V with respect to GND
Input Voltage (INL, INR, INBL, INBR)	ANEG < VIN < AVCC
Differential Input Voltage (INL, INR, INBL, INBR)	ANEG < VDiff < AVCC
Output Short-Circuit Protection	Continuous with 4.7Ω protection resistors
Storage temperature	–65°C to +105°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to DVCC+ 0.3V
ESD Protection Human Body Model (HBM) Machine Model (MM)	 2000V 200V

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS		
Operating Temperature Range	T_A	–20°C to +70°C		
Power Supply		**Voltage**	**Quiescent Current (*1)**	**Standby Current**
Analog power supply voltage	AVCC_CP AVCC_L AVCC_R	+3.3V ± 5%	5.6mA typical, 9mA maximum	< 5μA (*2)
Power Supply		**Load Resistance**	**Supply Current**	**Output Voltage**
Analog supply current at +3.3V	I_{SY}	32Ω	49mA typical	800mVrms @ 1kHz (*3)

Notes:

(*1) Input idling, output unloaded, internal oscillator, all external supply voltages at nominal center values
(*2) with PDB held low
(*3) 800mVrms sine wave across 32Ω load produces a 20mW output

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Minimum	Maximum	Unit
VIH	High-level input voltage	1.4		V
VIL	Low-level input voltage		0.4	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	I_B	INL, INBL, INR, INBR inputs	–1.0	0.1	+1.0	nA
Output Offset Voltage	V_{OS}	OUTL to OUTR, no DC input	–2.0	0.1	+2.0	mV

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

T_A = 25ºC, AVCC_CP = AVCC_L = AVCC_R = +3.3V, 1kHz signal, C2 = 22µF, C4 = 2.2µF, ANEG = PNEG (Figure 2 configuration)

1. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode
2. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	VOUT = 2.0Vrms, A-weighted, RL = 600Ω		122		dB
Total Harmonic Distortion plus Noise	THD+N	VOUT = 2.0Vrms, RL = 600Ω		–117		dB
		POUT = 30mW, RL = 32Ω		–100		dB
Power Supply Rejection	PSR	fin = 10Hz, 200mVp-p ripple	-	97	-	dB
		fin = 217Hz, 200mVp-p ripple	-	97	-	dB
		fin = 1kHz, 200mVp-p ripple	-	94	-	dB
		fin = 10kHz, 200mVp-p ripple	-	74	-	dB

Test Conditions (unless otherwise stated)

T_A = 25ºC, AVCC_CP = AVCC_L = AVCC_R = +3.3V, 1kHz signal, C2 = 22µF, C4 = 2.2µF, OSC pin grounded, ANEG = –3.3V ext.

1. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode
2. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	VOUT = 2.0Vrms, A-weighted, RL = 600Ω		122		dB
Total Harmonic Distortion plus Noise	THD+N	VOUT = 2.0Vrms, RL = 600Ω		–117		dB
		VOUT = 1.4Vrms, RL = 32Ω		–100		dB
		VOUT = 1.0Vrms, RL = 16Ω		–97		dB
Power Supply Rejection	PSR	fin = 10Hz, 200mVp-p ripple	-	106	-	dB
		fin = 217Hz, 200mVp-p ripple	-	102	-	dB
		fin = 1kHz, 200mVp-p ripple	-	95	-	dB
		fin = 10kHz, 200mVp-p ripple	-	75	-	dB
		fin = 20kHz, 200mVp-p ripple	-	70	-	dB

TYPICAL PERFORMANCE CURVES

The following typical performance curves are generated using an ESS' evaluation board. The internal charge pump is used to supply the negative rail. Measurements are taken using an Audio Precision Audio Analyzer.

Note that all measurements in the graphs include errors due to the test equipment plus those of the ES9018K2M DAC on the evaluation board. Although these errors are very low, they are significant when measuring a state-of-the-art headphone amplifier like the ES9601C. Therefore the parametric values shown in the characteristic curves are slightly degraded compared to the values in the tables as the latter are calculated from measurements in near-ideal conditions.

TYPICAL PERFORMANCE CURVES

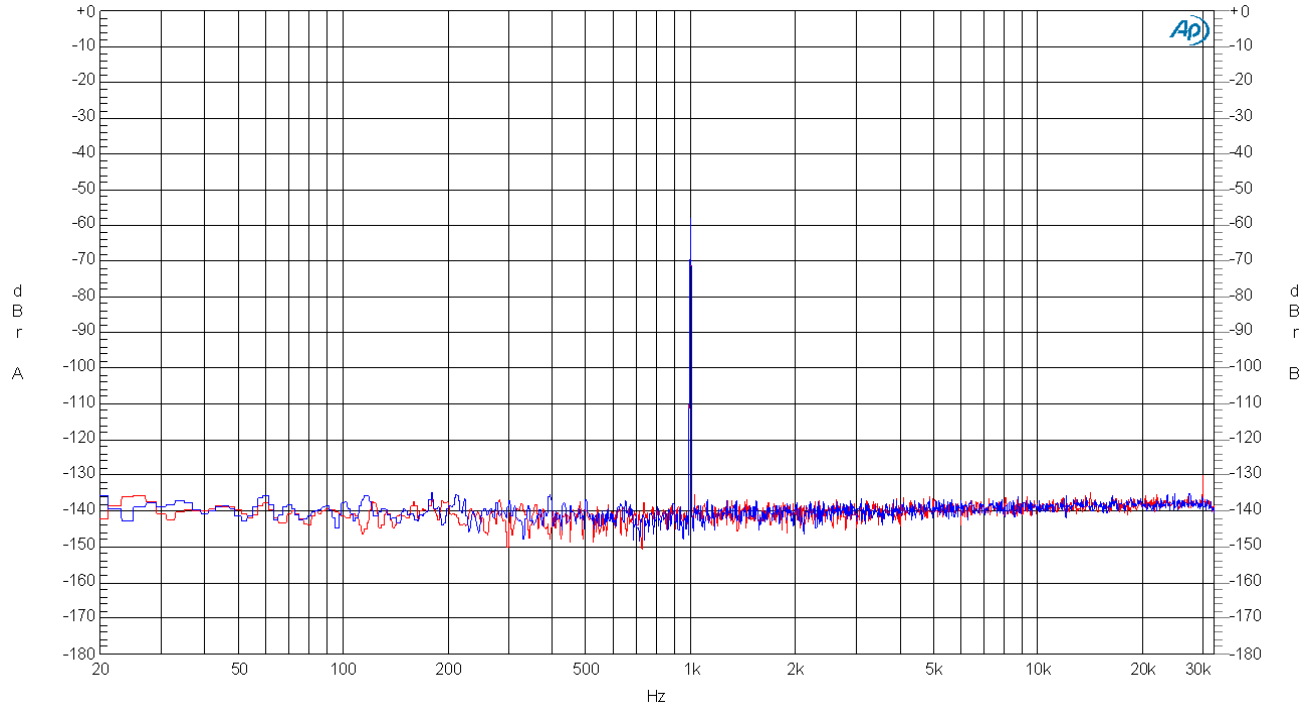


Figure 3. DNR FFT, 1kHz @ -60dB, Single-Ended, 32Ω Load

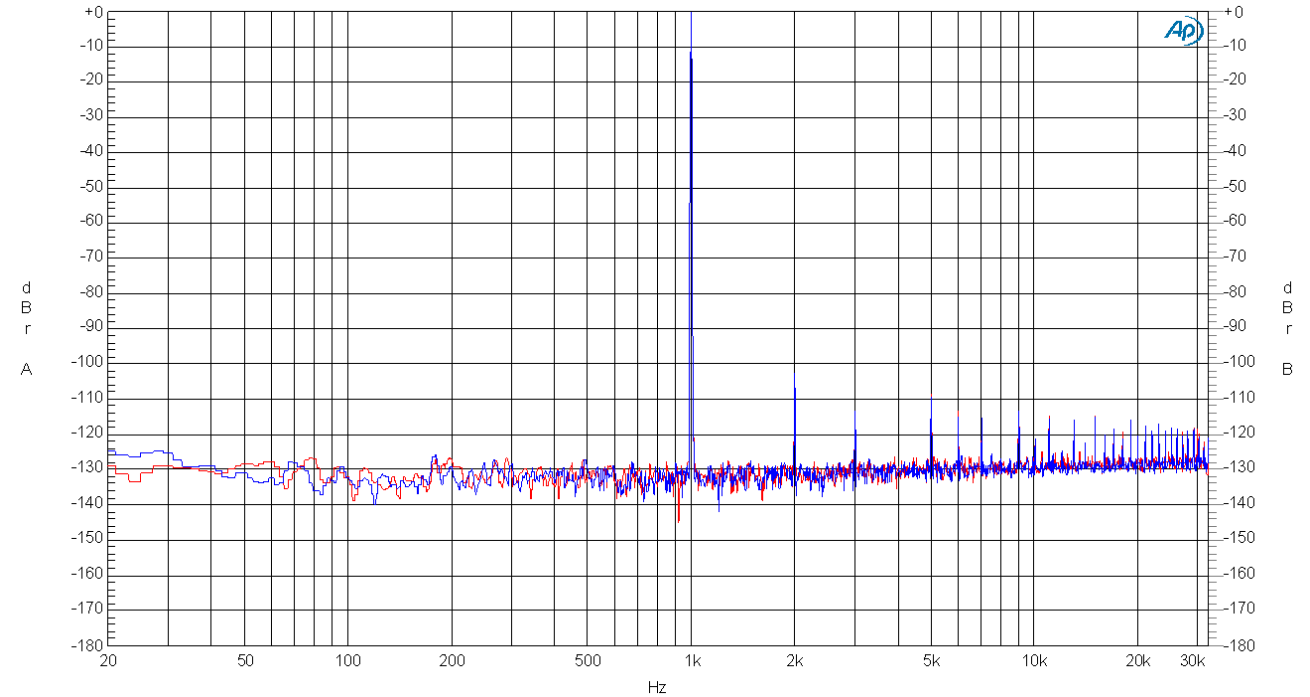


Figure 4. THD+N FFT, 1kHz @ 0dB, Single-Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

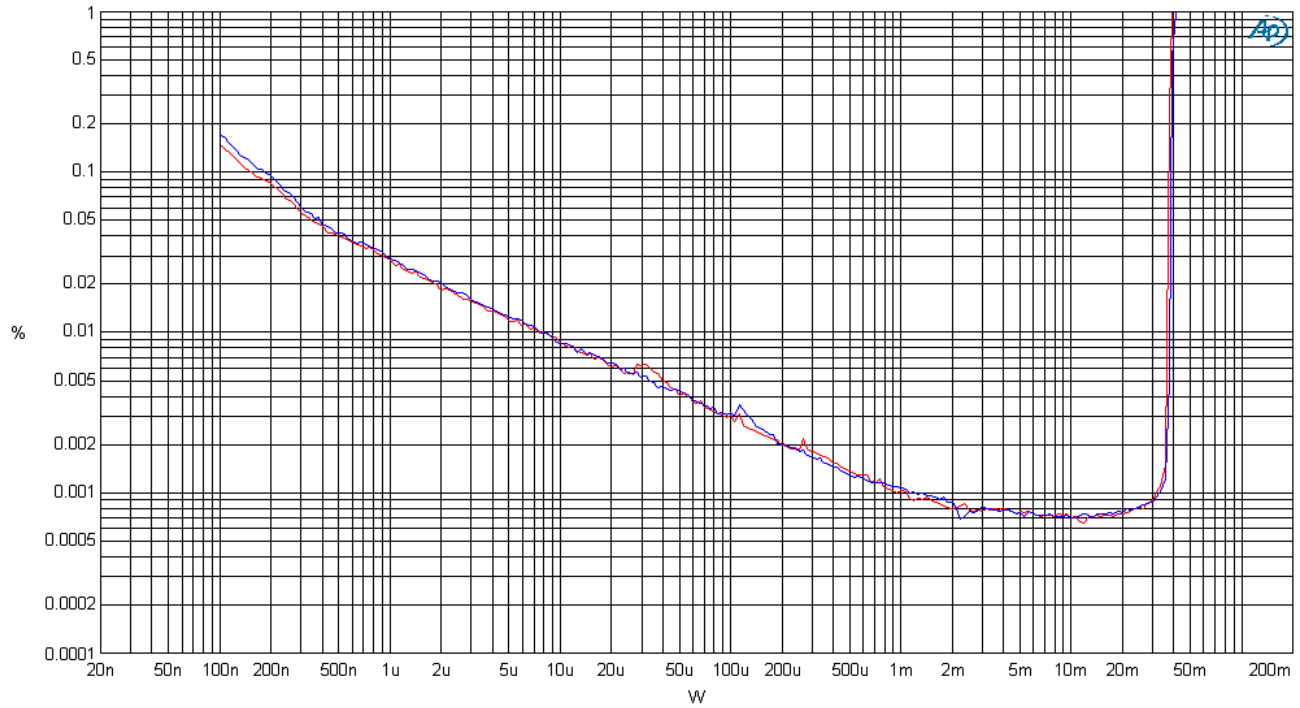


Figure 5. THD+N Unweighted vs. Output Power, Dual Channel Drive, Single Ended, 32Ω Load

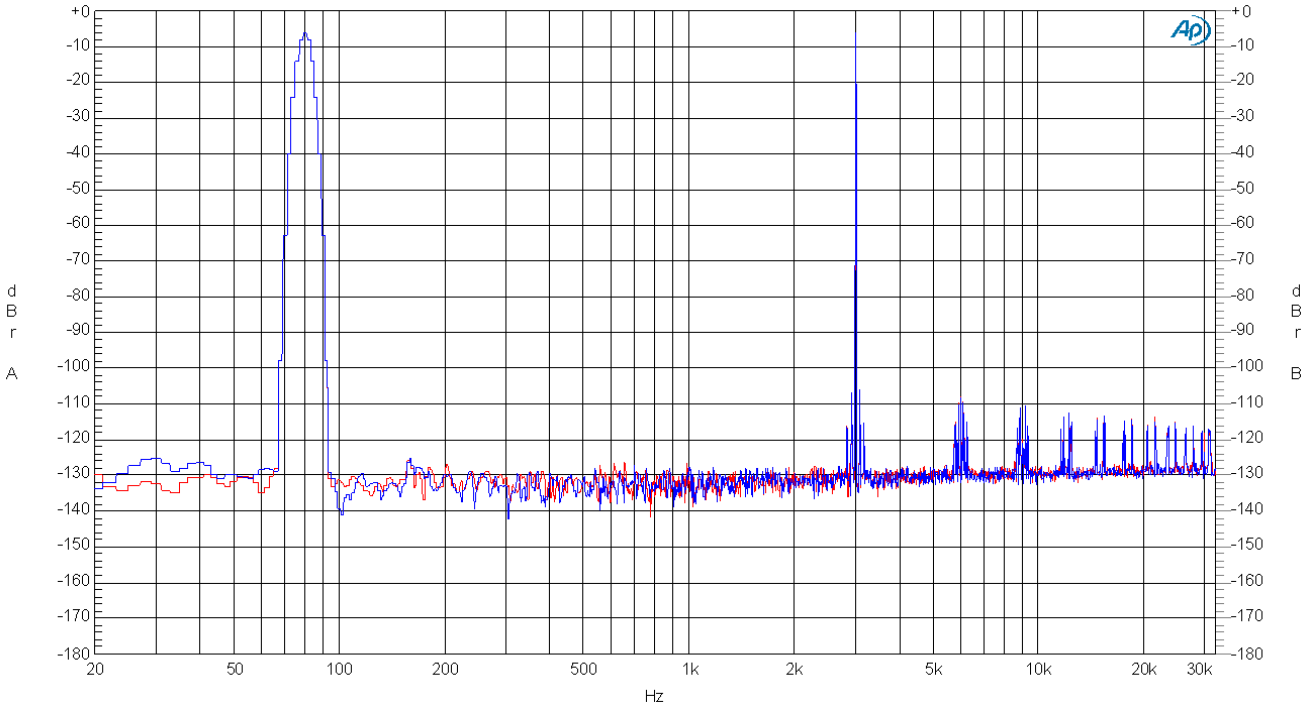


Figure 6. IMD FFT, 3kHz & 80Hz @ SMPTE 1:1, Single Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

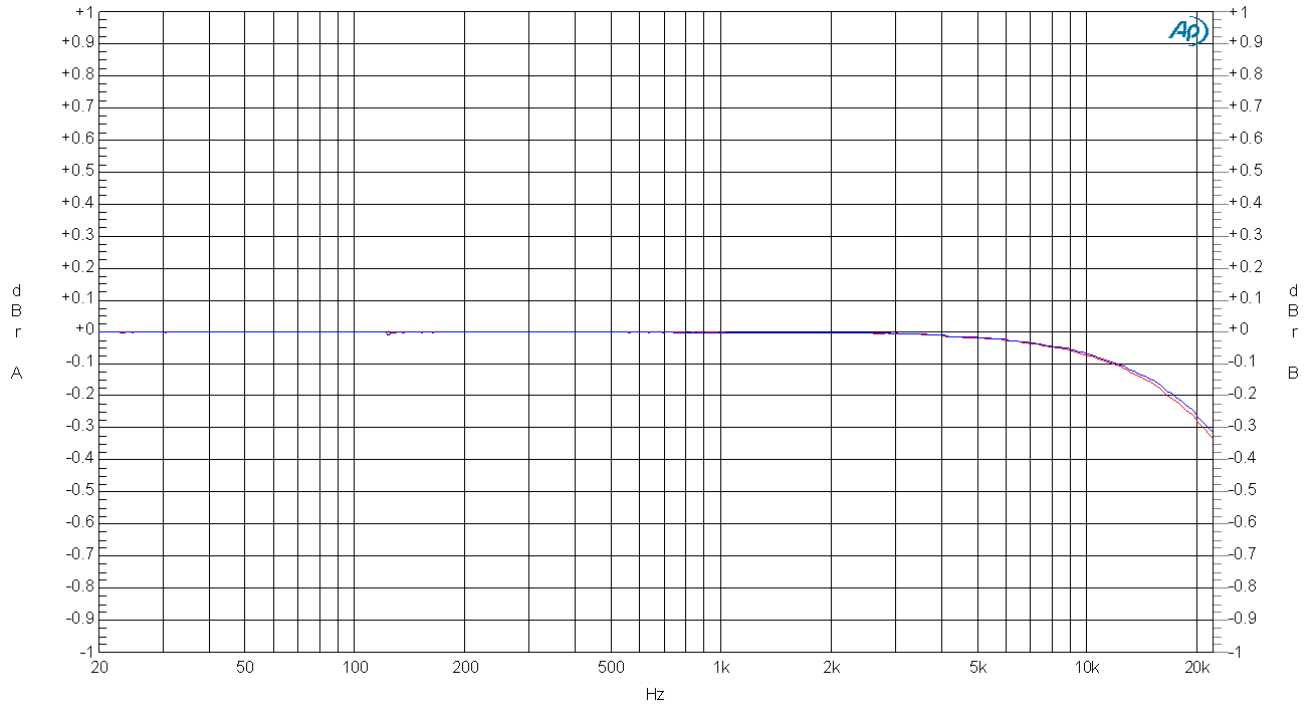


Figure 7. Frequency Response, 20Hz to 22kHz @ 0dB, Log Scale, Single Ended, 32Ω Load

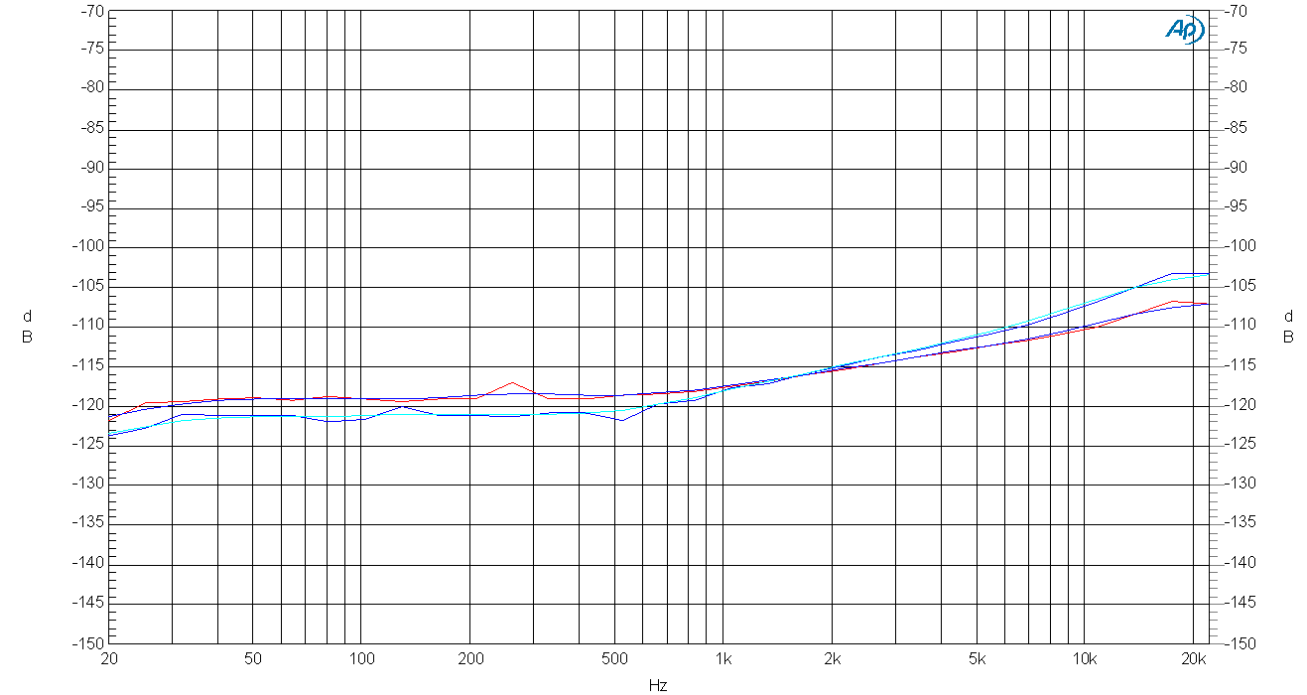


Figure 8. Crosstalk vs. Frequency, Single Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

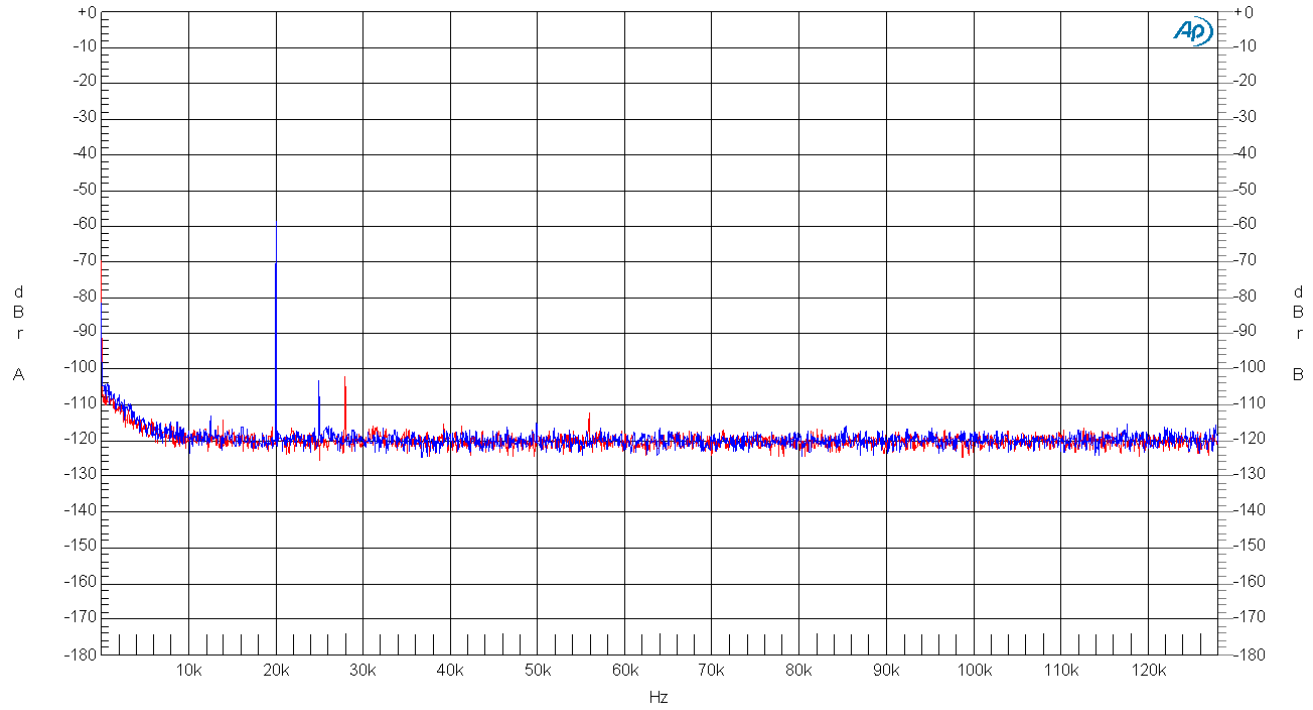


Figure 9. Wideband FFT, 20kHz @ –60dB, Single Ended, 32Ω Load

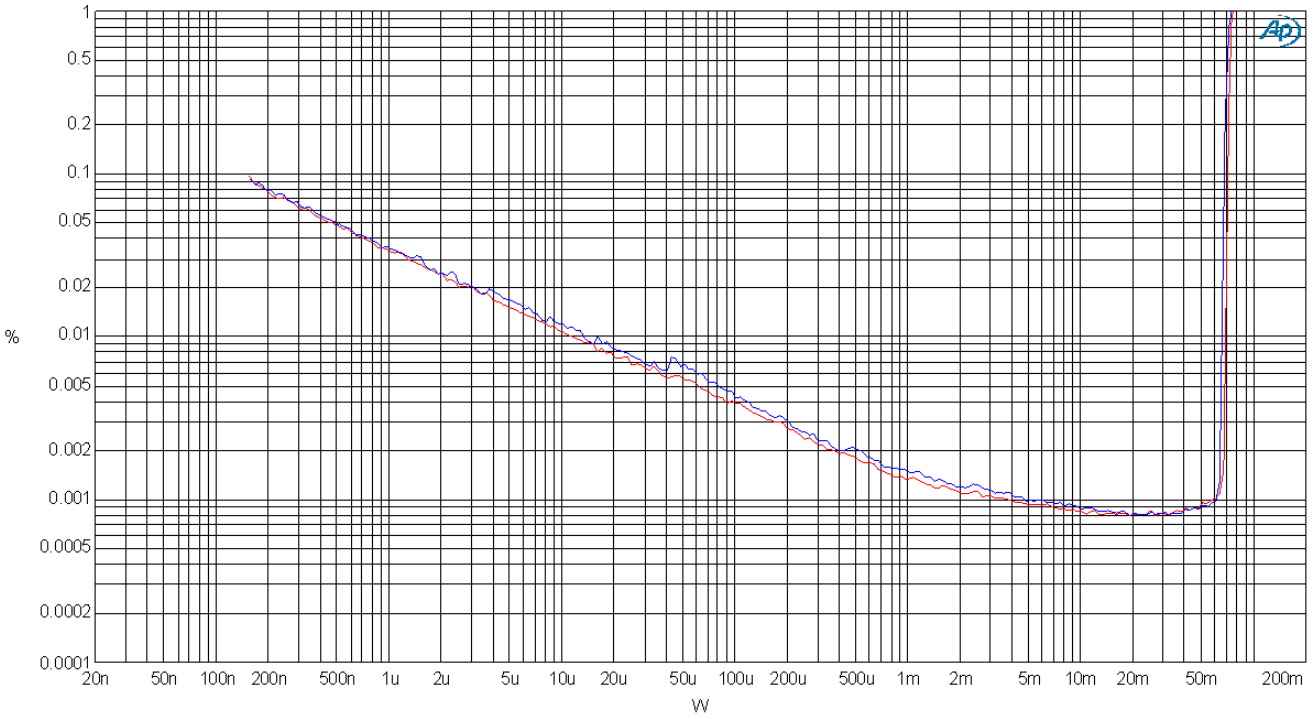


Figure 10. THD+N Unweighted vs. Output Power, Dual Channel Drive, Single Ended, 16Ω Load, external –3.3V supply

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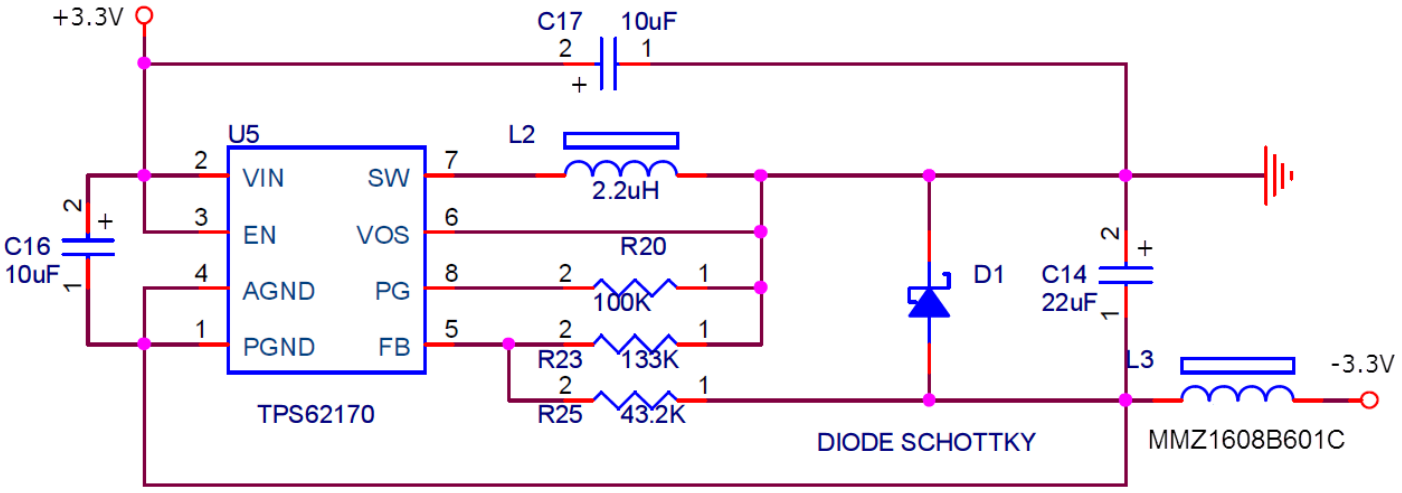
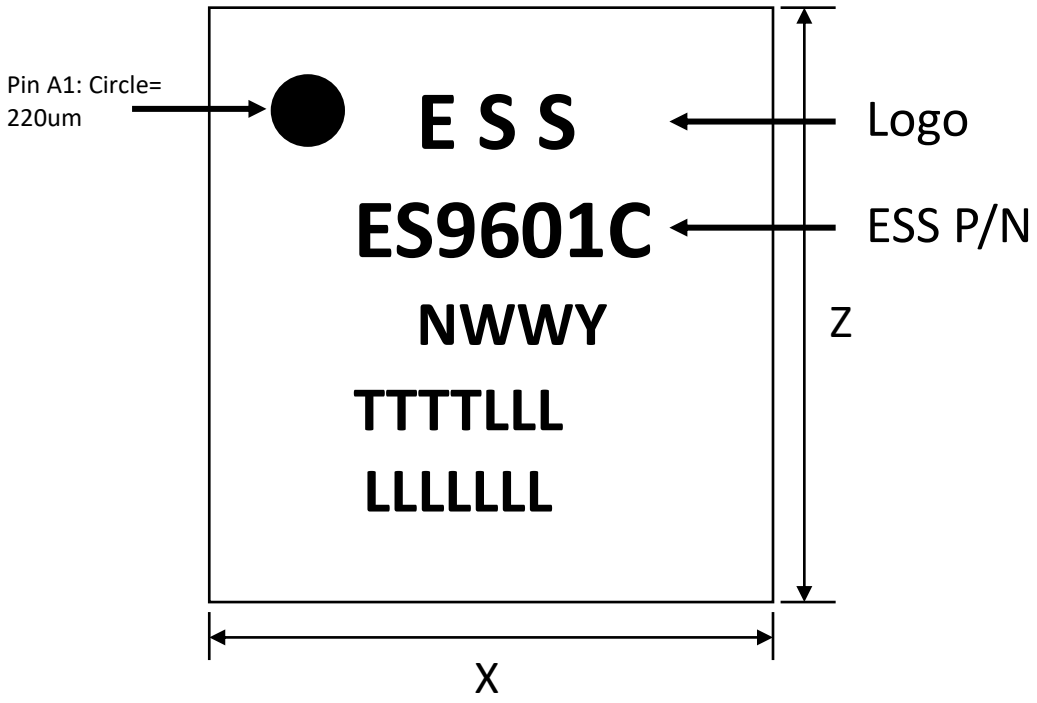


Figure 11. External –3.3V supply providing up to 500mA. Capacitors must be low-ESR ceramic or electrolytic.

16-Pin CSP Top View

16-Ball CSP Top View Marking

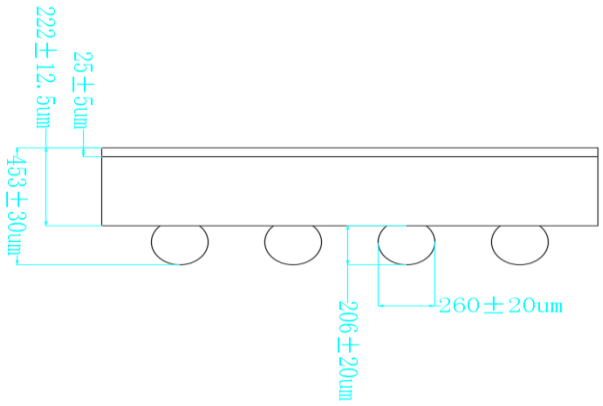


Top Center (0,0) = Package Center

T	*Tracking number*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*
N	*Silicon Revision*

Marking is subject to change. This drawing is not to scale.

16-Pin CSP Mechanical Dimensions



Side View

Parameter	Min	Normal	Max
	Millimeters		
Package body dimension X	1.7888	1.8188	1.8488
Package body dimension Z	1.7938	1.8238	1.8538
Package Height	0.423	0.453	0.483
SI thickness	0.2095	0.222	0.234.5
Bump Height (C1)	0.186	0.206	0.226
Bump Diameter	0.24	0.26	0.28
Total Ball Count Per Die	/	16	/
Ball Pitch X axis (min)	/	0.4	/
Ball Pitch Y axis (min)	/	0.4	/

Table 1. Package Dimensions

Position	Ball Name	X	Y
A1	PDB	–600	–600
A2	INR	–200	–600
A3	INBR	200	–600
A4	OUTR	600	–600
B1	AGND_CP	–600	–200
B2	C2	–200	–200
B3	ANEG	200	–200
B4	PNEG	600	–200
C1	C1	–600	200
C2	AVCC_CP	–200	200
C3	AVCC	200	200
C4	AGND	600	200
D1	OSC	–600	600
D2	INL	–200	600
D3	INBL	200	600
D4	OUTL	600	600

Ball center coordinates are measured from the BGA VIEW center (0,0)

Table 2. Ball Positioning

16-Pin CSP Mechanical Dimensions

Ball Matrix	1	2	3	4
A	PDB	INR	INBR	OUTR
B	AGND_CP	C2	ANEG	PNEG
C	C1	AVCC_CP	AVCC	AGND
D	OSC	INL	INBL	OUTL

Table 3. Ball Matrix

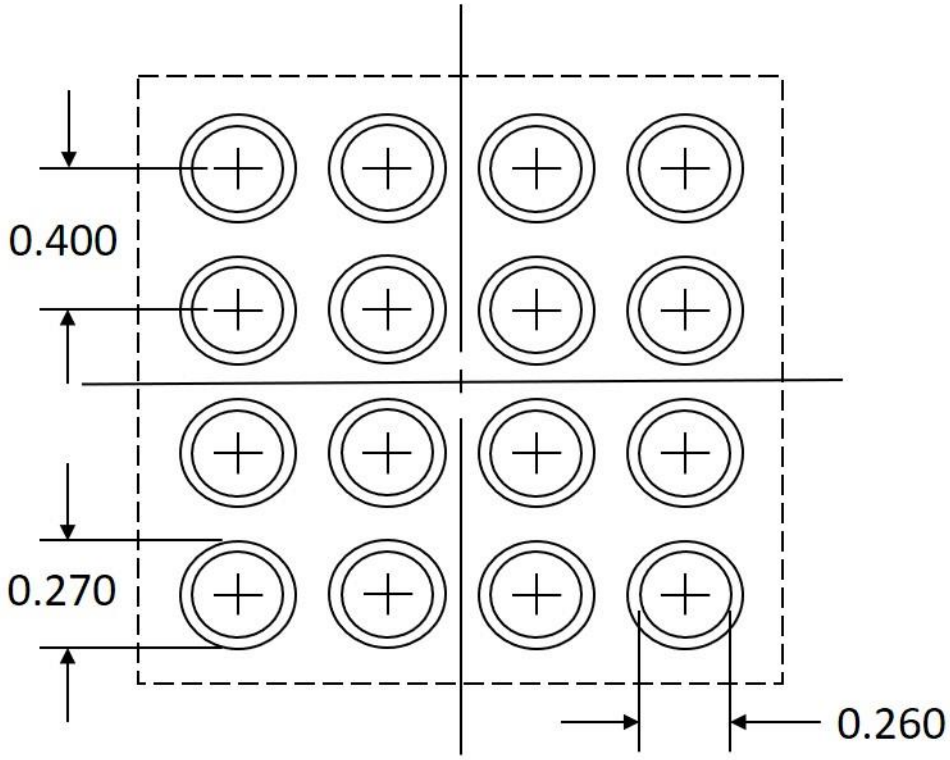
Notch Orientation	Up	Down	Right	Left	Other
		X			

Table 4. Package Orientation

Package Marking Information

1. Marking to be center on package
2. Lines 1 and 3 to be center justified
3. Lines 4 to 5 to be left hand justified
4. Pin A1 location is at the top left corner: Circle = 220µm
5. Font type: Arial
6. Character height: 220µm

Example 16-Ball CSP Land Pattern



Notes:

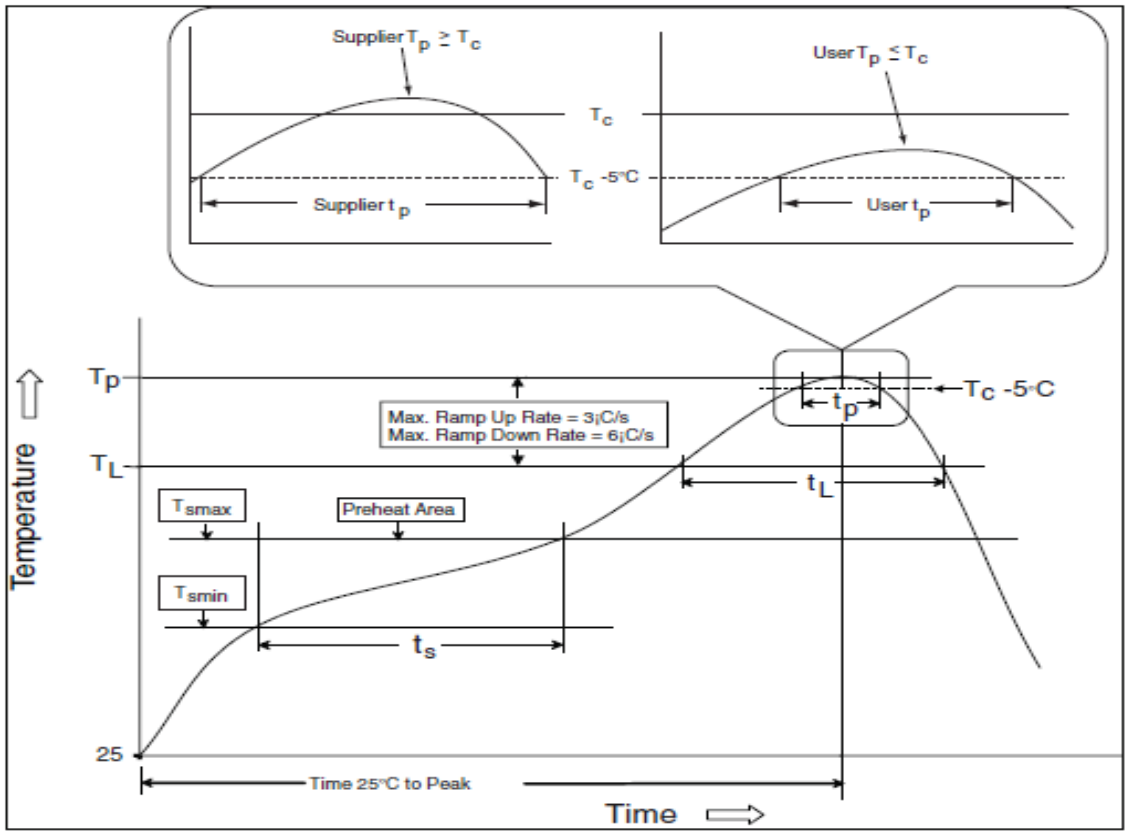
1. All dimensions are in millimeters unless specified otherwise.
2. Thermal vias should be 0.3mm to 0.33mm in diameter, with the barrel plated to 1oz copper.
3. For maximum solder mask in the corners, round the inner corners of each row.
4. For applications where solder loss through vias is a concern, plugging or tenting of the vias should be used. The solder mask diameter for each via should be 0.1mm larger than the via diameter.
5. Drawing is not to scale.

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.
Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:
Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ORDERING INFORMATION

Part Number	Description	Package
ES9601C	SABRE Headphone Amplifier	16-pin CSP

The letter C identifies the package type CSP

Revision History

Rev.	Date	Notes
0.1	July 07, 2014	Initial release
0.2	July 09, 2014	Added 4.7Ω output protection resistors to the simplified schematic of Figure 2, and “external –3.3V supply” is added to the description of Figure 9.
0.3	July 24, 2014	Updated CSP diagrams: BGA view, Top view, Side view, and Table 1.
0.4	August 8, 2014	Removed inch dimensions from Table 1
0.5	August 18, 2014	Ball callouts changed to follow CSP convention. Locations and functions of the solder balls have not changed so existing PCB layouts are NOT affected.
0.6	September 16, 2014	Added I_B and V_{OS} specifications
0.7	September 26, 2014	Added specifications to the Absolute Maximum Ratings table. Updated Figure 1 block diagram to more accurately represent the internal circuit.
0.8	September 30, 2014	Ball dimension changed from 0.25mm to 0.200mm diameter.
0.9	December 12, 2014	Updated application circuit diagram. THD+N conditions changed with 32Ω load impedance.
0.91	May 8, 2015	Added SABRE HiFi Logo. Updated ESS’ contact information.
0.92	March 7, 2019	Changed SABRE9601C to ES9601C. Updated SABRE® and SABRE SOUND®
1.0	April 2, 2019	Update package dimensions and top view marking.
1.1	April 18, 2019	Added 16-CSP Land Pattern