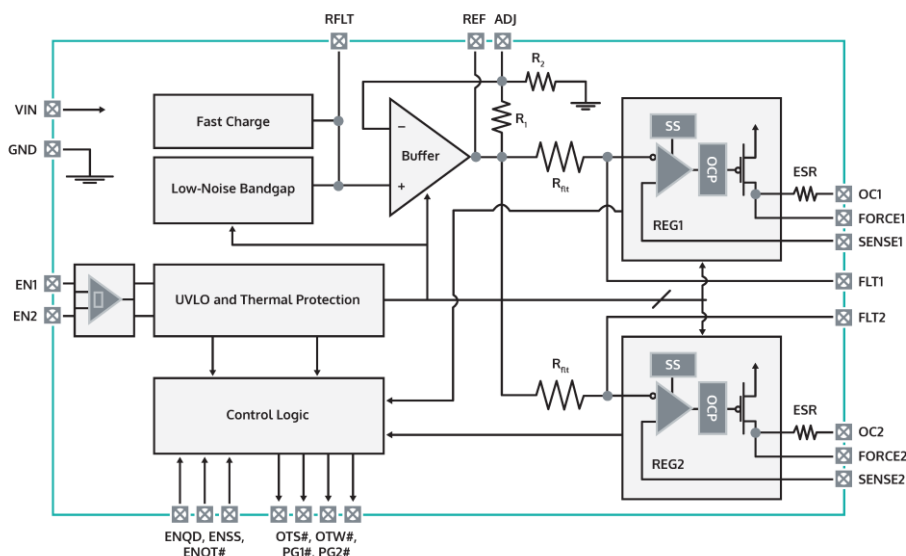**Analog Reinvented**

The **ES9311Q Dual, Ultra-Low Noise Linear Regulator** is the industry's highest-performance, ultra-low noise regulator optimized to supply the reference voltages for ESS' 32-Bit SABRE DACs and ADCs. Audio DACs require a very low-noise reference voltage to achieve high dynamic range (DNR). The ES9311's output noise is typically under 1µVrms from 100Hz to 100kHz, and less than 1.3µVrms from 10Hz to 100kHz. The temperature coefficient of each voltage output is typically 50ppm/°C. The dual regulator replaces three active devices and several discrete components used previously to produce a high-performance, low-noise regulator. The ES9311Q enables ESS' Flagship 8-Channel DAC, the ES9038PRO, to achieve its full 140dB DNR and is an ideal low-noise regulator for use with all ESS' 32-Bit SABRE® DACs.

The ES9311Q provides several unique features not available in commodity regulators: the two outputs require no decoupling capacitors, remote load sensing ensures output voltage accuracy right at the load, there are two output enable inputs, the outputs have a soft-start function, plus power-good, over-temperature warning, and over-temperature shutdown outputs.

The ES9311Q Dual, Ultra-Low Noise Linear Regulator is available in a 30-pin, 3mm x 5mm QFN package.
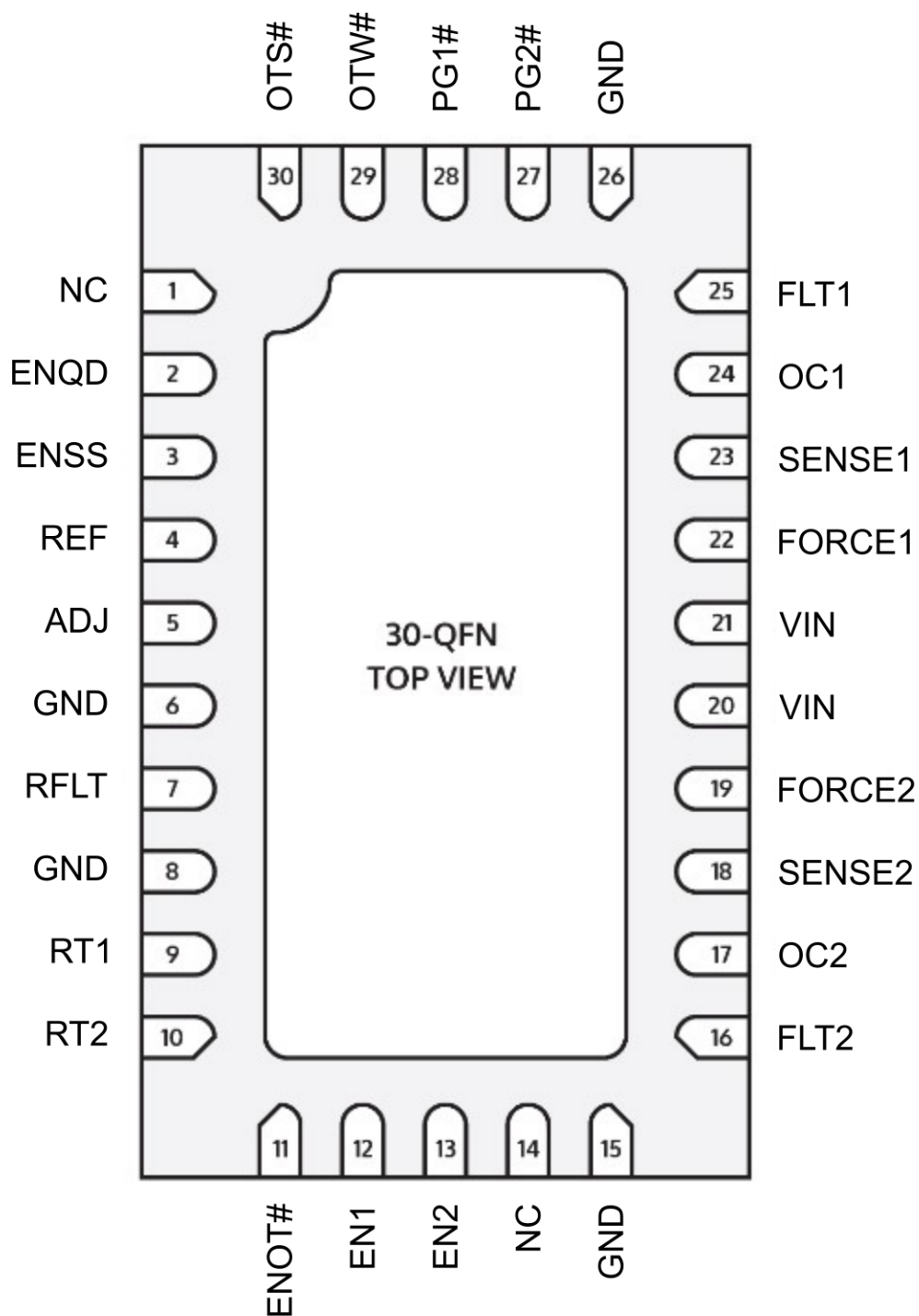
FEATURE	BENEFIT
o Dual outputs with 300mA total load	o Dual regulator minimizes board space requirements
o < 1µVrms output noise (100Hz to 100kHz)	o Low noise is required to achieve high converter DNR
o Operating from +3.5V to +5.5V	o Wide supply range operation
o Excellent line and load regulation	o Maintains accurate Vout with line/load variations
o Remote sensing for each output	o Enables excellent load regulation, typically 16mV/A
o Five enable inputs and four status outputs	o Provides design flexibility and host communications
o Over-current & over-temperature protection	o Protects regulator against system fault conditions
o 3.5mA total quiescent current	o Suitable for USB and battery powered designs
o 30-QFN package, 3mm x 5mm	o Minimizes PCB footprint

ES9311Q Dual, Ultra-Low Noise Linear Regulator

PIN LAYOUT

30-QFN
TOP VIEW

Top pins (left to right): 30 OTS#, 29 OTW#, 28 PG1#, 27 PG2#, 26 GND

Left pins (top to bottom):
1 NC
2 ENQD
3 ENSS
4 REF
5 ADJ
6 GND
7 RFLT
8 GND
9 RT1
10 RT2

Right pins (top to bottom):
25 FLT1
24 OC1
23 SENSE1
22 FORCE1
21 VIN
20 VIN
19 FORCE2
18 SENSE2
17 OC2
16 FLT2

Bottom pins (left to right): 11 ENOT#, 12 EN1, 13 EN2, 14 NC, 15 GND

ES9311Q Dual, Ultra-Low Noise Linear Regulator

PIN DESCRIPTIONS

Pin	Name	Pin Type	Pin Description
1	NC	-	No internal connection, pin may be grounded or left floating
2	ENQD	Input	Enable for Quick Discharge function, internal pull-up
3	ENSS	Input	Enable for Soft-Start function, internal pull-up
4	REF	Output	Low-noise bandgap reference output voltage
5	ADJ	Input	Input for fine adjustment of bandgap voltage output
6	GND	Ground	Ground
7	RFLT	Output	Connection for noise-bypass capacitor on bandgap reference
8	GND	Ground	Ground
9	RT1	I/O	Reserved, Connect to ground for normal operation
10	RT2	I/O	Reserved, Connect to ground for normal operation
11	ENOT#	Input	Enable for Over Temperature functions. Active low
12	EN1	Input	Enable for Output 1. Connect to VIN for automatic startup
13	EN2	Input	Enable for Output 2. Connect to VIN for automatic startup
14	NC	-	No internal connection, pin may be grounded or left floating
15	GND	Ground	Ground
16	FLT2	Output	Connection for noise-bypass capacitor on output 2
17	OC2	Output	Optional output capacitor connection
18	SENSE2	Input	Output 2 Sense
19	FORCE2	Output	Output 2 Force
20	VIN	Power	Regulator supply
21	VIN	Power	Regulator supply
22	FORCE1	Output	Output 1 Force
23	SENSE1	Input	Output 1 Sense
24	OC1	Output	Optional output capacitor connection
25	FLT1	Output	Connection for noise-bypass capacitor on output 1
26	GND	Ground	Ground
27	PG2#	Output	Power Good Output 2. Active low, open-drain
28	PG1#	Output	Power Good Output 1. Active low, open-drain
29	OTW#	Output	Over-Temperature Warning output. Active low, open-drain
30	OTS#	Output	Over-Temperature Shutdown output. Active low, open-drain
-	Exposed Pad	Ground	Connect exposed pad to Ground

ES9311Q Dual, Ultra-Low Noise Linear Regulator

FUNCTIONAL DESCRIPTION

The ES9311 is a dual, ultra-low noise voltage, low dropout (LDO) regulator designed for applications that require two stable voltage outputs that can supply up to 150mA per channel. Output voltage noise is typically <1µVrms from 100Hz to 100kHz and excellent power supply rejection of 90dB from 100Hz to 25kHz make this dual reference ideal for audio data converters and PLL supplies. The voltage reference design combines the advantages of both series voltage and shunt voltage references in one. That means the design has a low quiescent current, as in the series voltage reference, combined with a low output impedance that is characteristic of the shunt voltage reference. The output impedance is low over the whole output current range. In addition, the circuit is designed to operate with no output decoupling capacitor hence reducing BOM cost and PCB area. High-performance regulator features such as, soft-start, under-voltage lockout, fast transient response, over-temperature shutdown, over-current protection, and power-good indicators are included for ease-of-use and device protection.

Dual Regulator Functional Blocks

The dual LDO regulator consists of: a low-noise bandgap reference with fast charge for the filter capacitor, reference buffer amplifier, two high-performance 150mA low-dropout regulators, protection circuitry against fault conditions, plus control logic and signaling. There are five Enable inputs, one for each regulated supply, plus ones for enabling soft-start, over-temperature protection, and quick-discharge of the output voltage. All the Enable inputs include Schmitt triggers to prevent signal "chatter" when the input is noisy. There are four, active-low status outputs: power-good1, power-good2, over-temperature warning, and over-temperature shutdown. Power-good signals are activated when the input voltage is above 3.0V and when the output exceeds 90% of final value. If any overload condition occurs, e.g. over-current or over-temperature, the power-good signal will disappear. The regulator outputs use Kelvin sensing, i.e. force and sense connections, to maximize the voltage accuracy and minimize voltage perturbations right at the DAC AVCC connections.

Input Supply

The E9311 operates from a single +3.5V to +5.5V supply and provides two outputs each capable of providing up to 150mA. Power Supply Rejection (PSR) is typically 90dB that extends beyond the audio frequency range, up to 25kHz. When powering the ES9311 from a switching power supply it is advisable to employ HF decoupling on the input to minimize noise that may mix down into the audio band. High frequency PSR can also be improved by increasing the value of the noise filtering capacitors from 1µF to 10µF and this is recommended for Audio DAC and ADC applications.

The ES9311 includes an Under-Voltage Lockout (UVLO) circuit that ensures the output voltage rises gracefully without glitches or false starts that might introduce audible clicks or noise.

Outputs & Remote Sensing

Output noise from each supply is typically under 1µVrms from 100Hz to 100kHz, and less than 1.3µVrms from 10Hz to 100kHz. The temperature coefficient of each output is typically 50ppm/°C with a drift of ±0.5% over temperature which corresponds to a DAC gain drift of ±0.05dB over temperature. Line and load regulation are typically 0.7mV/V and 16mV/A (16mΩ output resistance) respectively. Isolation between the two outputs, which might affect crosstalk between left and right channels, is over 120dB at 1kHz so the effect is negligible.

Remote sensing maintains an accurate voltage at the load, even at high load currents, despite voltage drops in the connecting copper track. Bench power supply remote sensing uses a 4-wire connection, or Kelvin connection, that separates the current path to and from the load from the voltage signal developed across the load. The 4-wire measurement bypasses the voltage drop in the connecting cables by providing a voltage signal that is fed back to high-impedance ground and output sense inputs. Slightly different from a bench power supply, the ES9311 dual regulator relies on a low-impedance ground plane for the current return path and only uses remote sensing for the output connections as these tracks drop the most voltage. This 3-wire scheme maximizes load regulation in conjunction with a low-impedance ground plane.

Output Noise Reduction

The ES9311 requires three 1µF noise filter capacitors, CRF, CF1, and CF2 to achieve its low-noise performance. These capacitors should be low-leakage ceramic types with low-ESR and temperature rated for operation up to the maximum internal operating temperature of the end product. Dielectric types X7R or X5R are highly recommended for these capacitors. Higher values of noise filter capacitor can be used to increase high frequency PSR, e.g. 10µF, and this value and is recommended for the highest performance Audio applications. A fast-charge circuit that rapidly charges the noise bypass capacitor CRF minimizes startup time.

ES9311Q Dual, Ultra-Low Noise Linear Regulator

Input & Output Decoupling

The ES9311 requires one 4.7µF input decoupling capacitor, but NO output decoupling capacitors are required. Adding large decoupling capacitors directly to the outputs may cause instability and will degrade the performance of the regulators. A small amount of load capacitance is unavoidable, but if this exceeds 1nF then a 1µF should be connected between COUT and ground (see Figure 2). Also, if high load step-currents are anticipated, e.g. 1mA to 50mA, then 1µF capacitors should be connected between COUT1 and COUT2 and ground to improve load transient response. These capacitors are unnecessary in audio DAC and ADC applications as the load current is relatively constant, that is unless load capacitance exceeds 1nF.

Output Adjustment

The ES9311Q was designed to provide an adjustable output voltage ranging from +2.5V to VIN-0.2V. External resistors or a potentiometer may be used to adjust the output voltage to the desired values. The regulated output voltage, however, can be changed if desired. These adjustments are optional if +3.3V is desired.

Voltage adjustment is made using the ADJ input. To change the output voltage, one or two resistors, **R_5**, **R_7**, can be added as shown in Figure 12. Adding **R_5** and **R_7** will create parallel resistances with the internal gain setting resistors of 3.6045 kΩ and 10 kΩ respectively. The equation for setting output voltage is as follows:

$$V_{OUT} = 2.42 \left(1 + \left(\frac{3.6045 \text{ k}\Omega \text{ || } R_5}{10 \text{ k}\Omega \text{ || } R_7}\right)\right)$$

While it is possible to use this adjustment to operate the ES9311Q with an output voltage below its design point of 3.3 V, the "power good" outputs are designed to activate when the output voltage exceeds a level of approximately 3.0 V, and will not indicate correctly if an output at or below that level is selected. Furthermore, the performance of the device is only specified with a nominal 3.3 V output.

Overload Protection

Each output has over-current protection, set at ~250mA, and the regulator includes an over-temperature warning output, and an over-temperature shutdown output. The regulator outputs can be shorted to ground indefinitely but this is not recommended as the temperature cycling may reduce product longevity. Thermal-overload protection limits the total power dissipation in the ES9311Q. The over-temperature shutdown function can be disabled for high-availability systems using the ENOT# enable input. The over-temperature warning (OTW#) output is activated when the junction temperature reaches +105°C and turns off when the junction temperature drops below +100°C. The OTW output may be used to activate a system cooling-fan or notify the host processor of an impending thermal shutdown. Over-Temperature Shutdown (OTS) is activated at +130°C and is designed to protect the ES9311Q in the event of a fault condition. OTS has 15°C of hysteresis preventing the regulator from restarting automatically until the junction temperature drops below +115°C. Under continuous output fault conditions, the regulator outputs will switch ON and OFF as the device alternately cools and then reheats. Disabling the OTS function permits the junction temperature to exceed +130°C so be careful not to exceed the absolute maximum junction temperature rating of +150°C as this can impact the device's reliability.

Power Dissipation

The ES9311's maximum power dissipation depends on the thermal resistance of the case and PCB, the temperature difference between the die's junction temperature and the ambient temperature, and the airflow around the regulator. The power dissipated in the regulator is calculated from:
P = Iavcc1 x (Vin – AVCC1) + Iavcc2 x (Vin – AVCC2) + Vin x Iq
The maximum power dissipation is: Pmax = (Tj - Ta) / (Θj-c + Θc-a)
Where Tj - Ta is the temperature difference between the ES9311 junction temperature and the ambient temperature, Θjc is the thermal resistance from junction to case, and Θca is the thermal resistance from the case through the PC board, copper traces, and other materials to ambient.

ES9311Q Dual, Ultra-Low Noise Linear Regulator
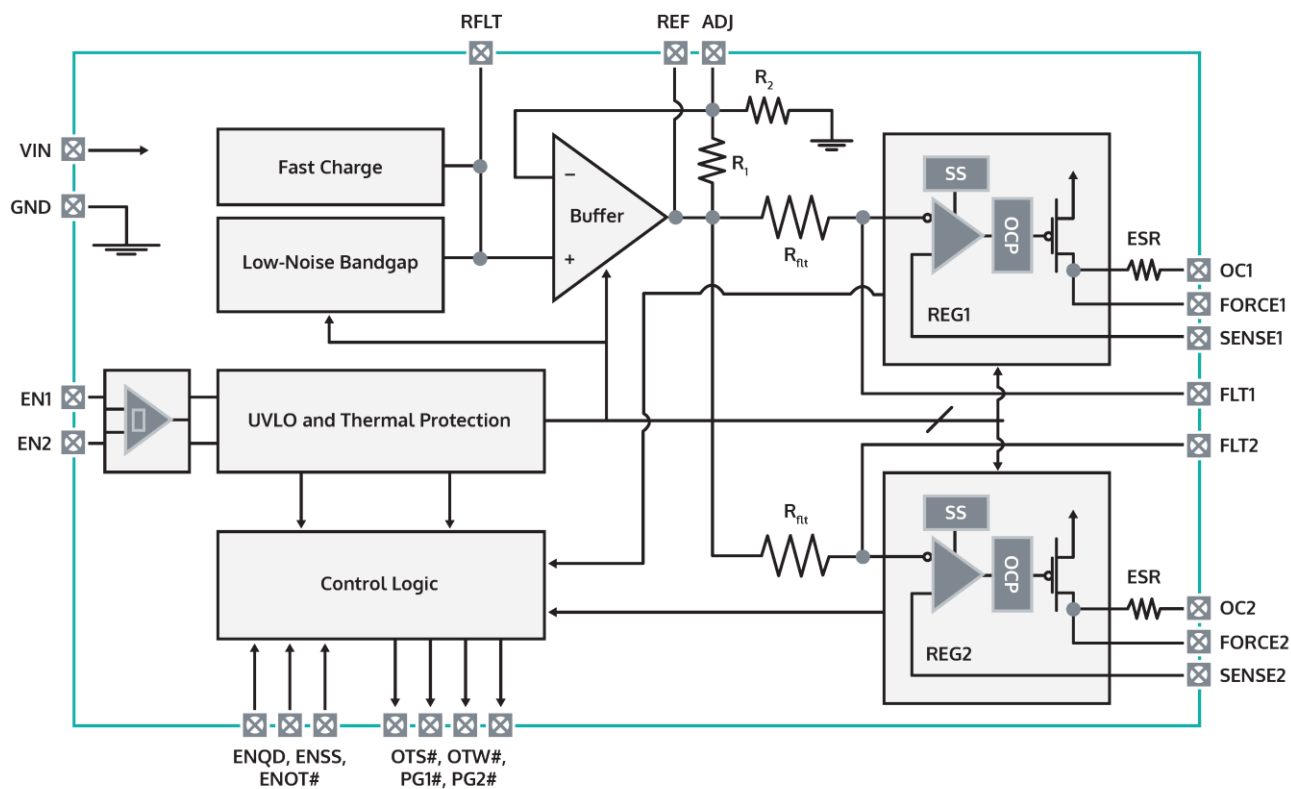
ES9311Q Block Diagram

Figure 1. Block Diagram of the ES9311Q Dual, Ultra-Low Noise Linear Regulator.

ES9311Q Dual, Ultra-Low Noise Linear Regulator
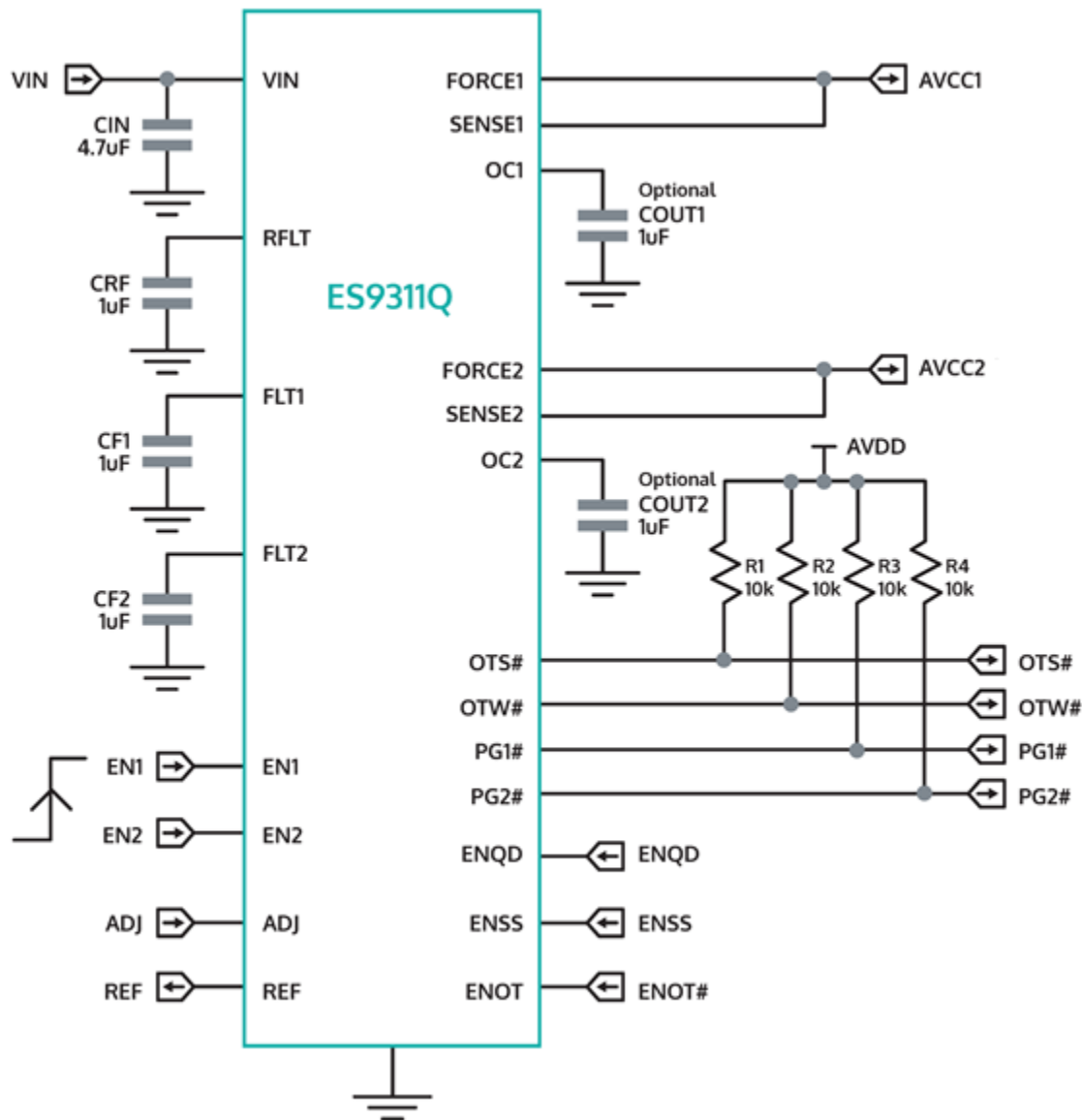
APPLICATION DIAGRAM

Figure 2. Simplified ES9311Q Application Circuit.

ES9311Q Dual, Ultra-Low Noise Linear Regulator

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Power Supply Voltage	+6.0V with respect to GND
Storage temperature	−65°C to +150°C
Operating Junction Temperature	+125°C
Thermal Impedance, Θ_{J-A}	46°C/W
Thermal Impedance, Θ_{J-C}	5°C/W
Voltage range for digital input pins	−0.3V to VIN + 0.3V

ESD Protection
    Human Body Model (HBM)
    Machine Model (MM)
	
	2000V
	200V

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature Range	T_a	−25°C to +85°C

Power Supply	Symbol	Voltage	Quiescent Current (Note 1)	Standby Current (Note 2)
Analog power supply voltage	VIN	+3.5V to +5.5V	3.5mA typical	<10μA typical

Notes

   1) Quiescent current with both channels enabled, no output load, nominal +5V supply
   2) Both outputs are disabled

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High-level input voltage	ENH	0.8			V
Low-level input voltage	ENL			0.4	V
Hysteresis			200		mV

ES9311Q Dual, Ultra-Low Noise Linear Regulator

ANALOG PERFORMANCE

Test Conditions

1. VIN = Vout + 0.5V, EN = VIN; Iload = 10mA; CIN = 4.7µF; CRF = CF1 = CF2 = 1µF; Tj = Ta = 25°C for typical specs
2. Tj = −25°C to +85°C for minimum and maximum specifications, unless otherwise noted.
3. Without external adjustment resistors R5/R7 in Figure 12.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Input Voltage Range	VIN		3.5		5.5	V
Quiescent Current	Iq	Iload = 0µA. Iq is for both regulators		3.5	4	mA
		Iload = 150mA. Iq is for both regulators		4.5		mA
Shutdown Current	Isd	EN1 = EN2 = GND		1	10	µA
Power Supply Rejection	PSR	100Hz to 25kHz, Iout = 1mA to 150mA		90		dB
Noise						
Output Noise	en	100Hz to 100kHz		0.76		µVrms
	en	10Hz to 100kHz		1.3		µVrms
Noise Spectral Density		10kHz		2.3		nV/√Hz
Output						
Output Voltage	Vout	Iload = 10 mA, Tj = +25°C	3.27	3.30	3.33	V
Output Voltage Range [1]	Vout	Iload = 10 mA, Tj = +25°C	2.5		VIN-0.2	V
Temperature coefficient	VoutTC	Tj = −25°C to +85°C		50		ppm/°C
Load Current	Iload	Maximum output for each supply	0		150	mA
Short-circuit current	Isc	Current for each supply		270		mA
Start-up Time from Enable	Tsu	Soft-Start enabled				ms
Start-up Time from Enable	Tsu	Soft-Start disabled				ms
Shut-down Time for Vout	Tsd	Cload = 1µF, Quick-Discharge disabled				ms
Shut-down Time for Vout	Tsd	Cload = 1µF, Quick-Discharge enabled				ms
Regulation						
Line Regulation	ΔVout / ΔVIN	VIN = Vout + 0.5V to 5.5V		0.7		mV/V
Load Regulation	ΔVout / ΔIout	Iout = 1mA to 150mA		16		mV/A
Dropout Voltage	Vdropout	Iout = 10mA		50		mV
	Vdropout	Iout = 150mA				mV
Thermal Protection						
Over-temperature Warning	OTW	Over-Temperature Enabled, Tj rising		105		°C
Hysteresis		Over-Temperature Enabled		5		°C
Over-temperature Shutdown	OTS	Over-Temperature Enabled, Tj rising		130		°C
Hysteresis		Over-Temperature Enabled		15		°C
Under-Voltage Lock-Out						
VIN Rising	UVLO			3.00		V
VIN Falling						V
Hysteresis	UVLOhys					mV

Other Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Range [1]	Vout	Iload = 10 mA, Tj = +25°C	2.5		VIN-0.2	V

Note [1]: with the adjustment resistors R5/R7 in Figure 12.

ES9311Q Dual, Ultra-Low Noise Linear Regulator

TYPICAL PERFORMANCE CURVES

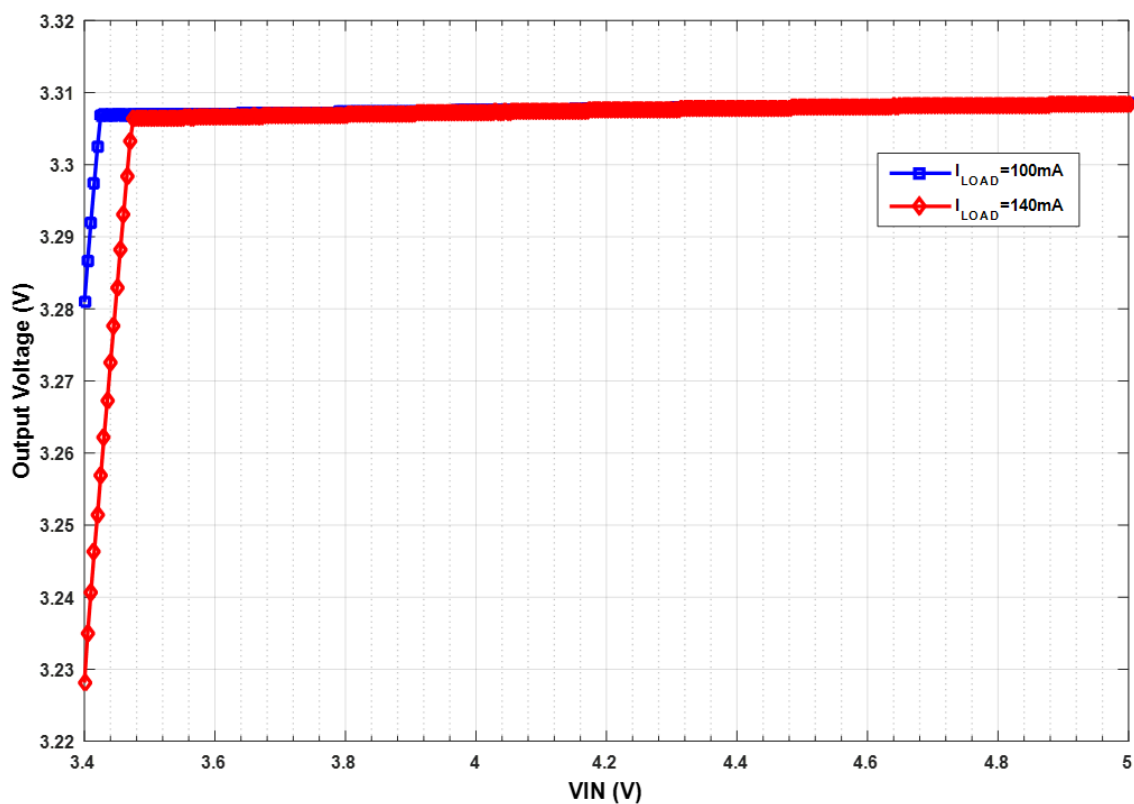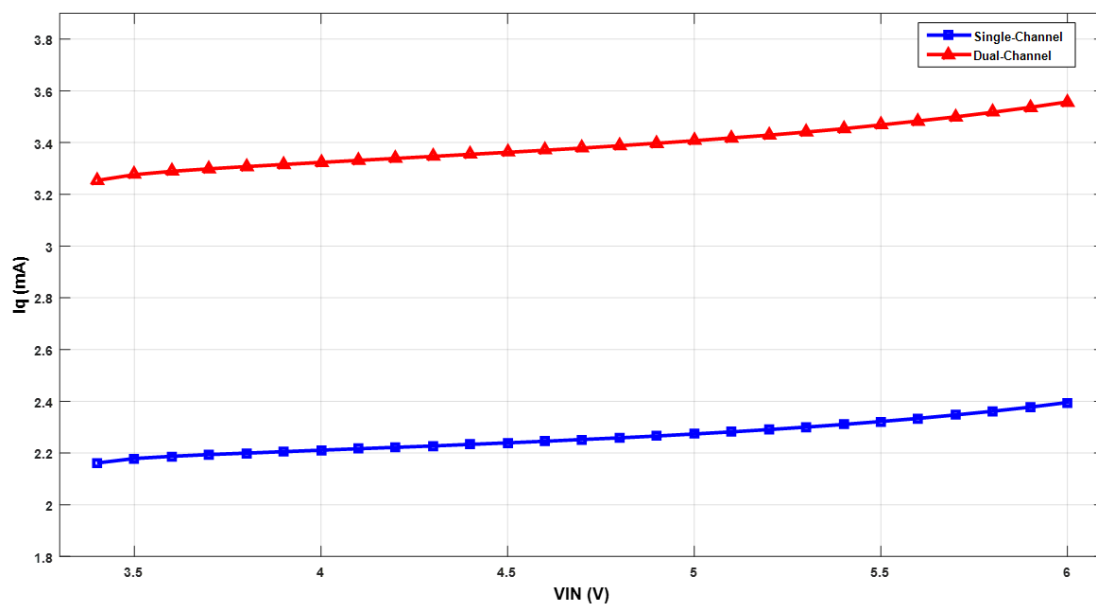Figure 3. Output Voltage vs. Input Voltage (Dropout)

Figure 4. Quiescent Current vs. Input Voltage

ES9311Q Dual, Ultra-Low Noise Linear Regulator
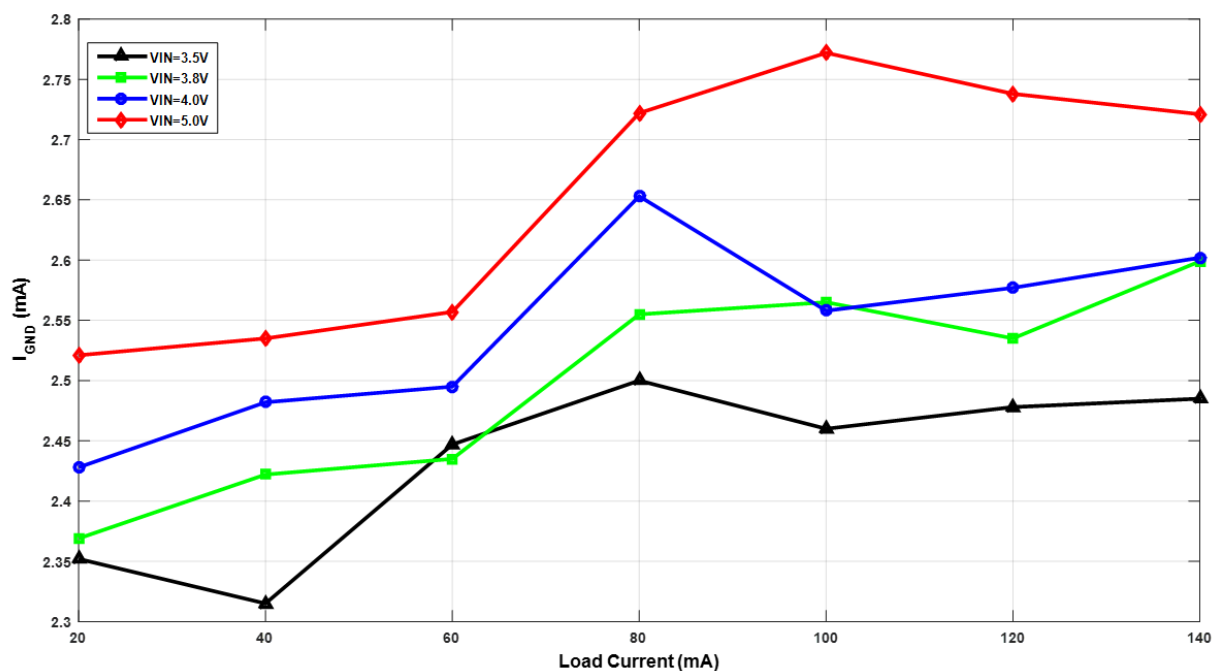
TYPICAL PERFORMANCE CURVES (continued)

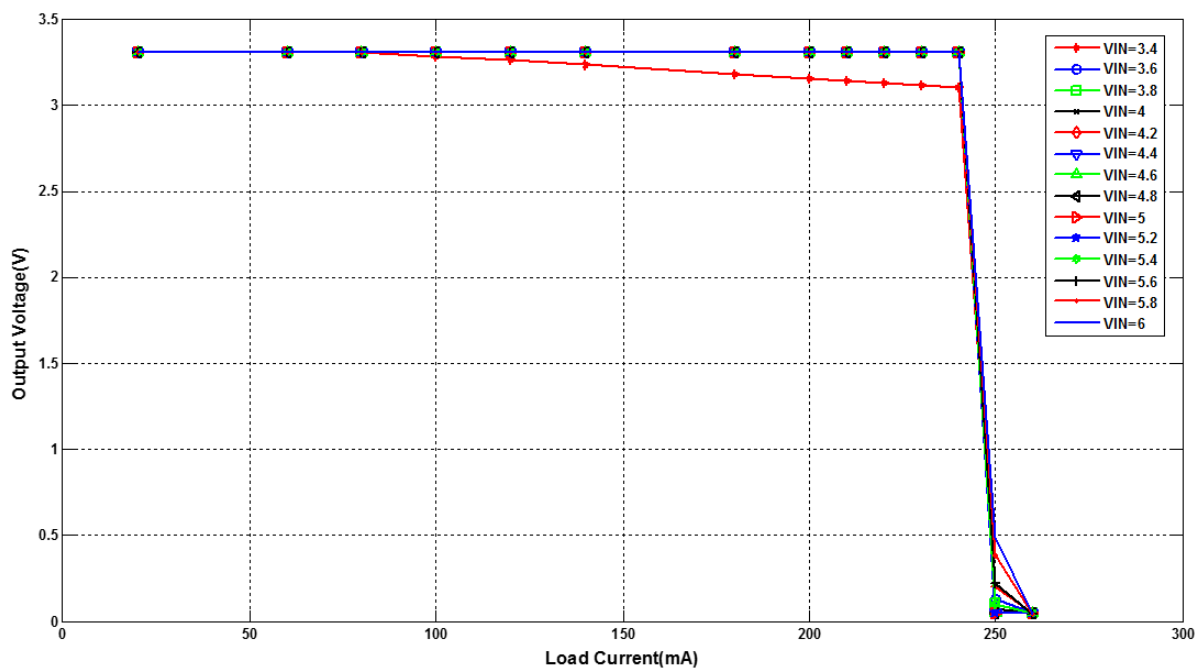Figure 5. GND Pin Current (single channel) vs. Load Current

Figure 6. Output Voltage vs. Load Current (Current Limit)

TYPICAL PERFORMANCE CURVES (continued)
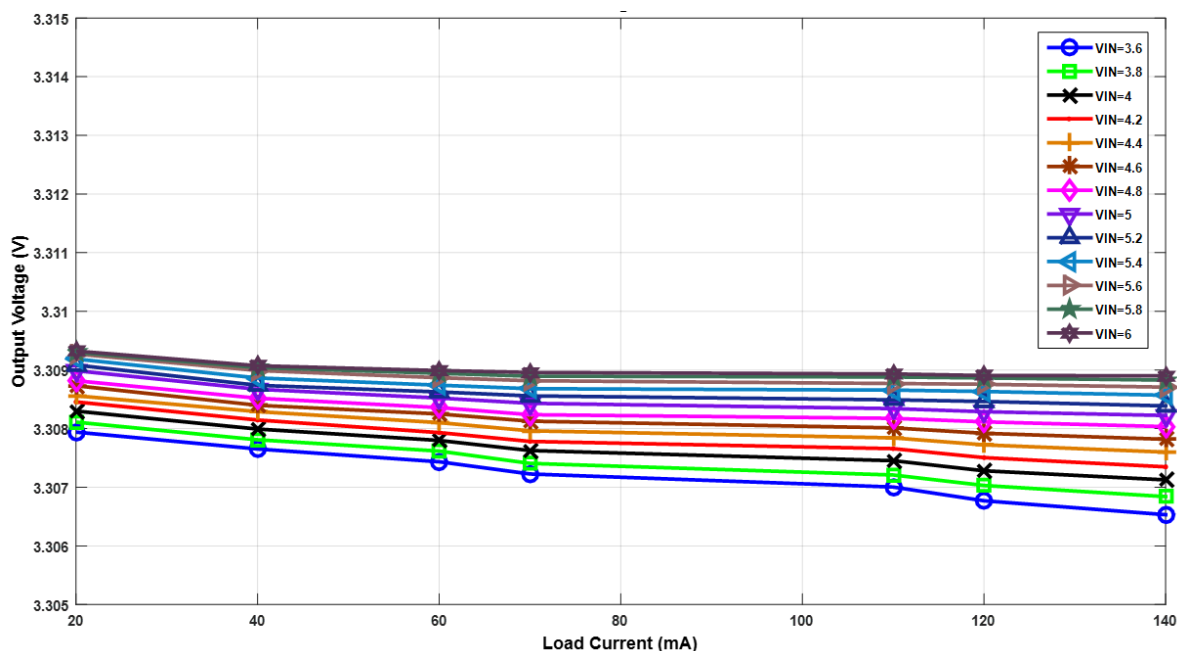
Figure 7. Output Voltage vs. Load Current (Load Regulation)
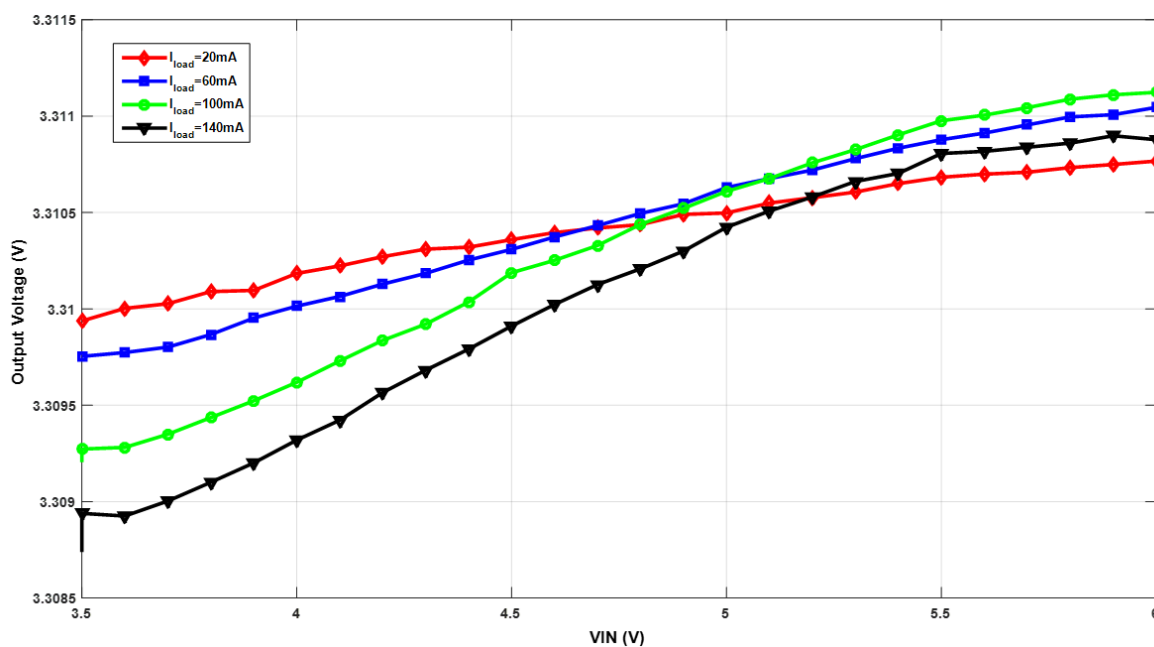
Figure 8. Output Voltage vs. Input Voltage (Line Regulation)

ES9311Q Dual, Ultra-Low Noise Linear Regulator

TYPICAL PERFORMANCE CURVES (continued)
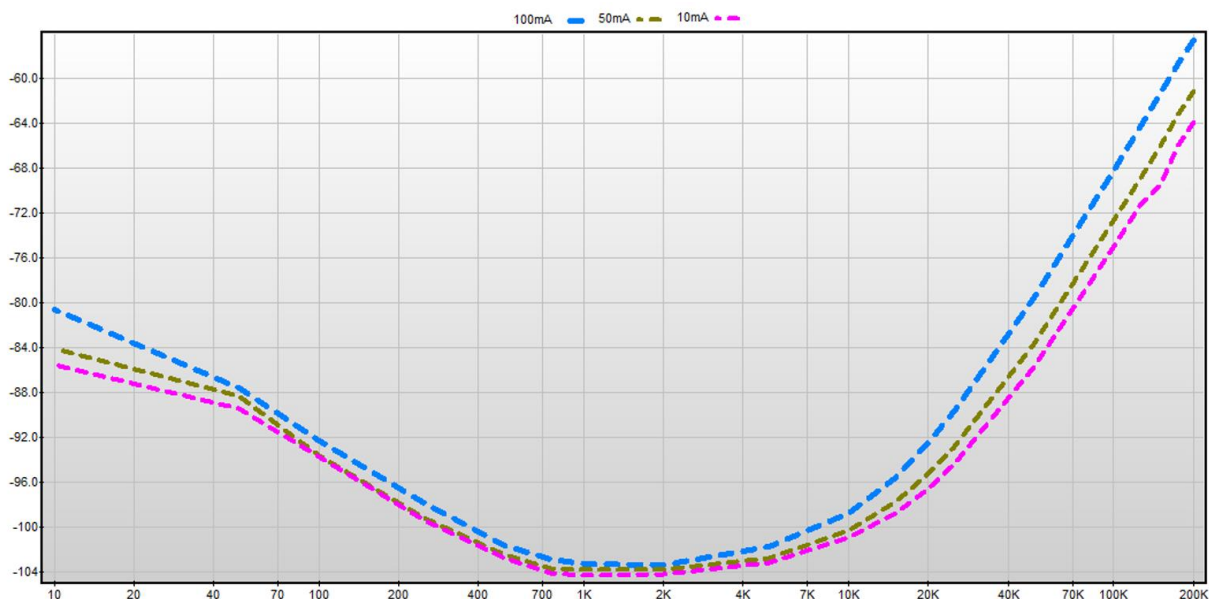
Figure 9. Power Supply Rejection (dB) vs. Frequency (Hz) with VIN = 3.8V, 10µF Filter Caps

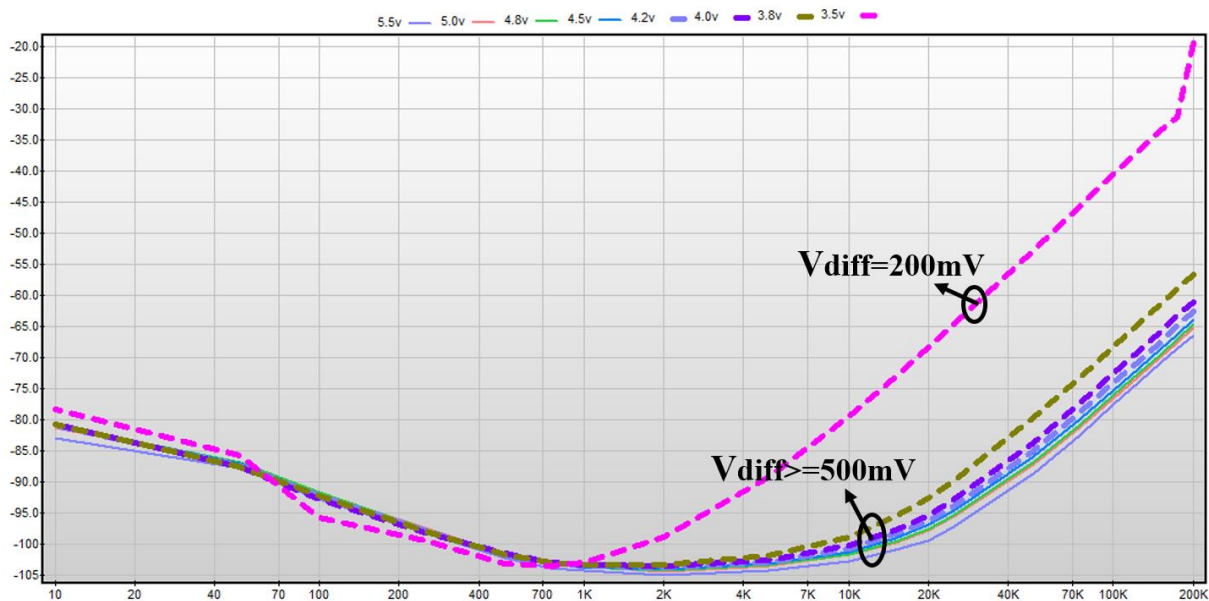Figure 10. Power Supply Rejection (dB) vs. Frequency (Hz) with Iload = 100mA, 10µF Filter Caps

ES9311Q Dual, Ultra-Low Noise Linear Regulator
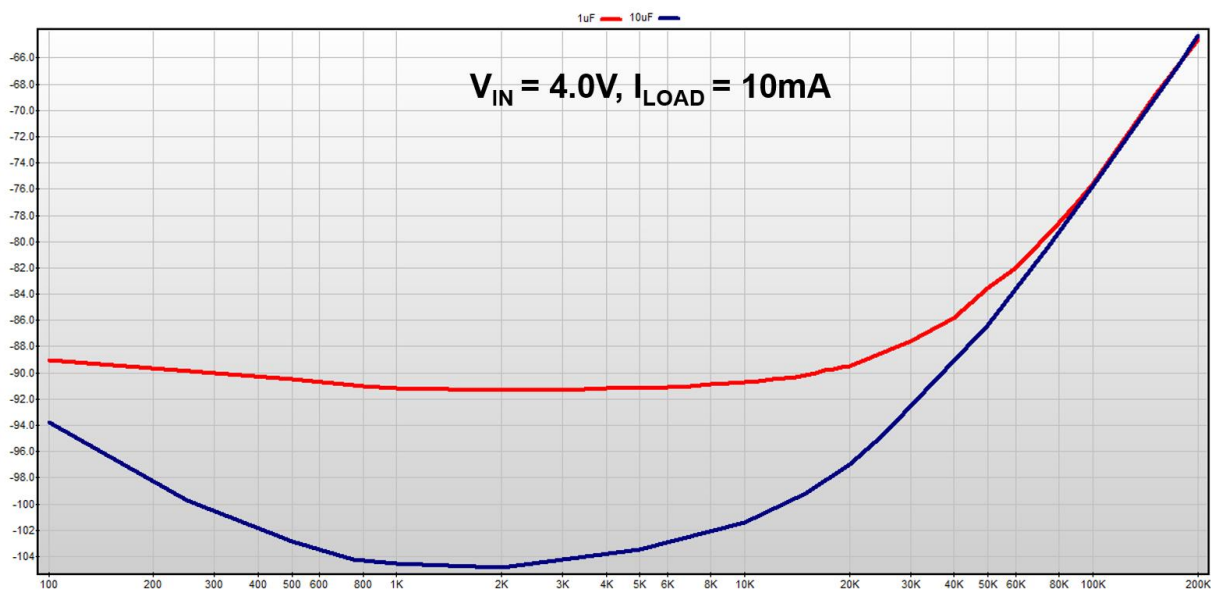
TYPICAL PERFORMANCE CURVES (continued)

Figure 11. Power Supply Rejection (dB) vs. Frequency (Hz) with $1\mu F$ and $10\mu F$ filter Capacitors

ES9311Q Dual, Ultra-Low Noise Linear Regulator
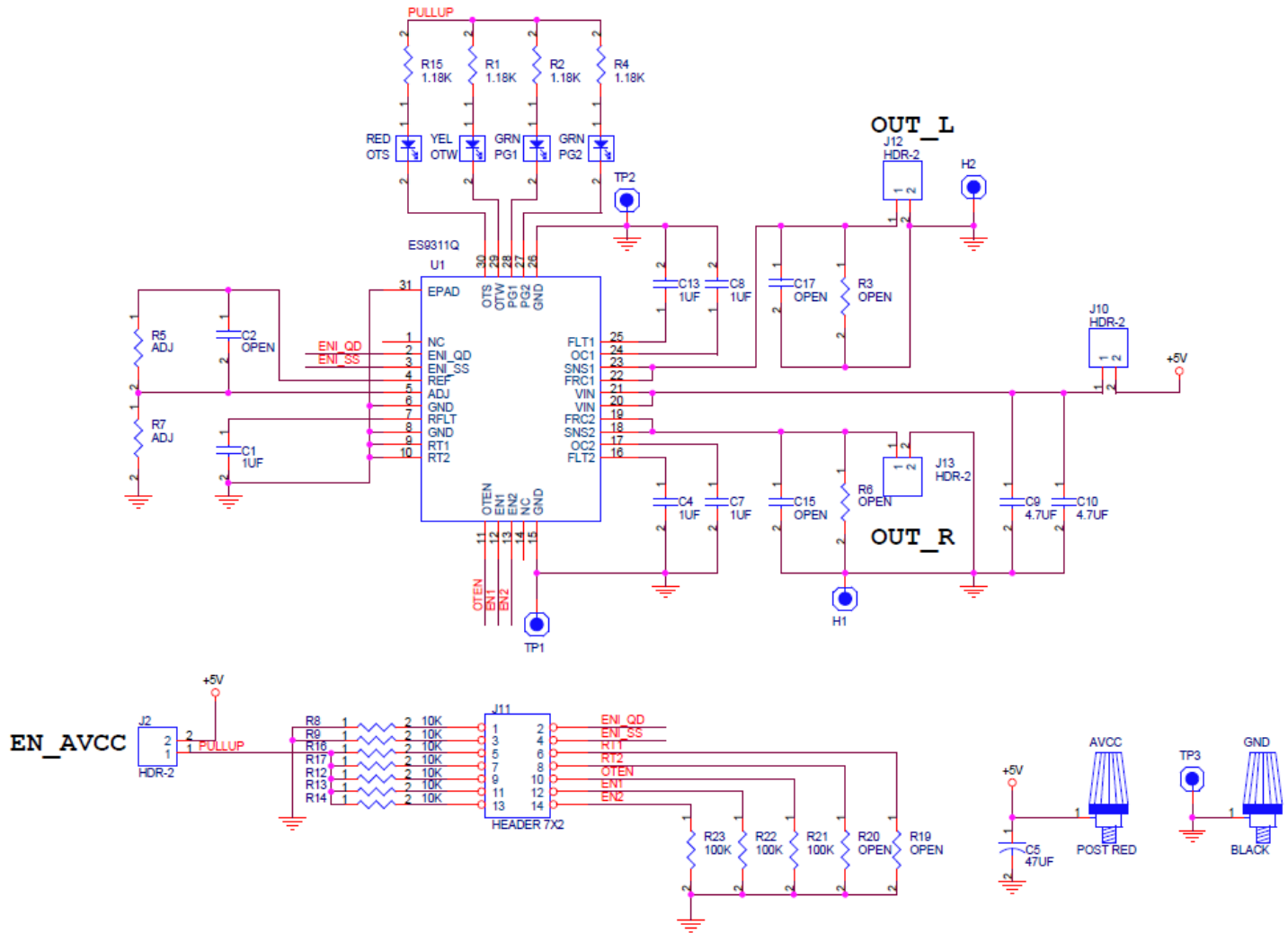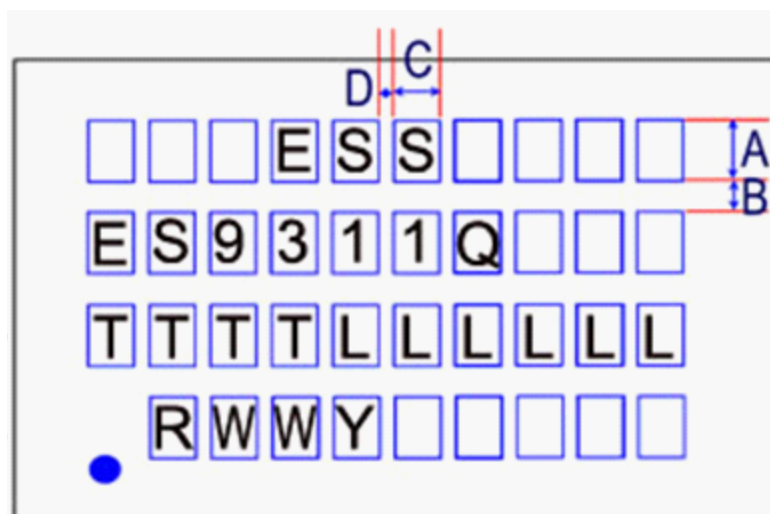

Figure 12. ES9311Q Evaluation Board Circuit

ES9311Q Dual, Ultra-Low Noise Linear Regulator

30-Pin QFN Top View Marking

	Dimension in mm			
Package Type	A	B	C	D
QFN 5mm x 3mm	0.4	0.2	0.3	0.2

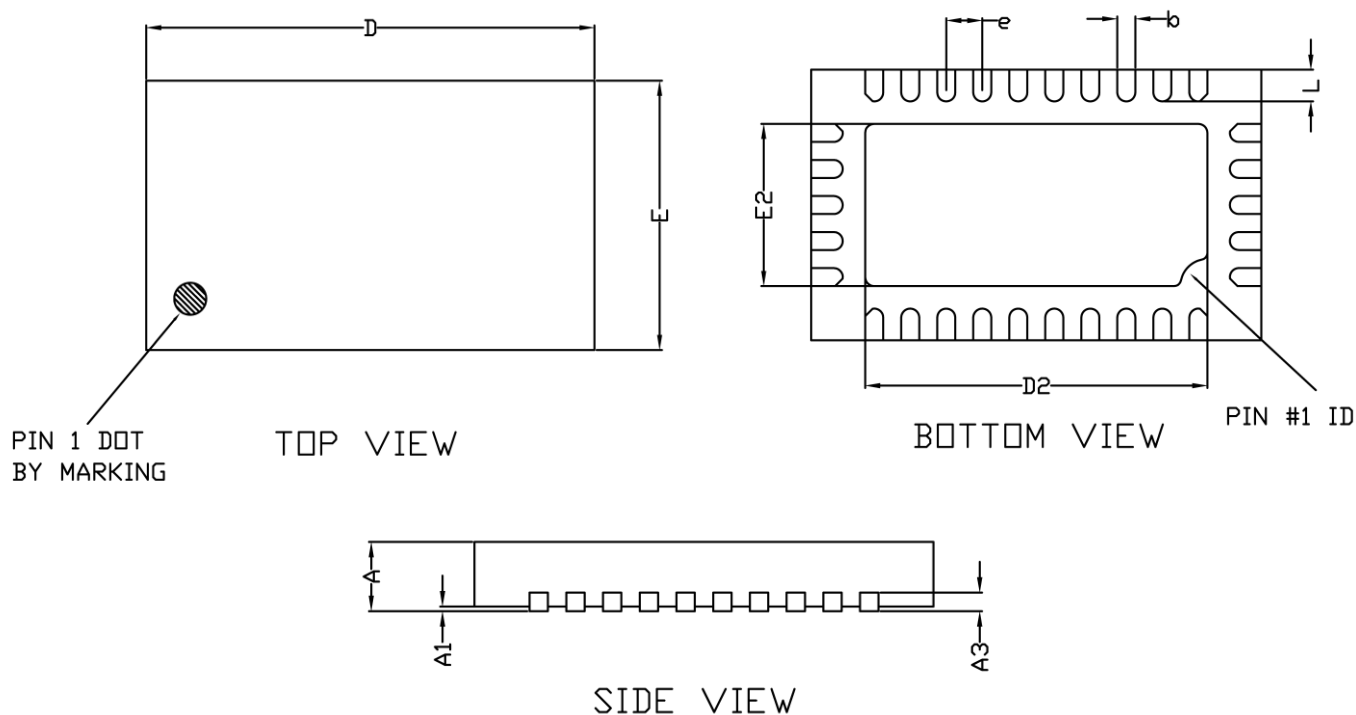|	
T	*Tracking number*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*

Marking is subject to change. This drawing is not to scale.

Figure 13. ES9311Q Marking Diagram

ES9311Q Dual, Ultra-Low Noise Linear Regulator

30-Pin QFN Mechanical Dimensions

PIN 1 DOT
BY MARKING

TOP VIEW

BOTTOM VIEW

PIN #1 ID

SIDE VIEW

Common Dimensions (mm)			
Package	**Very Very Thin**		
Reference	**Minimum**	**Nominal**	**Maximum**
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.2 REF		
D	4.95	5.00	5.05
E	2.95	3.00	3.05
b	0.15	0.20	0.25
L	0.25	0.35	0.45
D2	3.75	3.80	3.85
E2	1.75	1.80	1.85
e	0.4 BSC		

Table 1. Package Dimensions

ES9311Q Dual, Ultra-Low Noise Linear Regulator

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)
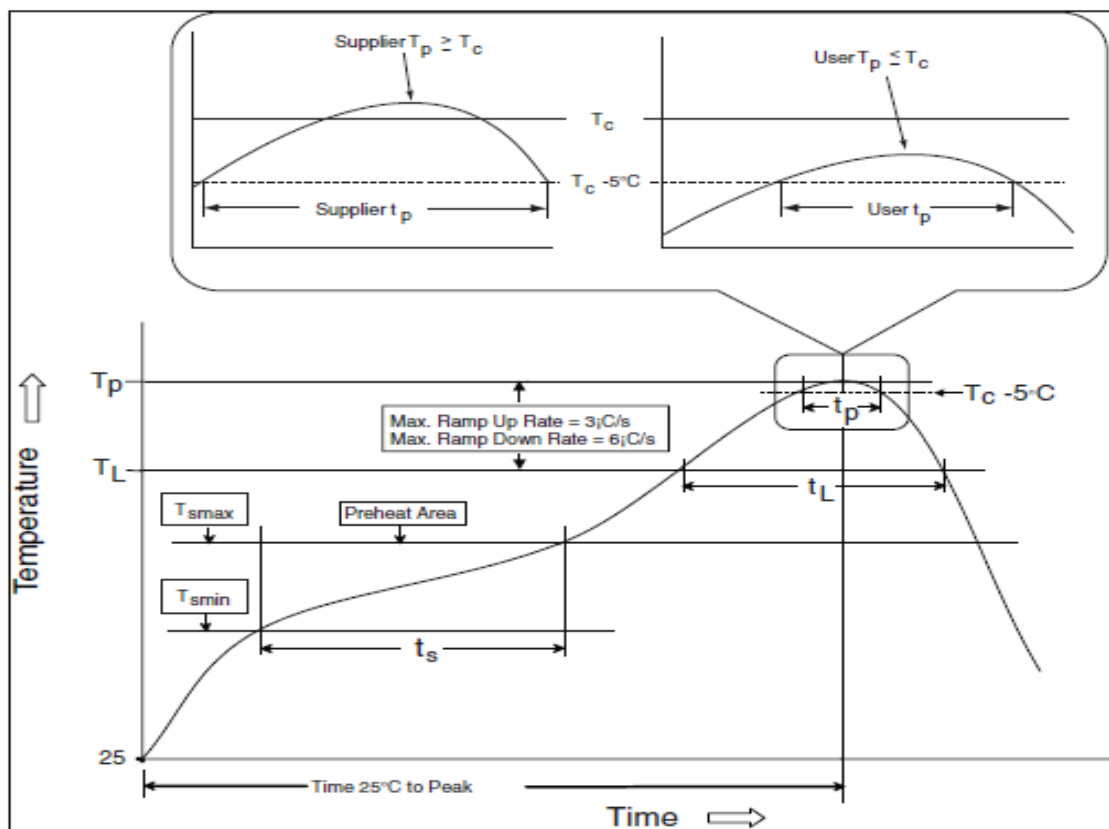
Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:
Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.

ES9311Q Dual, Ultra-Low Noise Linear Regulator

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C / second max.
Time 25°C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ES9311Q Dual, Ultra-Low Noise Linear Regulator

ORDERING INFORMATION

Part Number	Description	Package
ES9311Q	Dual, Ultra-Low Noise Linear Regulator	30-pin QFN

The letter Q identifies the package type QFN.

Revision History

Rev.	Date	Notes
0.1	December 15, 2015	Initial release
0.2	January 4, 2016	Added characterization graphs
0.3	February 16, 2016	Updated values of shutdown current and quiescent current
0.31	March 1, 2016	Corrected package dimension reference in Table 1
0.4	March 14, 2016	Added connection information for exposed pad. Package thermal impedance values added. Expanded section on input and output decoupling
0.51	May 31, 2016	Added information about voltage adjustment using external resistors, "Patent pending", and corrected pin count on package drawing. Added package marking diagram.
0.52	November 9, 2020	Updated the Marking specification
0.53	January 8, 2021	Added Output Range to throughout the document Removed 3.3V from AVCC1/2 in Application Diagram Updated output noise and noise spectral density
0.54	May 3, 2021	Corrected Evaluation board circuit Pin 9,10 set to RT1,RT2 as Reserved, connect to ground for normal operation
0.55	August 22, 2022	Update HQ address