杰力科技股份有限公司
Excelliance MOS Corporation

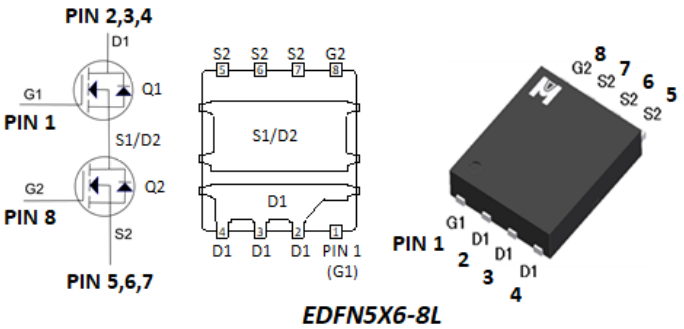
EMP18K03HPCS

Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	Q1	Q2
BVDSS	30V	30V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	5.7mΩ	2.0mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	8.8mΩ	2.8mΩ
I_D @T_C=25°C	77A	172A
I_D @T_A=25°C	16A	29A

▪ Pin Description:



EDFN5X6-8L

Dual N Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant

▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS Q1	LIMITS Q2	UNIT
Gate-Source Voltage		V_{GS}	±20	±12	V
Continuous Drain Current	T_C = 25 °C	I_D	77	172	A
	T_C = 100 °C		48	126	
Continuous Drain Current	T_A = 25 °C	I_D	16	29	
	T_A = 70 °C		12	23	
Pulsed Drain Current[1]		I_{DM}	136	384	
Avalanche Current		I_{AS}	70	100	
Avalanche Energy	L = 0.01mH	EAS	24.5	50	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	122.5	250	
Power Dissipation	T_C = 25 °C	P_D	54	125	W
	T_C = 100 °C		22	50	
Power Dissipation	T_A = 25 °C	P_D	2.4	2.7	W
	T_A = 70 °C		1.5	1.7	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

▪ 100% UIS testing in condition of VD=25V, L=0.01mH, VG=10V, IL=54A, RG=25Ω,Rated VDS=30V N-CH_Q1

▪ 100% UIS testing in condition of VD=25V, L=0.01mH, VG=10V, IL=70A, RG=25Ω,Rated VDS=30V N-CH_Q2

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM Q1	MAXIMUM Q2	UNIT
Junction-to-Case		$R_{\theta JC}$		2.3	1.0	°C/W
Junction-to-Top	Steady-State	$R_{\theta JT}$		42	30	
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$		23	18	
	Steady-State	$R_{\theta JA}$		53	46	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test

▪ Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.6	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	μA
		V_{DS} =30V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	77			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		4.2	5.7	mΩ
		V_{GS} = 4.5V, I_D = 20A		6.0	8.8	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 15A		50		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		830		pF
Output Capacitance[5]	C_{oss}			330		
Reverse Transfer Capacitance[5]	C_{rss}			40		
Gate Resistance[4,5]	R_g	f = 1MHz		0.7		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 20A		15		nC
	Q_g(V_{GS}=4.5V)			6.9		
Gate-Source Charge[1,2,5]	Q_{gs}			3.3		
Gate-Drain Charge[1,2,5]	Q_{gd}			1.8		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		5.8		nS
Rise Time[1,2,5]	t_r			11		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			14		
Fall Time[1,2,5]	t_f			3.1		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				45	A
Pulsed Current[3]	I_{SM}				136	
Forward Voltage[1,4]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 20A, dI_F/dt = 400A / μS		12		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2.1		A
Reverse Recovery Charge[5]	Q_{rr}			13		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪Q1_TYPICAL CHARACTERISTICS

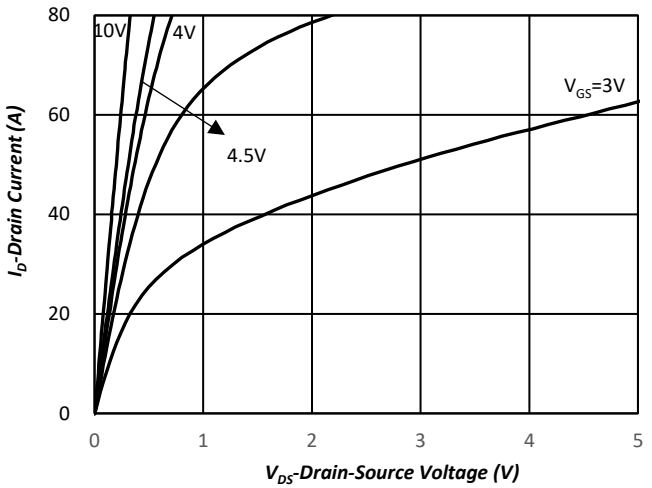


Fig.1 Typical Output Characteristics

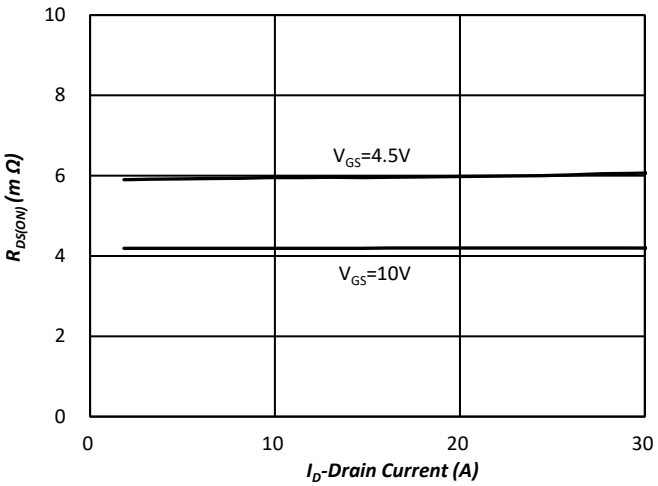


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

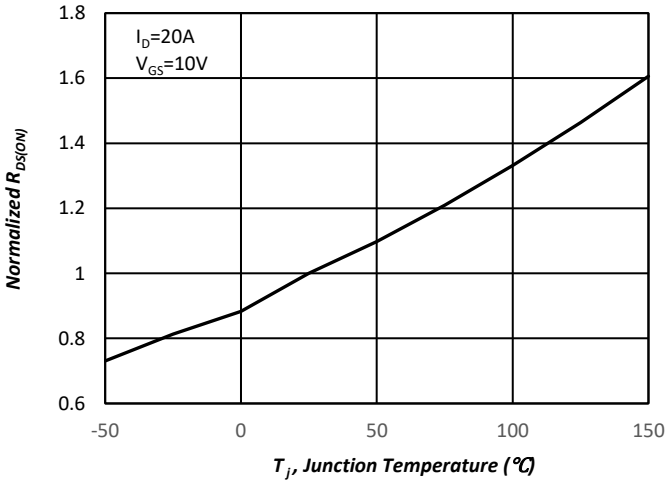


Fig.3 Normalized On-Resistance v.s. Junction Temperature

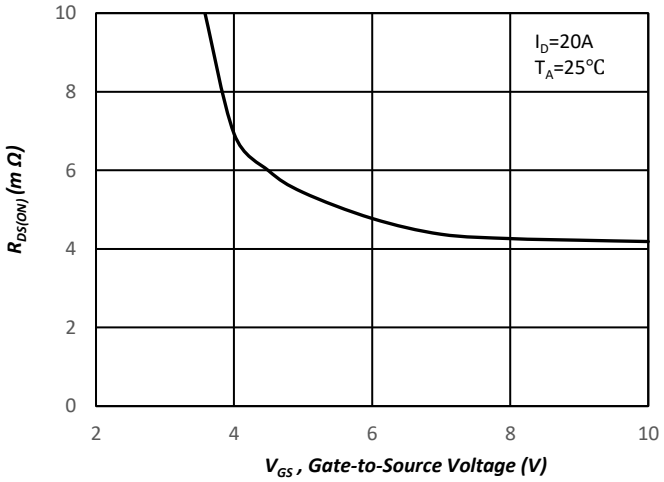


Fig.4 On-Resistance v.s. Gate Voltage

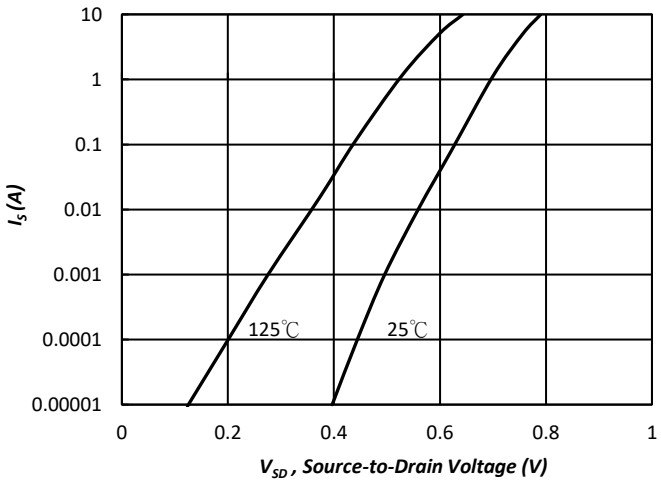


Fig.5 Forward Characteristic of Reverse Diode

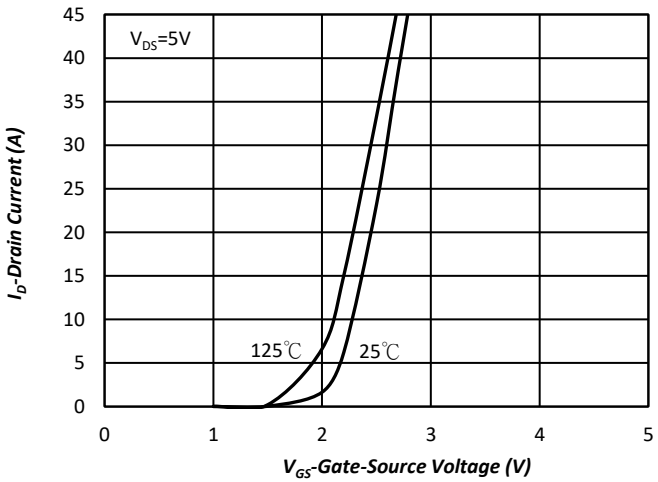


Fig.6 Transfer Characteristics

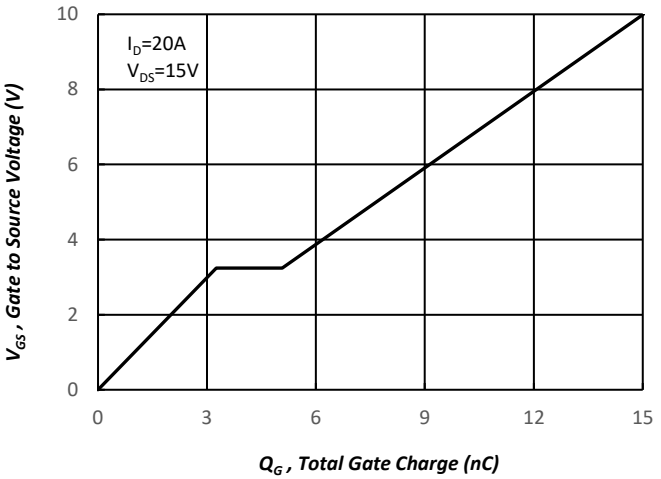


Fig.7 Gate Charge Characteristics

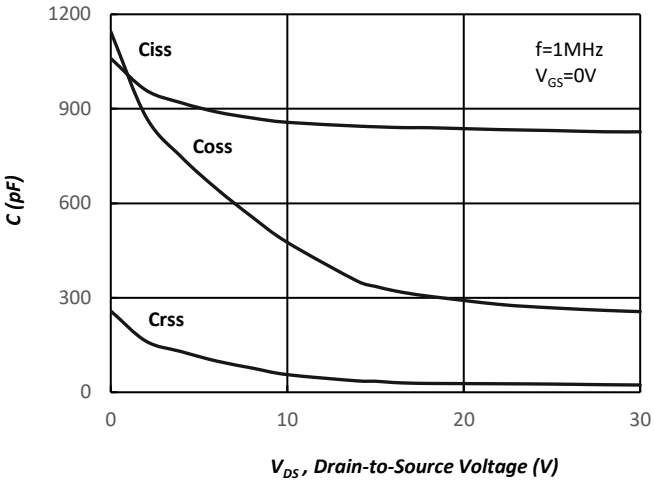


Fig.8 Typical Capacitance Characteristics

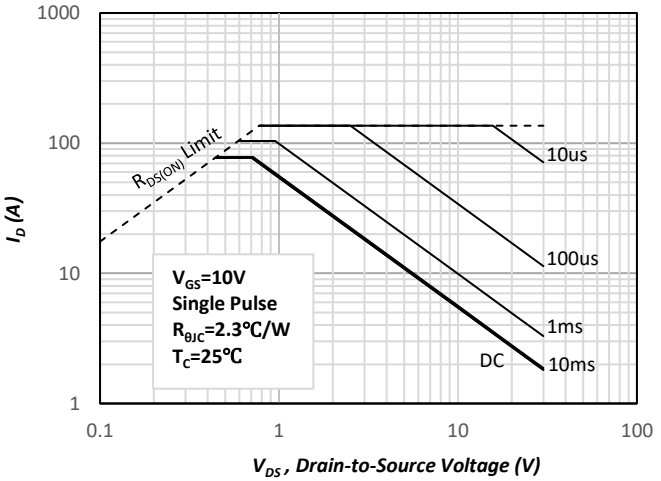


Fig 9. Maximum Safe Operating Area

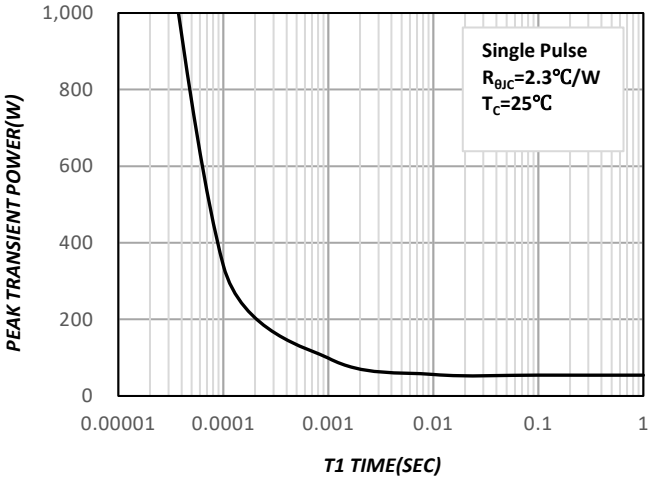


Fig 10. Single Pulse Maximum Power Dissipation

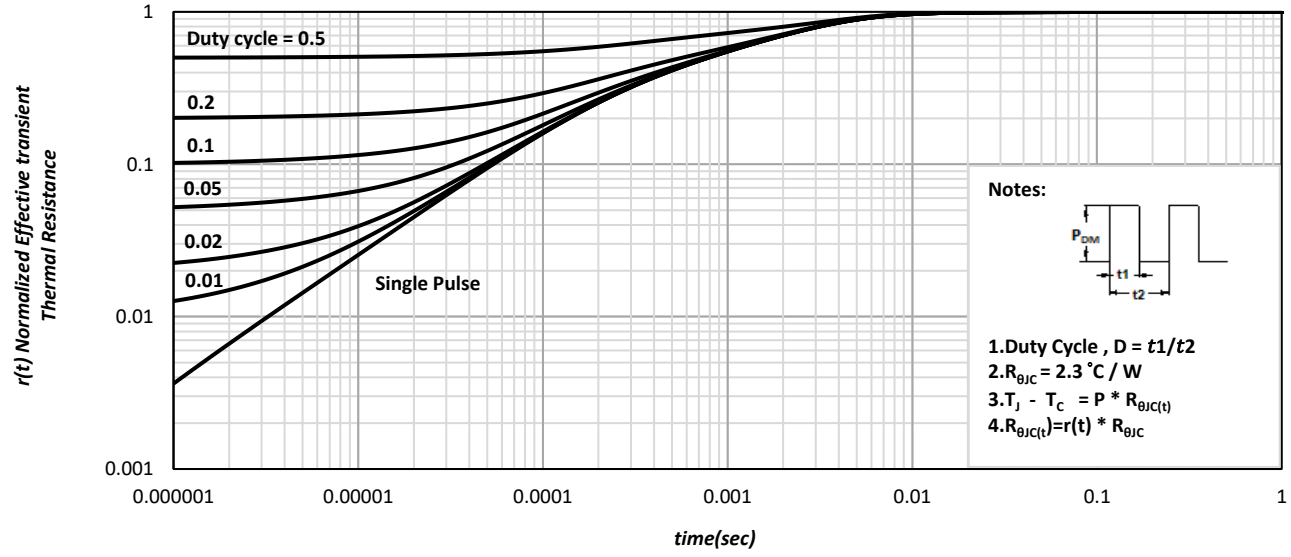


Fig 11. Effective Transient Thermal Impedance

▪ Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.6	2.5	V
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	μA
		V_{DS} =30V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	172			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		1.5	2.0	mΩ
		V_{GS} = 4.5V, I_D = 20A		2.1	2.8	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 15A		110		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		2470		pF
Output Capacitance[5]	C_{oss}			830		
Reverse Transfer Capacitance[5]	C_{rss}			55		
Gate Resistance[4,5]	R_g	f = 1MHz		0.8		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 20A		45		nC
	Q_g(V_{GS}=4.5V)			20		
Gate-Source Charge[1,2,5]	Q_{gs}			8.2		
Gate-Drain Charge[1,2,5]	Q_{gd}			4.1		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		9.9		nS
Rise Time[1,2,5]	t_r			13		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			33		
Fall Time[1,2,5]	t_f			8.2		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				104	A
Pulsed Current[3]	I_{SM}				384	
Forward Voltage[1,4]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 20A, dI_F/dt = 400A /μS		29		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			3.3		A
Reverse Recovery Charge[5]	Q_{rr}			47		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

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▪Q2_TYPICAL CHARACTERISTICS

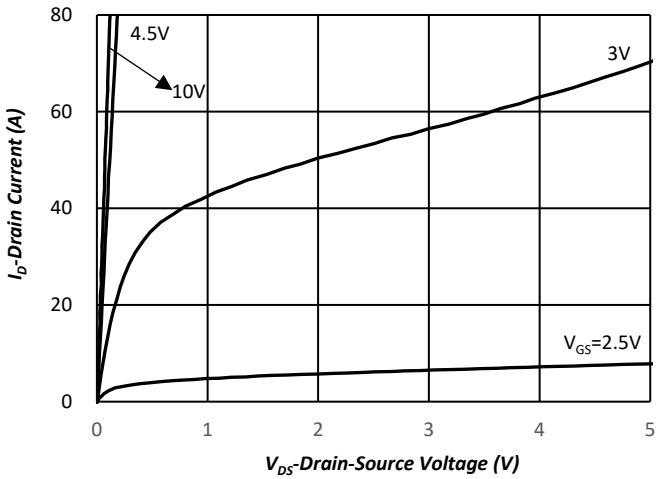


Fig.1 Typical Output Characteristics

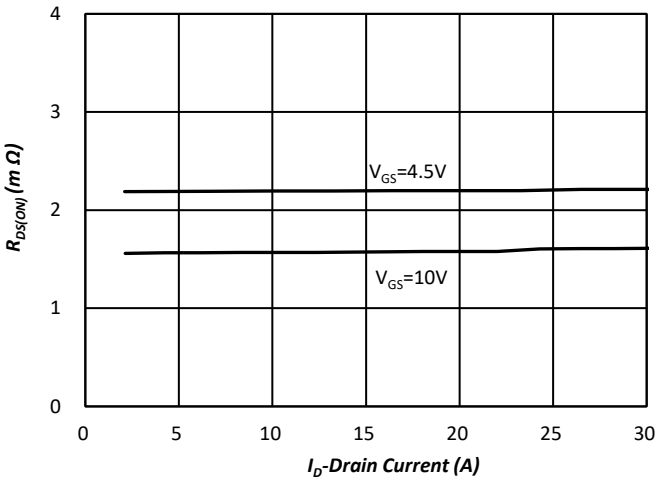


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

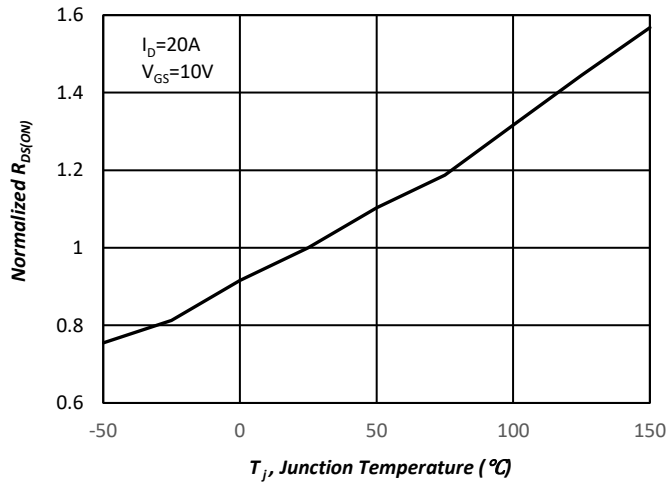


Fig.3 Normalized On-Resistance v.s. Junction Temperature

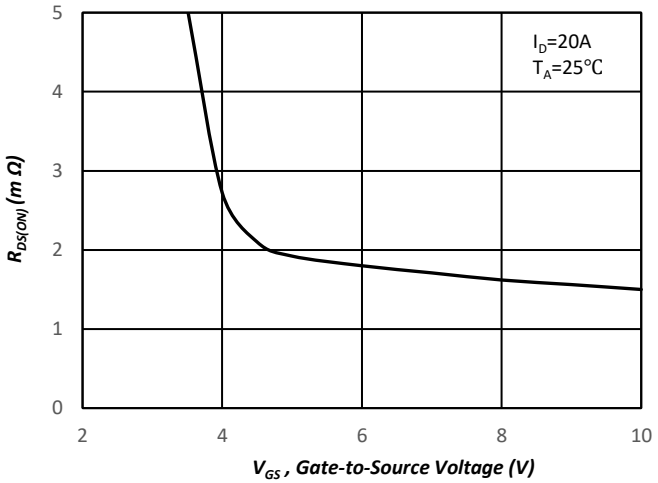


Fig.4 On-Resistance v.s. Gate Voltage

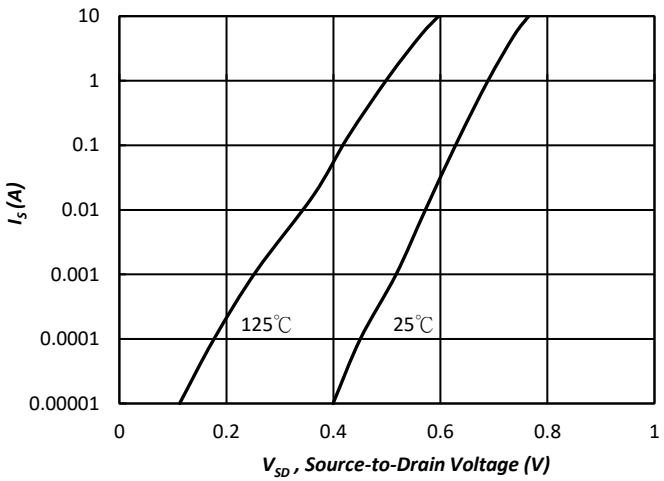


Fig.5 Forward Characteristic of Reverse Diode

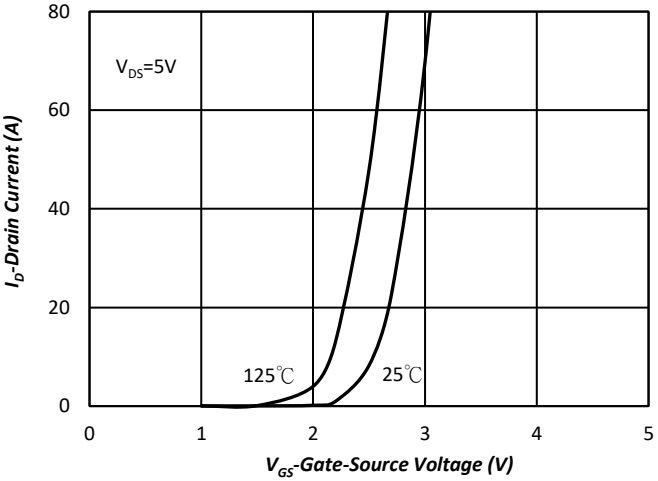


Fig.6 Transfer Characteristics

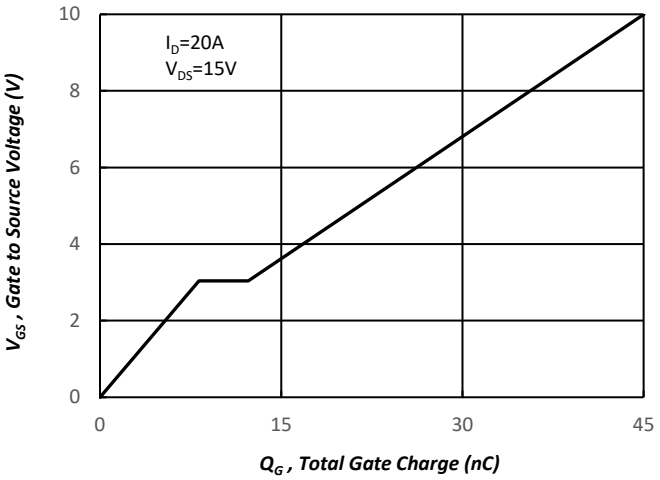


Fig.7 Gate Charge Characteristics

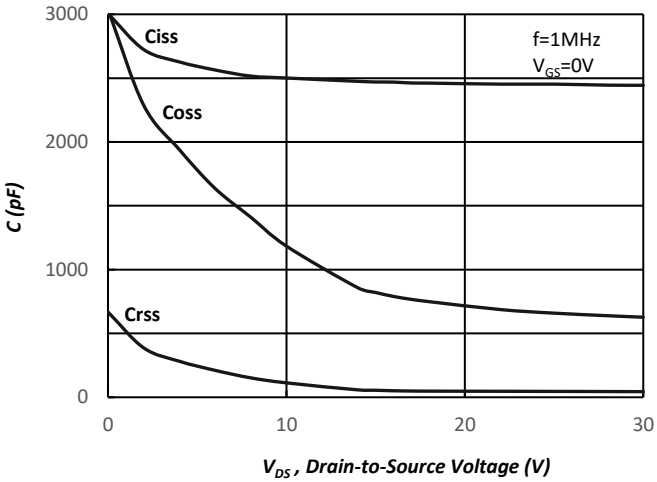


Fig.8 Typical Capacitance Characteristics

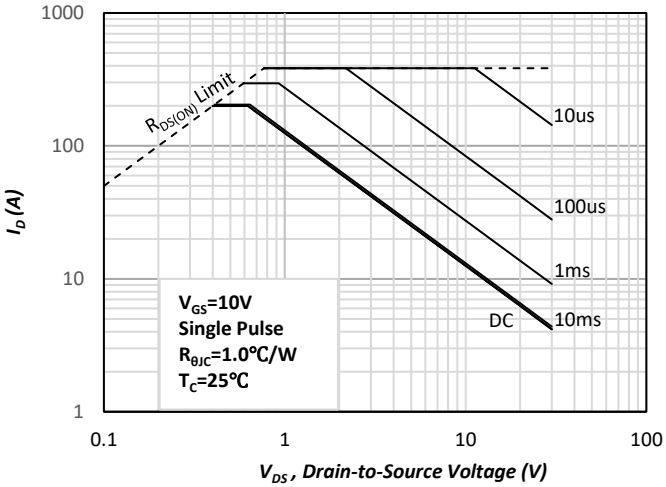


Fig 9. Maximum Safe Operating Area

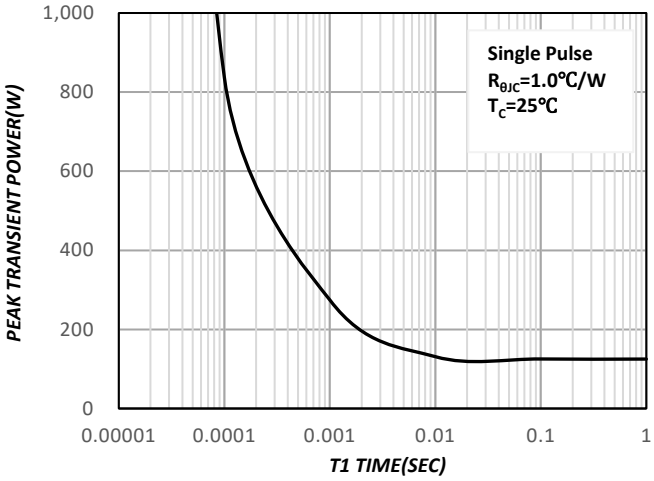


Fig 10. Single Pulse Maximum Power Dissipation

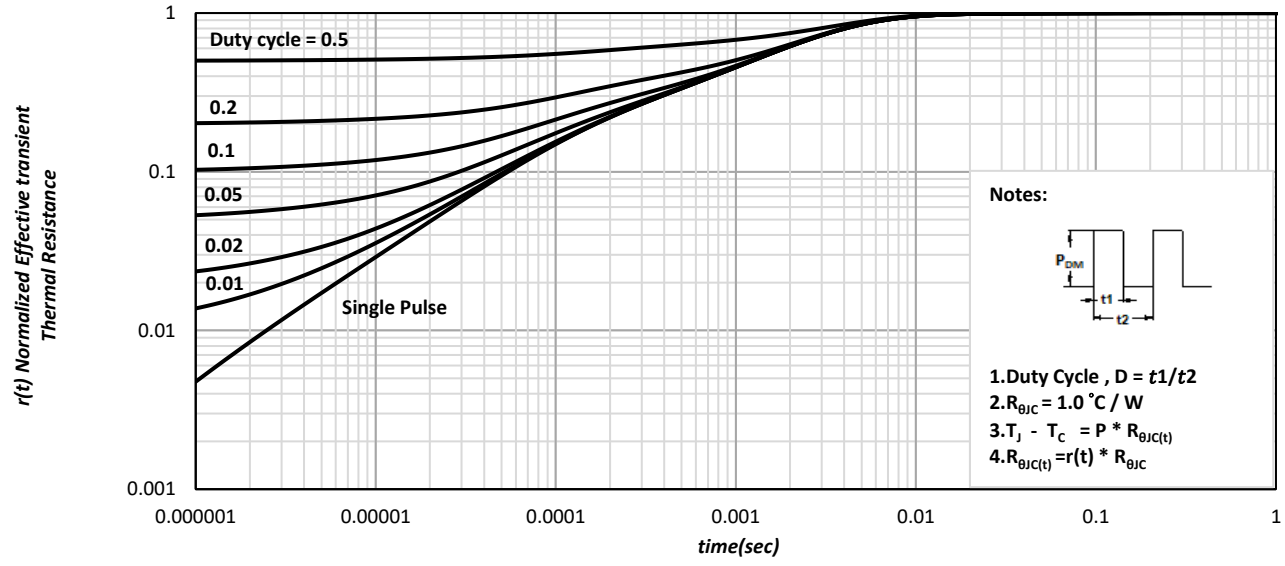


Fig 11. Effective Transient Thermal Impedance

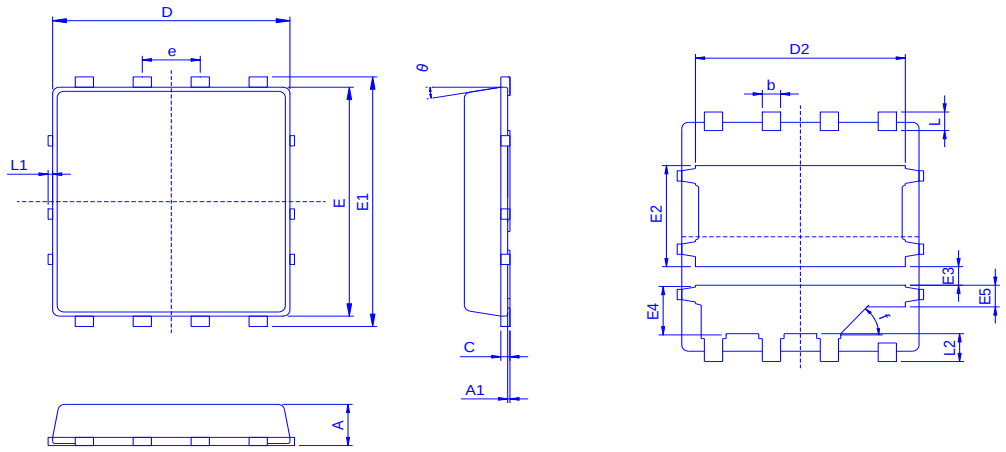
Ordering & Marking Information:

Device Name: EMP18K03HPCS for Asymmetric EDFN5X6-8L

P18K03S: Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

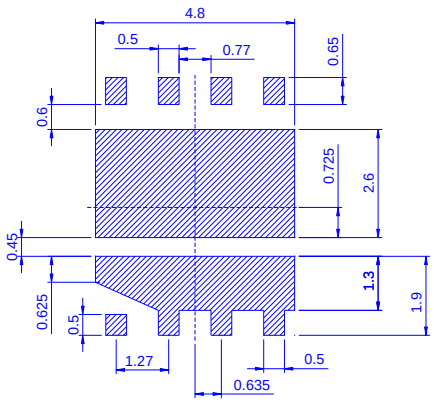
Outline Drawing



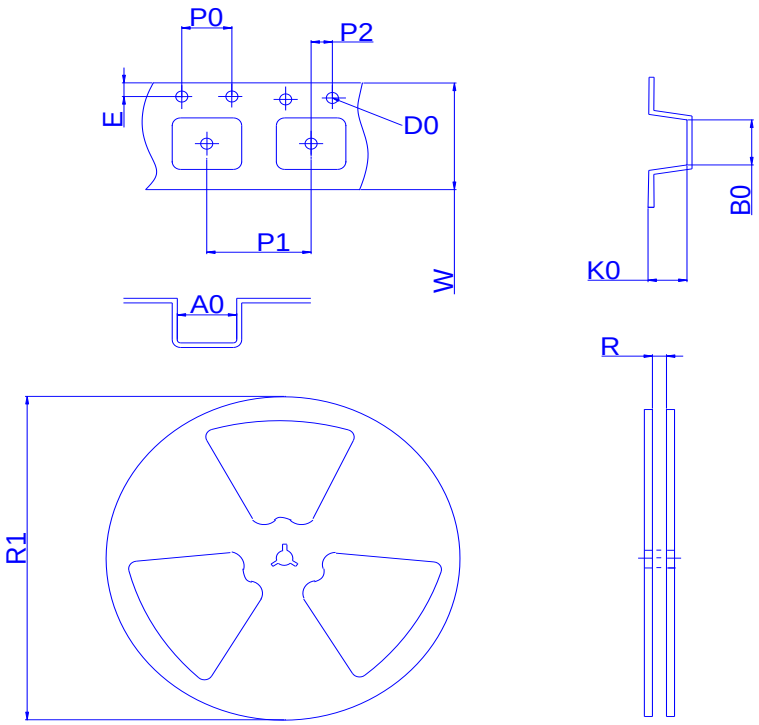
Dimension	A	A1	b	c	D	D2	E	E1	E2	E3	E4	E5	e
Min.	0.85	-	0.33	0.15	4.80	3.61	5.55	5.90	2.02	0.40	1.10	0.48	-
Typ.	0.90	-	0.40	0.20	4.90	3.81	5.65	6.00	2.17	0.45	1.18	0.53	1.27
Max.	1.10	0.05	0.51	0.30	5.40	4.70	5.80	6.10	2.50	0.60	1.42	0.58	-

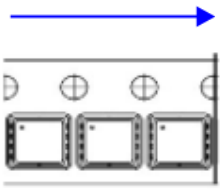
Dimension	L	L1	L2	θ
Min.	0.35	-	0.48	0°
Typ.	0.45	-	0.58	
Max.	0.71	0.10	0.81	12°

Footprint



◆ **Tape&Reel Information:2500pcs/Reel**



Package	EDFN5X6-8L
Reel	13”
Device orientation	FEED DIRECTION 

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.6	4	8	2	12	12.4	330
±	0.2	0.2	0.1	0.1	0.6	0.1	0.1	0.1	0.3	2	2