EMIF08-VID01C2

8 line low capacitance EMI filter and ESD protection

Main product characteristics

Where EMI filtering in ESD sensitive equipment is required :

- LCD & camera for mobile phones
- Computers and printers
- Communication systems
- MCU Boards

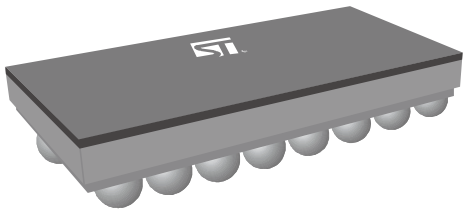
Description

The EMIF08-VID01C2 is an 8 line highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The flip chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15kV.

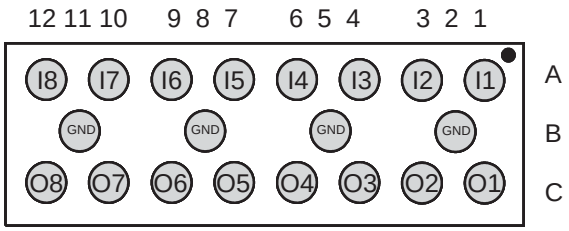
Benefits

- High efficiency EMI filter (-33 dB @ 900 Mhz)
- Low line capacitance suitable for high speed data bus
- Low serial resistance for camera impedance adaptation
- Optimized PCB space consuming: 1.29 mm x 3.92 mm
- Very thin package: 0.695 mm
- Coating resin on back side and lead free package
- High efficiency in ESD suppression on inputs pins (IEC61000-4-2 level 4).
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.



Coated flip chip package

Pin configuration (Bumps side)



Complies with following standards:

IEC61000-4-2

level 4 input pins	15 kV	(air discharge)
	8 kV	(contact discharge
level 1 output pins	2 kV	(air discharge)
	2 kV	(contact discharge

MIL STD 883E - Method 3015-6 Class 3

Figure 1. Basic cell configuration

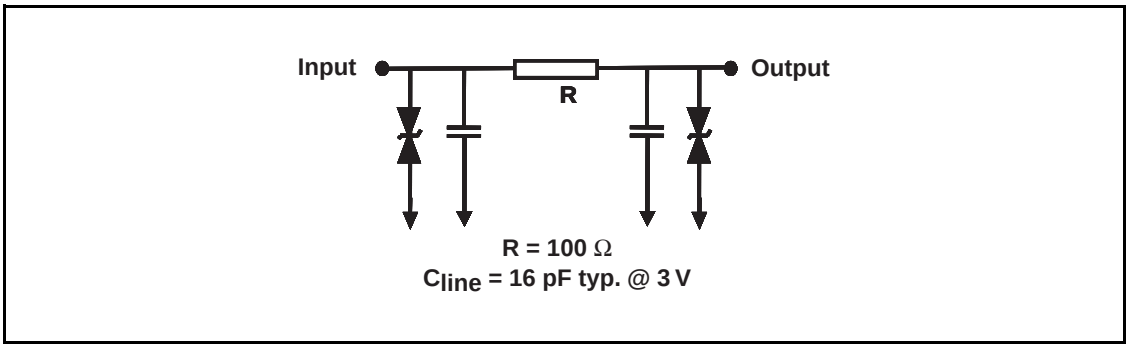
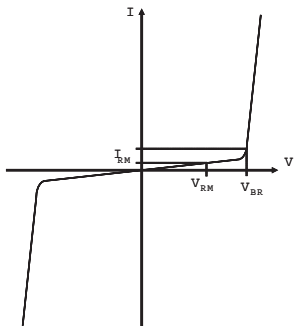


Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
Vpp	ESD discharge IEC61000-4-2 air discharge ESD discharge IEC61000-4-2 contact discharge	15 8	kV KV
Tj	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

1 Electrical characteristics (T_{amb} = 25°C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
R	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1mA	6	8	10	V
I_{RM}	V_{RM} = 3V per line			500	nA
$R_{I/O}$	I=10mA	80	100	120	Ω
C_{line}	V_R = 3V DC, 1 MHz		16	19	pF

Figure 2. S21 (dB) attenuation measurement

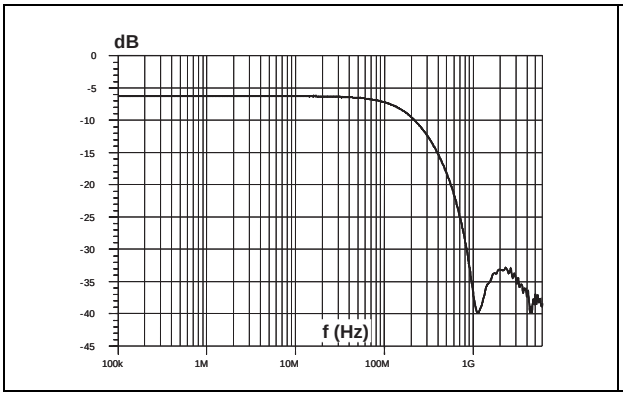


Figure 3. Analog crosstalk measurement

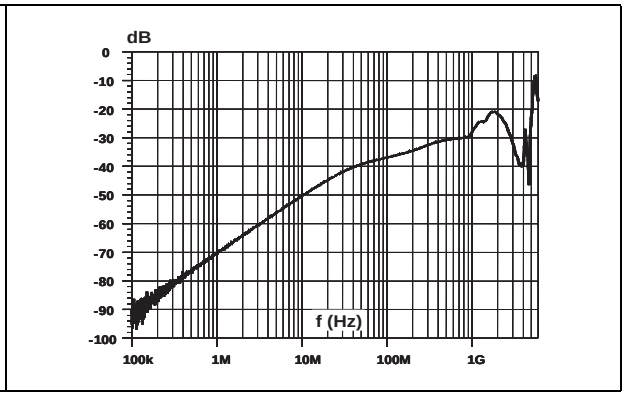


Figure 4. ESD response to IEC61000-4-2 (+15 kV air discharge) on one input V_{in} and one output V_{out}

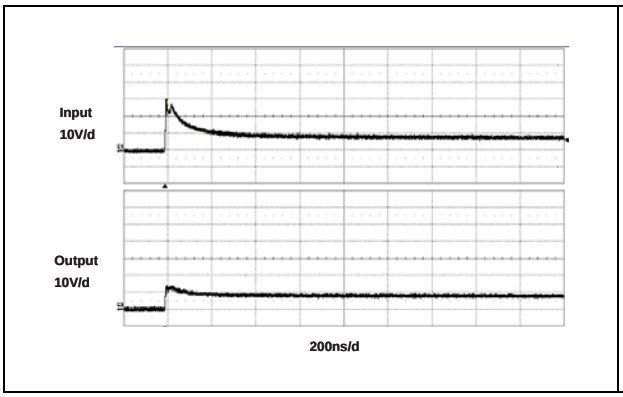


Figure 5. ESD response to IEC61000-4-2 (- 15 kV air discharge) on one input V_{in} and one output V_{out}

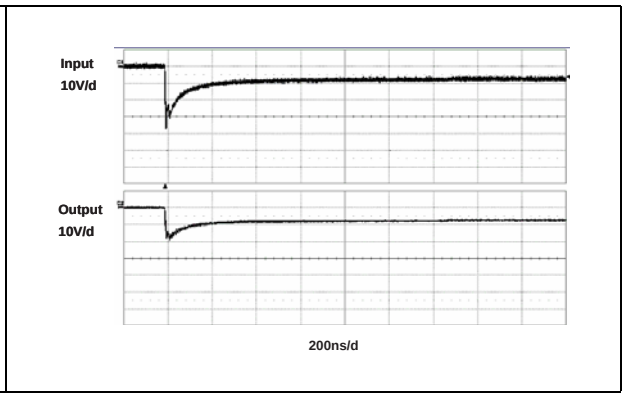
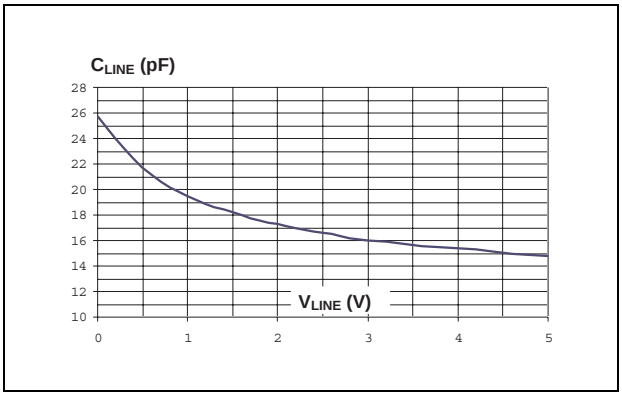
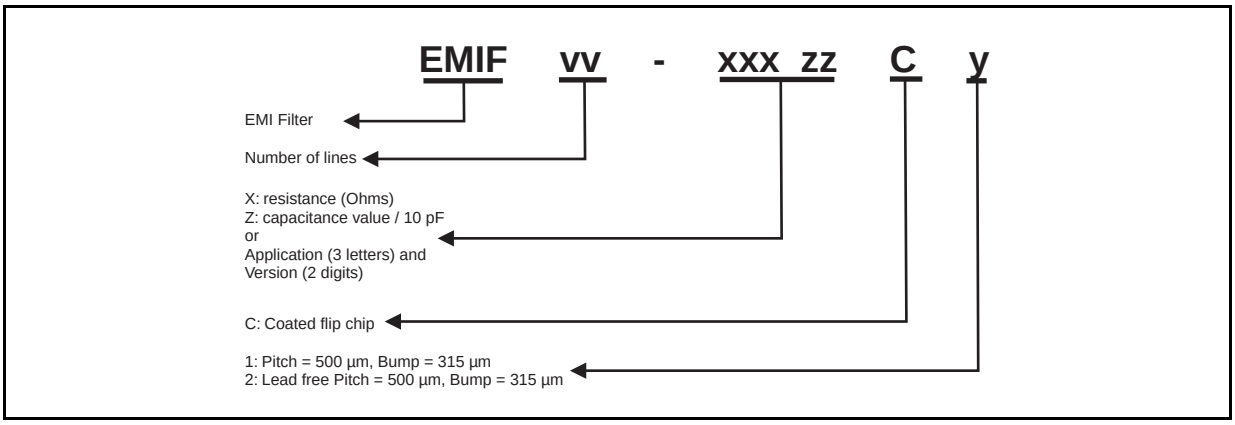


Figure 6. Line capacitance versus applied voltage



2 Ordering information scheme



3 Package mechanical data flip chip

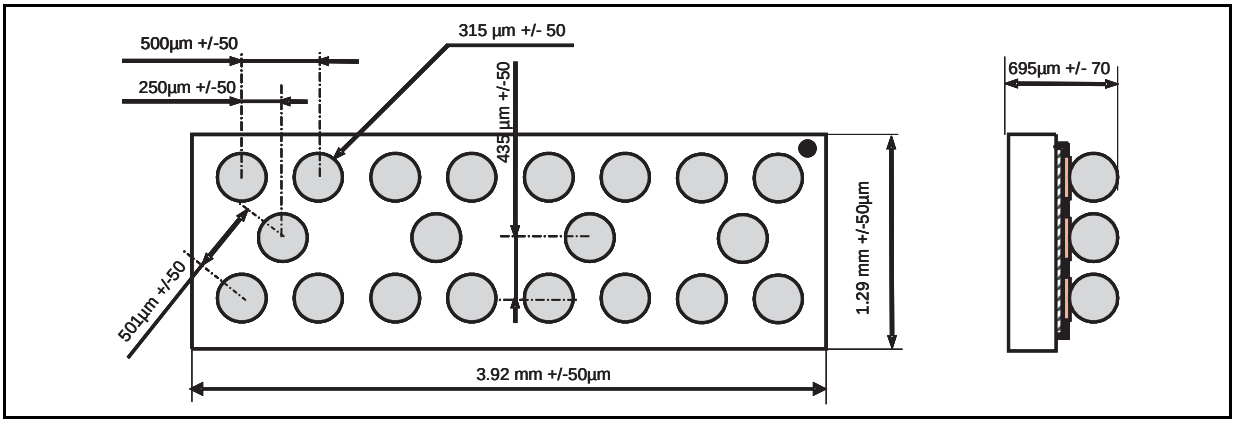


Figure 7. Marking

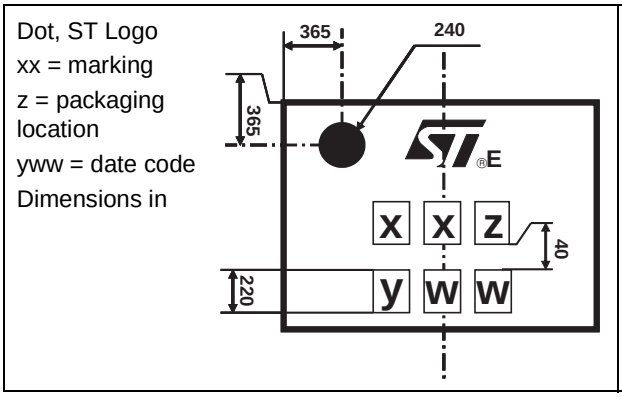


Figure 8. Foot print receommendation

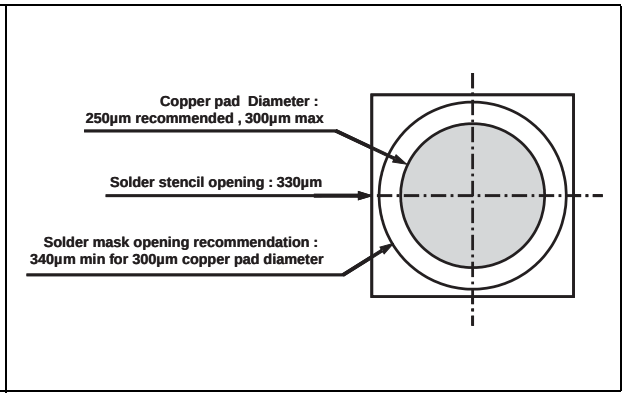
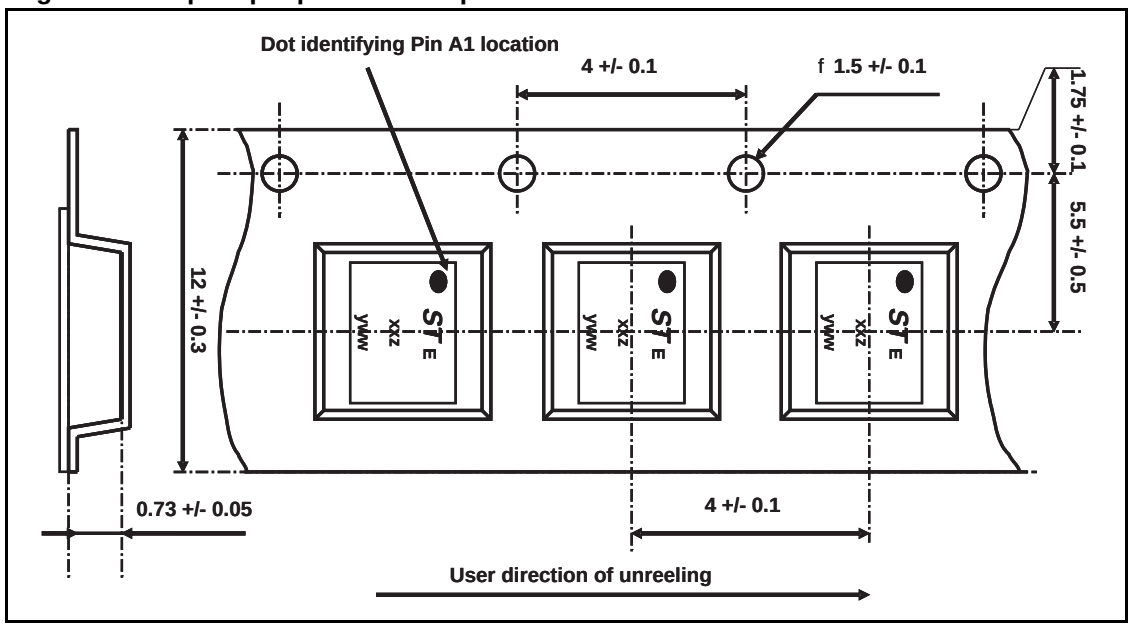


Figure 9. Flip chip tape and reel specification



4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF08-VID01C2	GS	Flip Chip	7.4mg	5000	7” Tape and reel

5 Revision history

Date	Revision	Changes
13-Jul-2005	1	Initial release.
11-Aug-2005	2	Fonts changed in Figures 7, 8, and 9.