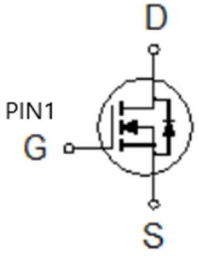
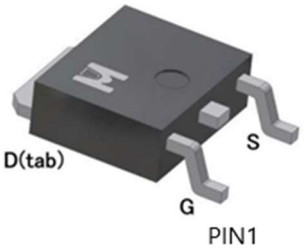
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DSON\ (MAX.)}$	25mΩ
I_D	35A





N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	35	A
	T_C = 100 °C		22	
Pulsed Drain Current[1]		I_{DM}	140	
Avalanche Current		I_{AS}	50	
Avalanche Energy	L = 0.1mH	E_{AS}	125	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	62.5	
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V			1	μA
		V_{DS} = 70V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	35			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 30A		21.5	25	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 30A		38		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		1575		pF
Output Capacitance	C_{oss}			216		
Reverse Transfer Capacitance	C_{rss}			47		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.5		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 80V, V_{GS} = 10V, I_D = 30A		20.8		nC
Gate-Source Charge[1,2]	Q_{gs}			8.5		
Gate-Drain Charge[1,2]	Q_{gd}			6.8		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 50V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		20		nS
Rise Time[1,2]	t_r			80		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			90		
Fall Time[1,2]	t_f			100		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				35	A
Pulsed Current[3]	I_{SM}				140	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 25A, dI_F/dt = 100A / μS		120		nS
Reverse Recovery Charge	Q_{rr}			380		nC

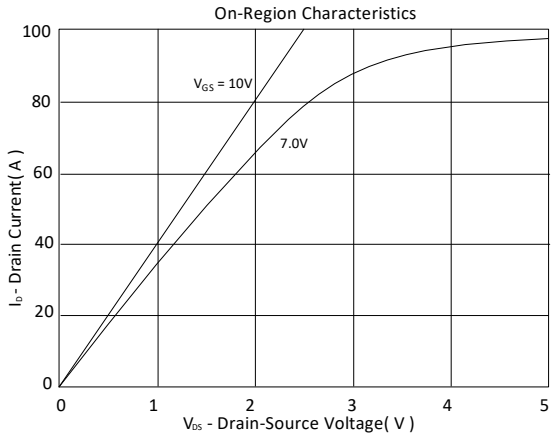
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

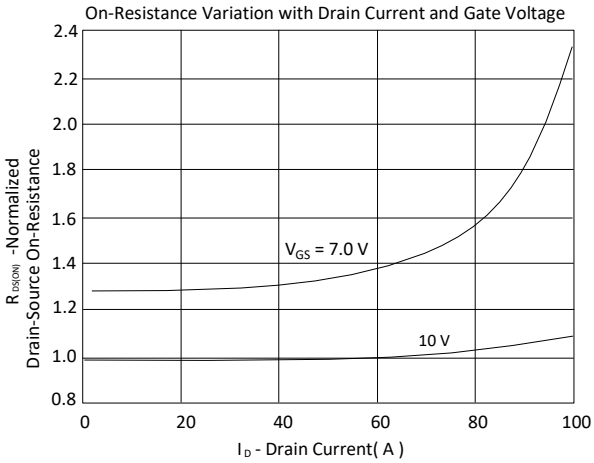
[2]Independent of operating temperature.

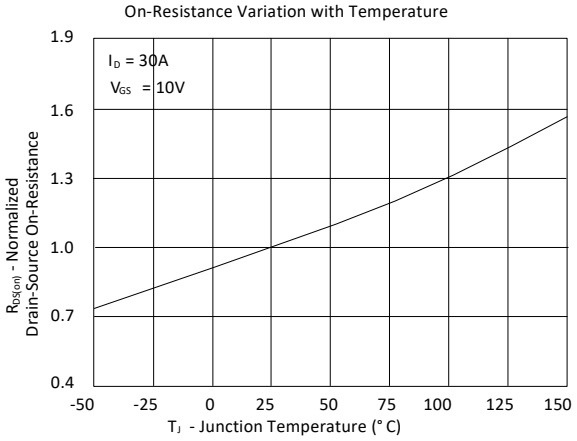
[3]Pulse width limited by maximum junction temperature.

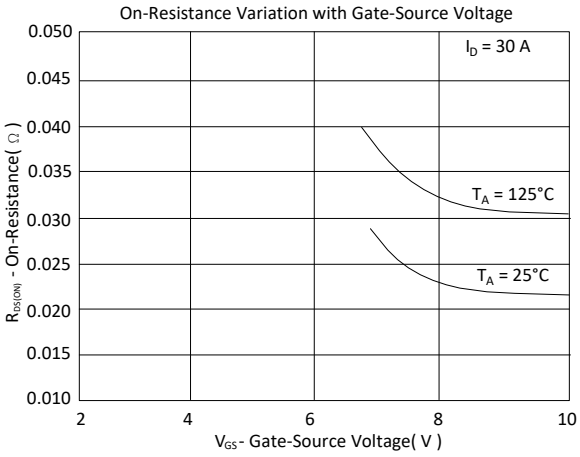
EMC will review datasheet by quarter, and update new version.

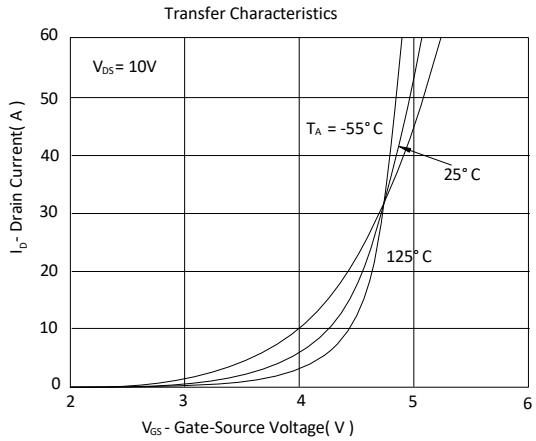
TYPICAL CHARACTERISTICS

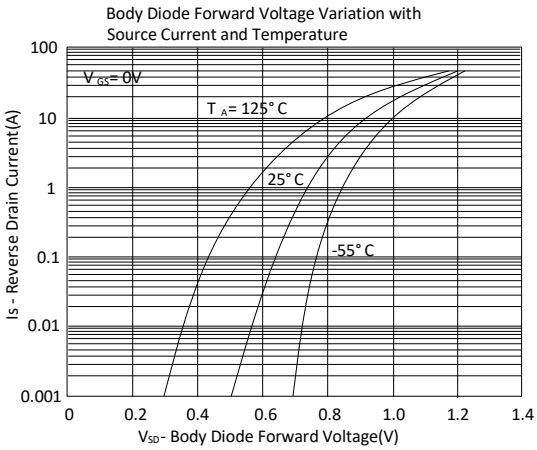




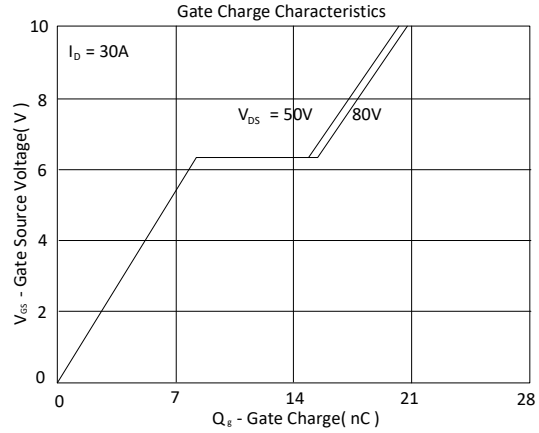




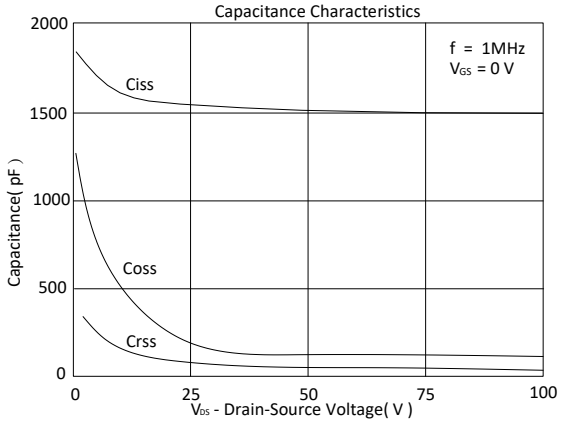




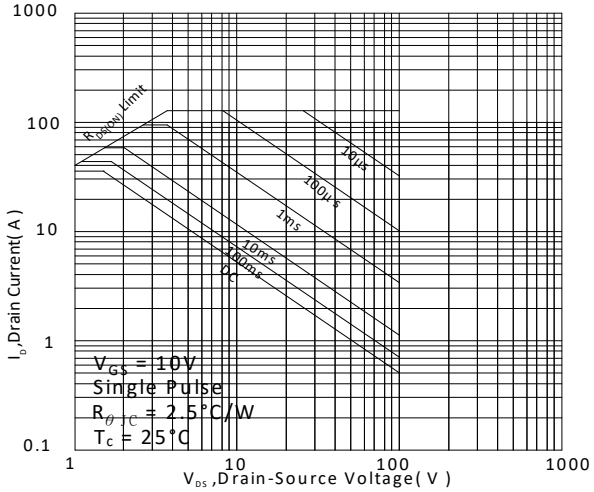
Gate Charge Characteristics



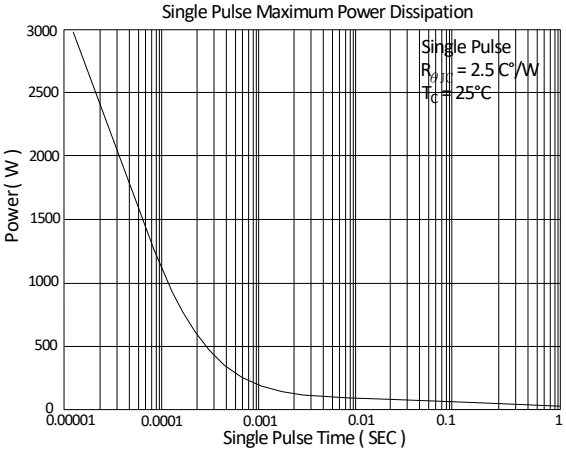
Capacitance Characteristics



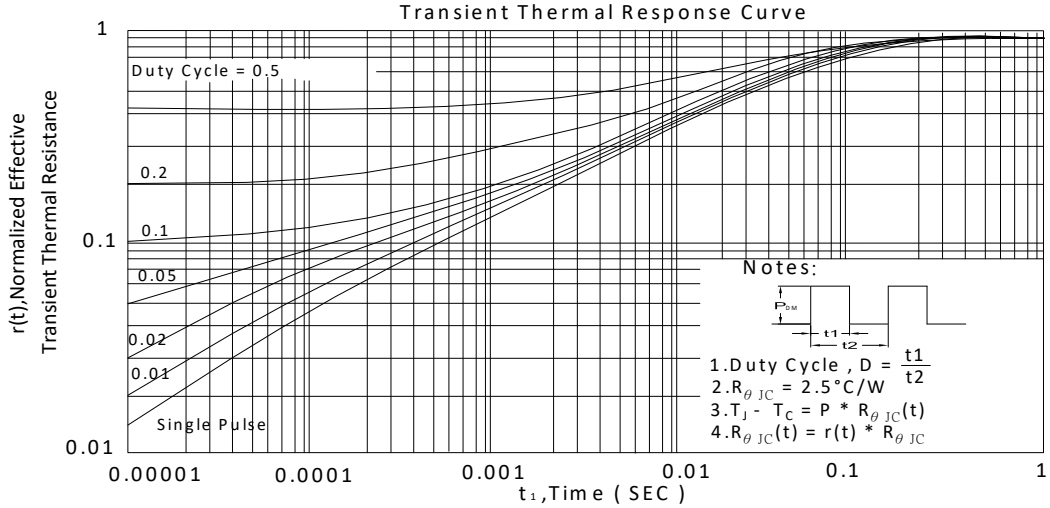
Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Ordering & Marking Information:

Device Name: EMD25N10A for DPAK (TO-252)

EMD25N10A : Device Name

ABCDEFG: Date Code

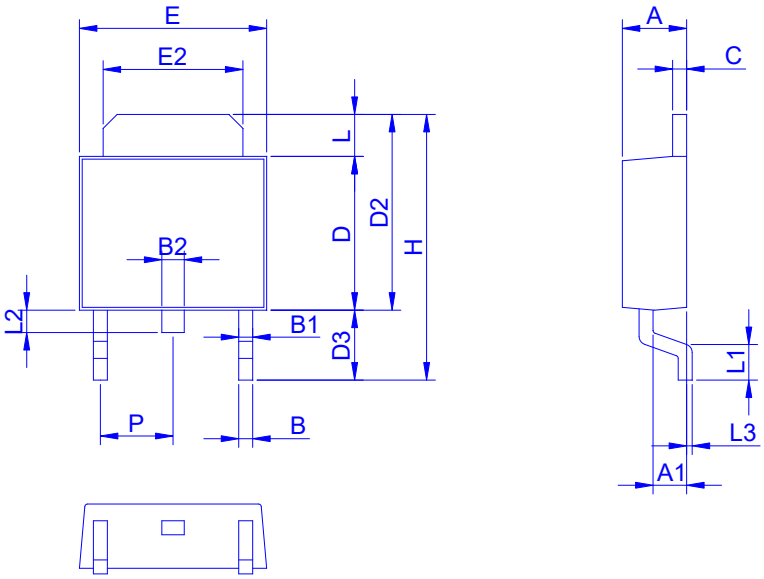
A: Assembly House

B: Year(A:2008 B:2009 C:2010….)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

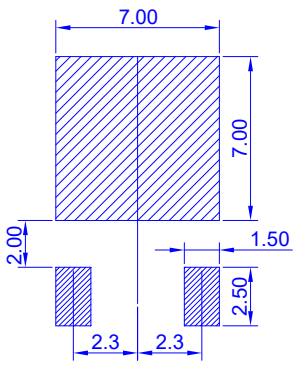
DEFG: Serial No.

Outline Drawing

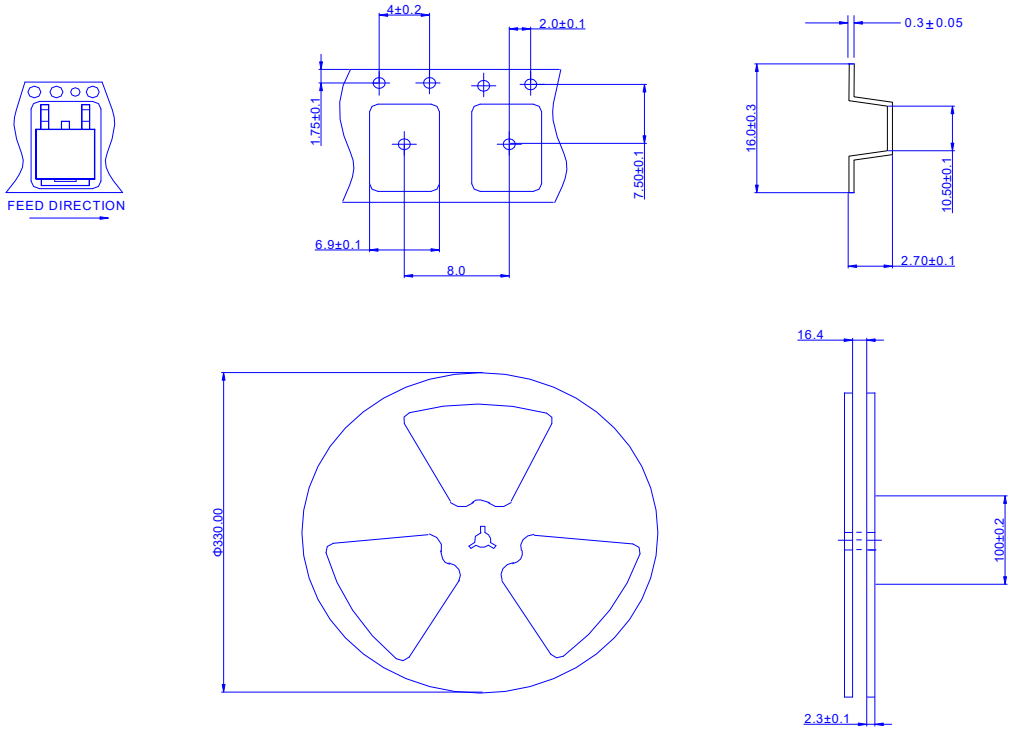


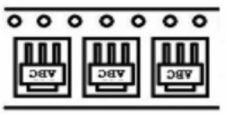
Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint



◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	TO252-2
Reel 尺寸	13”
編帶方式	FEED DIRECTION 
前空格	35
後空格	35
裝箱數	
滿捲數量	2.5K
捲/內盒比	1：1
內盒滿箱數	2.5K
內/外箱比	10：1
外箱滿箱數	25K