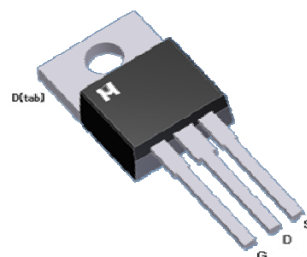
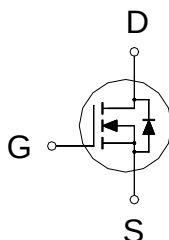


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	80V
$R_{DS(on)} (MAX.)$	7m Ω
I_D	128A



UIS, Rg 100% Tested

Pb-Free Lead Plating



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	128	A
	$T_C = 100^\circ\text{C}$		100	
Pulsed Drain Current ¹		I_{DM}	380	
Avalanche Current		I_{AS}	90	mJ
Avalanche Energy	$L = 0.1\text{mH}, I_D = 90\text{A}, R_G = 25\Omega$	E_{AS}	405	
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	202	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	227	W
	$T_C = 100^\circ\text{C}$		90	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = 40\text{V}$, $L = 0.1\text{mH}$, $V_G = 10\text{V}$, $I_L = 60\text{A}$, Rated $V_{DS} = 80\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.55	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		60	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	80			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 30V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 64V, V_{GS} = 0V$			1	μA
		$V_{DS} = 60V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	128			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 40A$		6.0	7.0	m Ω
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 40A$		50		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 40V, f = 1MHz$		3186		pF
Output Capacitance	C_{oss}			325		
Reverse Transfer Capacitance	C_{rss}			33		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.8		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 40V, V_{GS} = 10V, I_D = 40A$		36		nC
Gate-Source Charge ^{1,2}	Q_{gs}			21		
Gate-Drain Charge ^{1,2}	Q_{gd}			6.5		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 40V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		50		nS
Rise Time ^{1,2}	t_r			150		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			100		
Fall Time ^{1,2}	t_f			160		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I_S				128	A
Pulsed Current ³	I_{SM}				380	
Forward Voltage ¹	V_{SD}	$I_F = 40A, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 20A, dI_F/dt = 100A / \mu S$		90		nS
Reverse Recovery Charge	Q_{rr}			320		nC

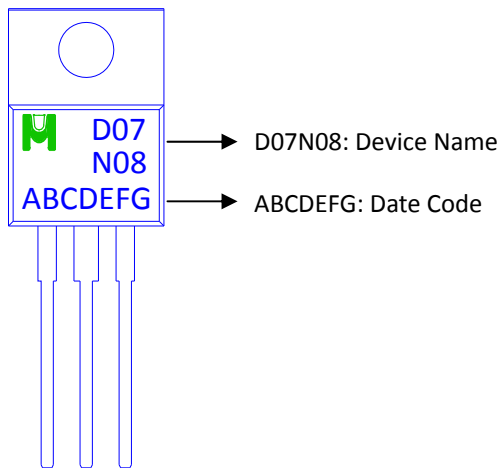
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

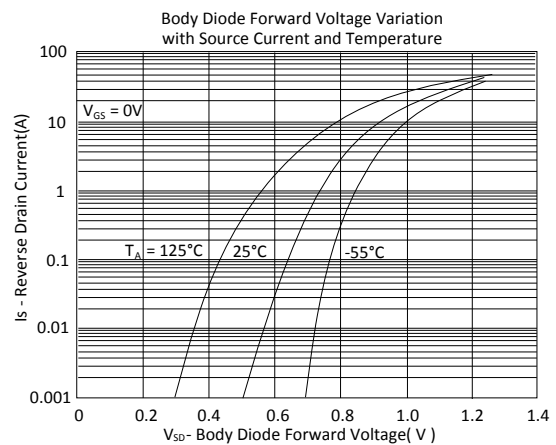
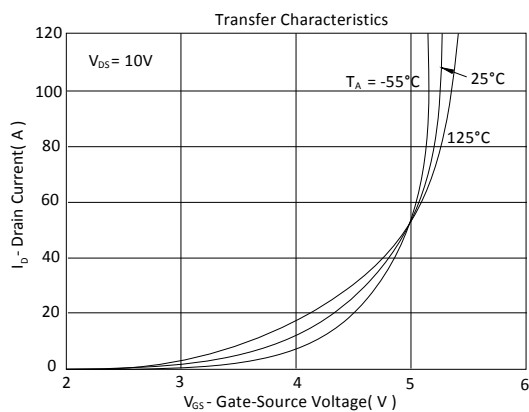
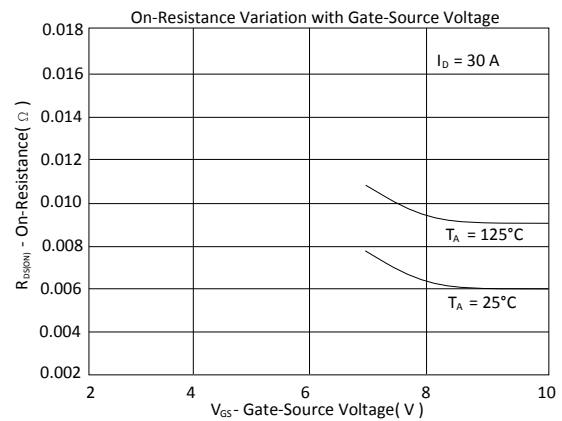
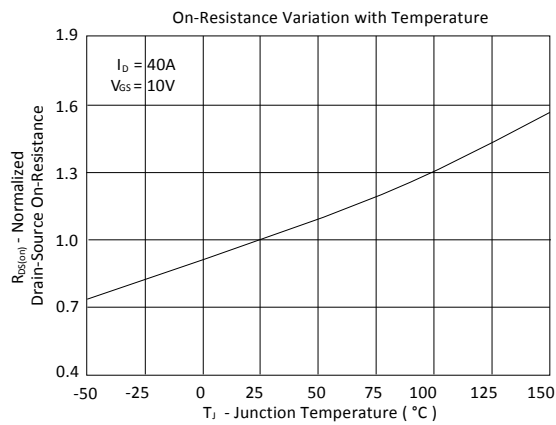
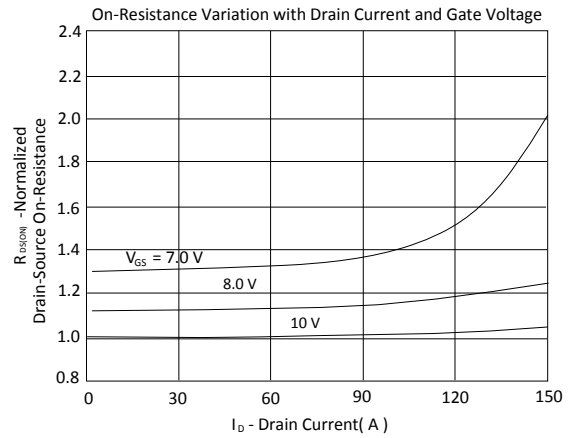
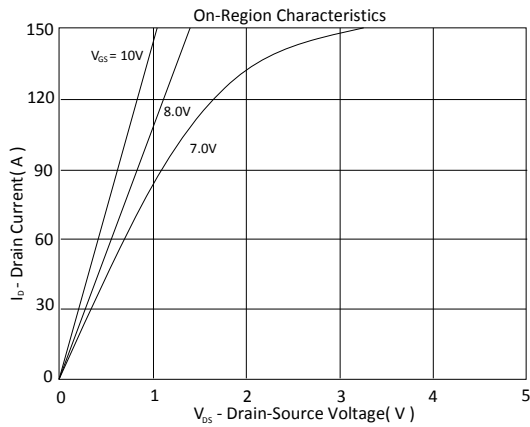
Ordering & Marking Information:

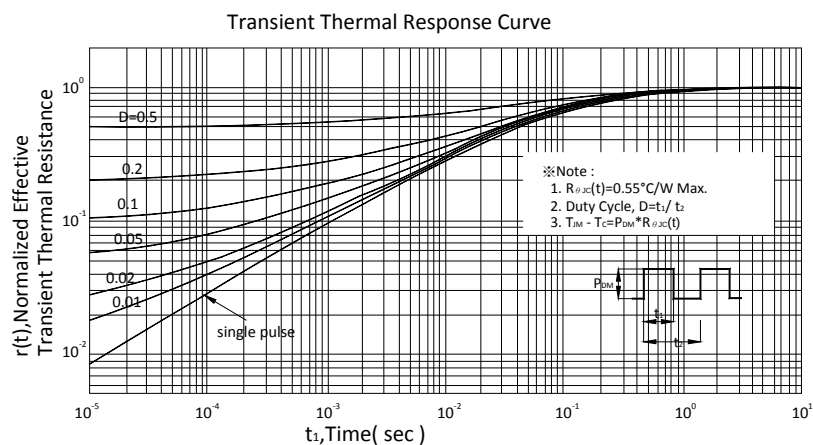
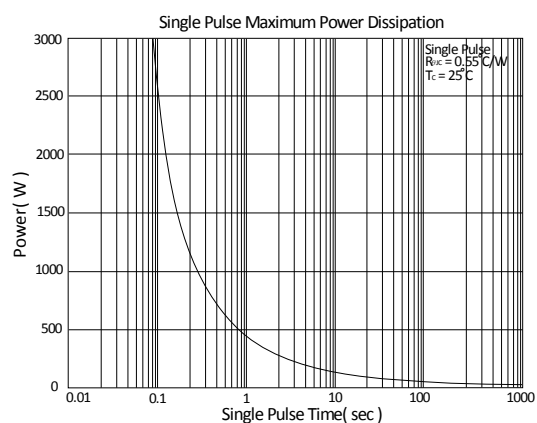
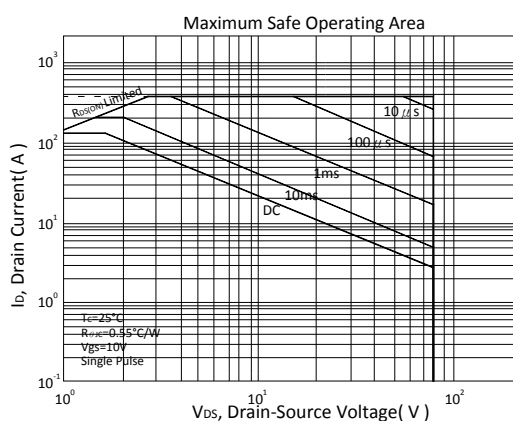
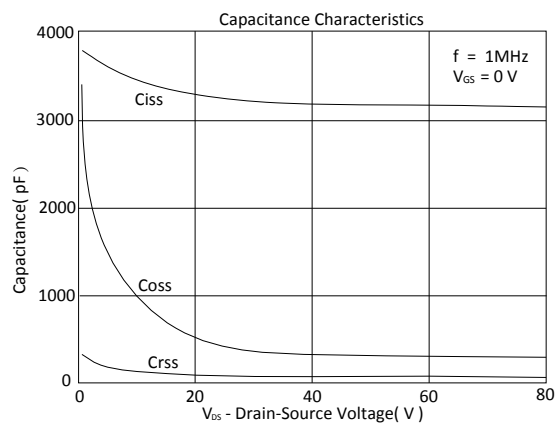
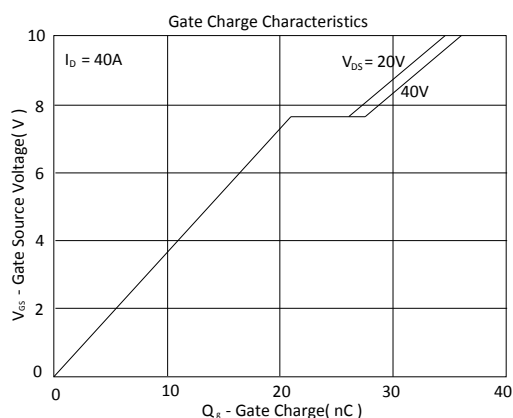
Device Name: EMD07N08E for TO-220



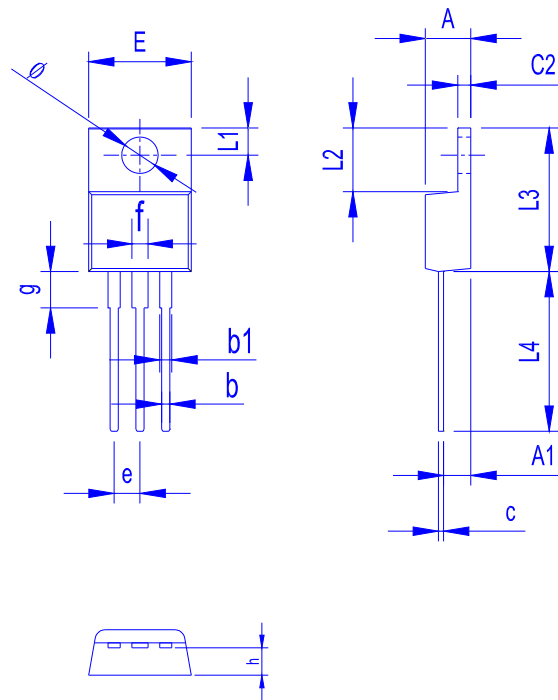


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	b	b1	c	c2	E	L1	L2	L3	L4	∅	e	f	g	h
Min.	4.20	0.70	0.90	0.30	1.10	9.80	2.55	6.10	14.80	13.50	3.40	2.35	1.30	3.40	2.40
Max.	4.80	1.10	1.50	0.70	1.50	10.50	2.85	6.50	15.40	14.50	3.80	2.75	1.90	3.80	3.00