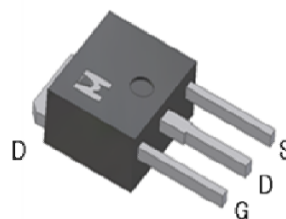
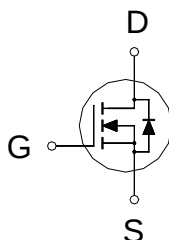


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)} (MAX.)$	12m Ω
I_D	68A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	68	A
	$T_C = 100^\circ\text{C}$		43	
Pulsed Drain Current ¹		I_{DM}	150	
Avalanche Current		I_{AS}	18	mJ
Avalanche Energy	$L = 0.1\text{mH}, I_D = 18\text{A}, R_G = 25\Omega$	E_{AS}	16.2	
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	8.1	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	89	W
	$T_C = 100^\circ\text{C}$		35	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.4	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.0		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$			1	μA	
		$V_{DS} = 70V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25		
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	68			A	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 12A$		9.5	12	m Ω	
		$V_{GS} = 4.5V, I_D = 10A$		11.5	15		
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 12A$		45		S	
DYNAMIC							
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$		2130		pF	
Output Capacitance	C_{oss}			336			
Reverse Transfer Capacitance	C_{rss}			29			
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.5		Ω	
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 50V, V_{GS} = 10V,$ $I_D = 12A$		38		nC	
	$Q_g(V_{GS}=4.5V)$			23			
Gate-Source Charge ^{1,2}	Q_{gs}			10			
Gate-Drain Charge ^{1,2}	Q_{gd}			8.2			
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 50V,$ $I_D = 12A, V_{GS} = 10V, R_{GS} = 6\Omega$		6		nS	
Rise Time ^{1,2}	t_r			10			
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			8			
Fall Time ^{1,2}	t_f			25			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)							
Continuous Current	I_S				68	A	
Pulsed Current ³	I_{SM}				150		
Forward Voltage ¹	V_{SD}	$I_F = 12A, V_{GS} = 0V$			1.2	V	
Reverse Recovery Time	t_{rr}	$I_F = 12A, dI_F/dt = 100A / \mu S$		30		nS	
Reverse Recovery Charge	Q_{rr}			130		nC	

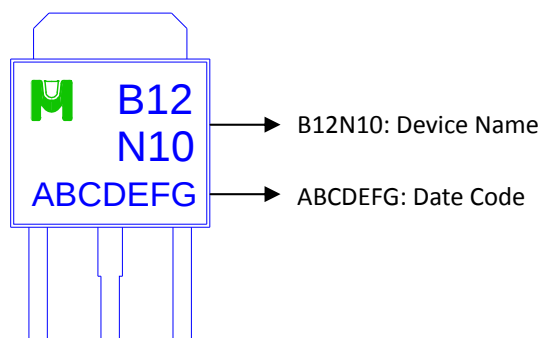
¹Pulse test : Pulse Width $\leq 300\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

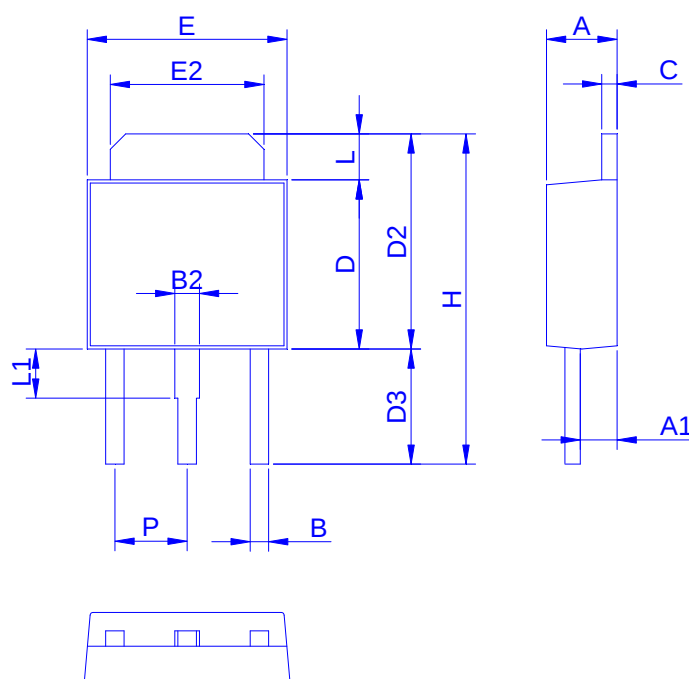
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB12N10CS for IPAK (TO-251)



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B2	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.10	0.90	0.40	0.60	0.40	5.30	6.70	3.40	6.30	4.80	10.2	0.89	0.90	2.10
Max.	2.50	1.50	0.90	1.15	0.60	6.25	7.30	4.30	6.80	5.50	11.5	1.40	1.80	2.50



TYPICAL CHARACTERISTICS

