



義隆電子股份有限公司

ELAN MICROELECTRONICS CORP.

EM78P803A

8-bit MCU

2005/8/12

Version 1.3.3

ELAN MICROELECTRONICS CORP.

No. 12, Innovation 1st RD., Science-Based Industrial Park

Hsin Chu City, Taiwan

TEL: (03) 5639977

FAX: (03) 5780617



Version History

Version	Content	Release Date
1.0	1. Initial version 2. Original Spec. is oriented from EM78805C v2.0 spec	2004/03/29
1.1	1. Modified the LCD driving waveform of 1/3 bias 2. Add internal clock source for R to F Counter 3. Add option code for supporting 16-bit counter mode	2004/05/26
1.2	1. Modified ERIC mode function 2. Modified pad assignment	2004/6/30
1.3	1. Modified the configuration of PLL 2. Modified the selection of CNT2 source 3. Fix up the bug in R to F macro 4. Modified the setup of Low Battery Detect	2004/11/30
1.3.1	1. Modified the operating voltage range	2004/12/3
1.3.3	1. Modified the table of sub frequency divider. 2. Modified the definition of R2FHR option code. 3. Modified the power consumption and reset level on POVD function (in product spec., not in target spec.) 4. Modified the definition of P803ON option code 5. Modified the product no. of 64-pin QFP	2005/8/12



User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

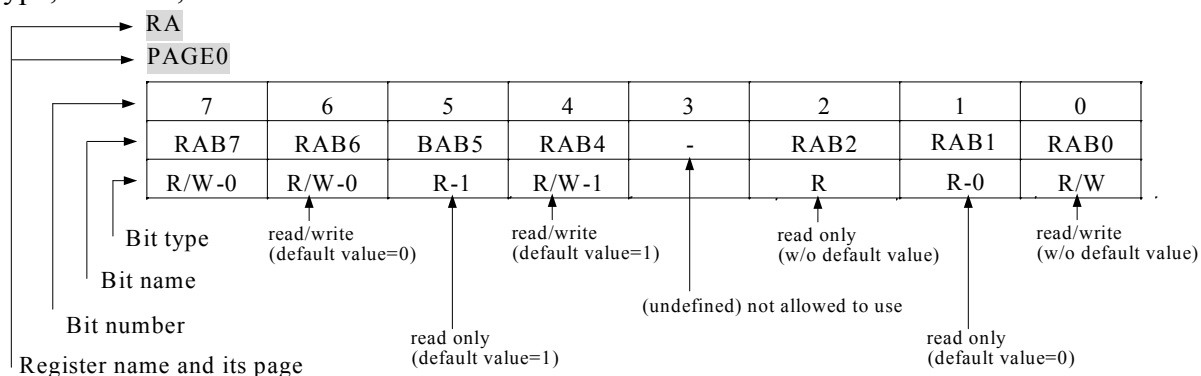
1. There are some undefined or not existent bits in the registers. For these bits, user need to take more care on them while program use them as data to execute logic or math operations. Because these bits are not relative to chip function, they never test in the factory. We use different symbols to recognize them.

“0” or “1” → value always equal to 0 or value always equal to 1, (not existent, read only)

“-” → value unknown, (not existent) undefined bits do not allow to use.

“x” → (general purpose) undefined bits do not allow to use as RAM or other data read, write or read/write.

2. You will see some names for the register bits definitions. Some name will appear very frequently in the whole spec. The following describes the meaning for the register's definitions such as bit type, bit name, bit number and so on.



3. Family Relation

Mask	ROMless	OTP
EM78805C	EM78R803	EM78P803A

4. Main Function Difference

	EM78805C	EM78P803A	EM78R803	EM78801
Type	Mask	OTP	ROMless	Mask
ROM size	12k x 13b	8k x 13b	16k x 13b	8k x 13b
Max. I/O	22	28	28	24
Main Clock	3.5826MHz x 1/8, 1/2, 1, 2	3.5826MHz x 1/2, 1, 2, 4 & ERIC mode	3.5826MHz x 1/2, 1, 2, 4 & ERIC mode	3.5826MHz x 1/2, 1, 2, 4 & ERIC mode
LCD (Max. Seg.x Com.)	24 x 8/4 1/4 Bias	28 x 8/4 1/3, 1/4 Bias	28 x 8/4 1/3, 1/4 Bias	24 x 8/4 1/3, 1/4 Bias
Tone Generator	Yes	Yes	Yes	No
DED	Yes	Yes	Yes	No
R to F Counter	No	No	Yes	Yes
16-bit counter	No	No	Yes (Pad Option)	Yes

5. Notice of ERIC Mode:

In ERIC mode, the RC oscillation circuit on the chip with an external resistor provides the system clock. There is no 32.768kHz clock because no crystal connects to the system. The sub frequency which plays the role as the same as 32.768kHz is divided from system clock. User can setup the scale factor by CODE option when downloading the program. Furthermore, to be careful to use the sub frequency clock when system working in ERIC mode. Some frequency didn't suggest might cause unpredictable condition. Please refer Sec.VII.15 for more detail

6. Common registers 0x20 ~ 0x3F only have three banks (banks 0,1,2). Notice that there is no bank 3 in these common registers. The bank 3 doesn't exist.
7. Care must be taken while programming. When R4 (bit7, bit6) = (1,1), common registers 0x10 ~ 0x1F cannot be read or written otherwise program maybe go to dead lock. ICE cannot reflect this problem. This is incompatible situation between mask and ICE.

I. Main Feature

- **Single power supply**
Operating voltage range: 2.8V ~ 5.5V(7.1652MHz)
4.5V ~ 5.5V(14.331MHz)
2.2V ~ 5.5V(3.5826MHz/ERIC mode)
2.2V ~ 5.5V(Sleep/Idle/Green mode)
- **CPU**
8-bit RISC kernel
99.9% single instruction cycle commands
- **Clock**
32.768KHz clock source
Built-in PLL to generate main clock 3.5826MHz x 0.5, 1, 2 and 4
Optional ERIC mode only with an external R
- **Timer and counter**
Watch Dog: Programmable free running on chip watchdog timer
TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler
COUNTER1: 8-bit counter with 8-bit prescaler can be an interrupt source
COUNTER2: 8-bit counter can be an interrupt source
Both of counters have reload function.
- **Memory**
8k x 13bits on chip Electrical One Time Programmable Read Only Memory (OTP-ROM)
0.5k x 8bits on-chip CID RAM
112 x 8bits common registers
- **I/O**
Up to 28 bi-directional tri-state I/O ports (18 independent I/O)
IO with internal Pull high, wake-up and interrupt functions
- **Operation mode**
Four modes can be selected. (Main clock is generated by internal PLL.)

Mode	CPU status	Main clock	32.768 kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Idle mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on
- **Interrupt**
Selective signal sources and overflow interrupt
STACK: 8 levels stack for subroutine nesting
8 interrupt source, 5 external, 3 internal
- **Reset**
Power on reset, /POVD reset (by PAD option) or external /RESET pin
- **Programmable Tone Generators**
Programmable Tone1 and Tone2 generators
Independent single tone generation for Tone1 and Tone2
Mixed dual tone generation by Tone1 and Tone2 with 2dB difference
Can be programmed for DTMF tone generation
- **DED**
Differential-input Energy Detector (DED) for line energy detection
- **LCD**
LCD operation voltage chosen by software
Common driver pins: 8/4
Segment driver pins: 28
1/3 bias or 1/4 bias with output buffer

1/4 duty or 1/8 duty

■ **PACKAGE**

64-pad die (EM78P803AH)

100-pin QFP (EM78P803AQ)

64-pin QFP:

Name	/POVD	ERICen
EM78P803AAAQ	Disable (H)	Disable (L)
EM78P803AABQ	Disable (H)	Enable (H)
EM78P803AB AQ	Enable (L)	Disable (L)
EM78P803ABBQ	Enable (L)	Enable (H)

II. General Description

This is an 8-bit CID (Call Identification) RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on-chip watchdog (WDT), RAM, OTP-ROM, programmable real time clock /counter, internal interrupt, power down mode, LCD driver, Energy Detector (DED) or Low Batter Comparator and tri-state I/O. It provides a single chip solution for versatile and general-purpose application use.

III. Application

Caller ID adjunct box or phone units for FSK/DTMF CID dual system development and general-purpose application.

IV. Pin Configuration

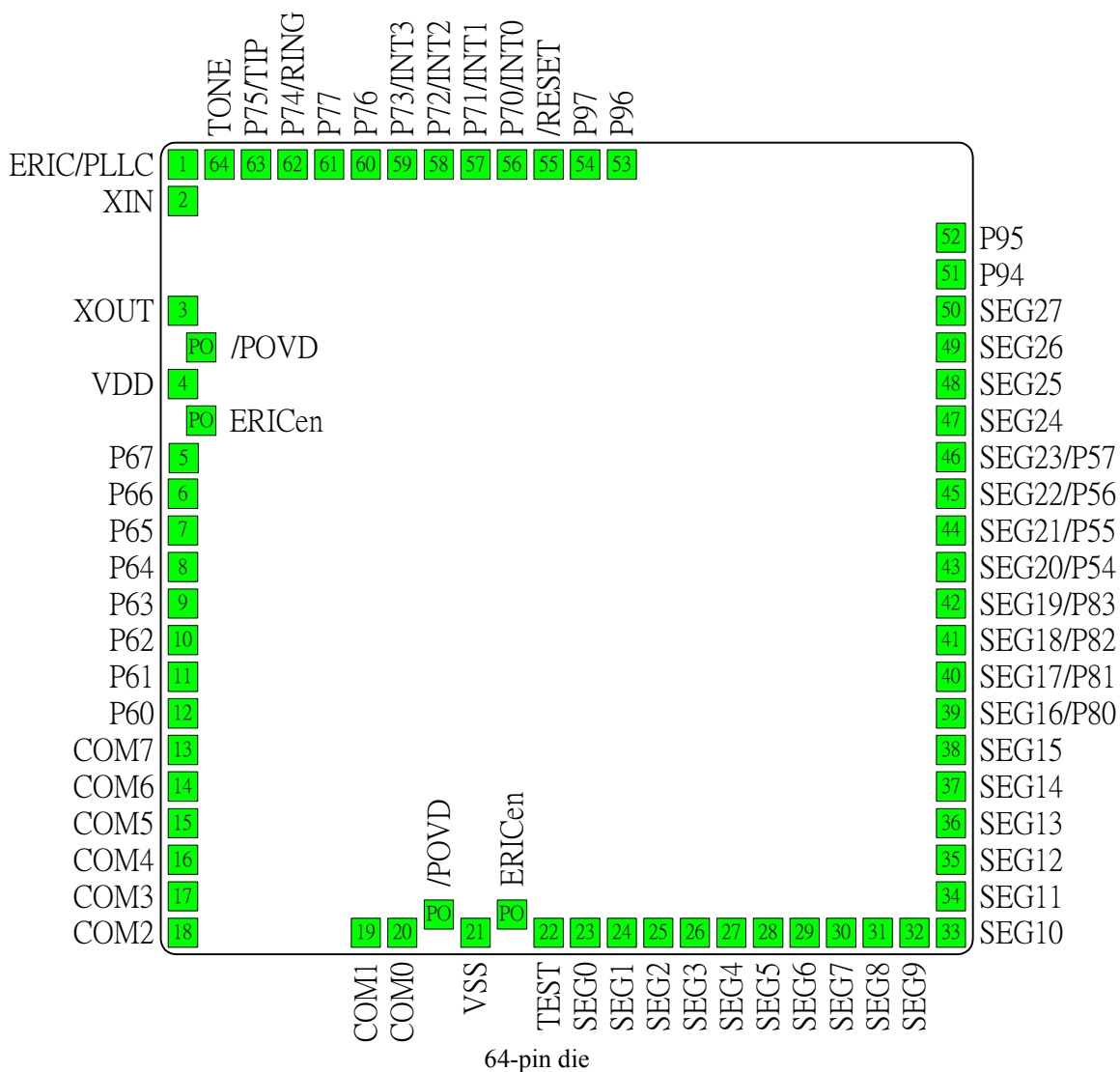


Fig.1 Pad assignment

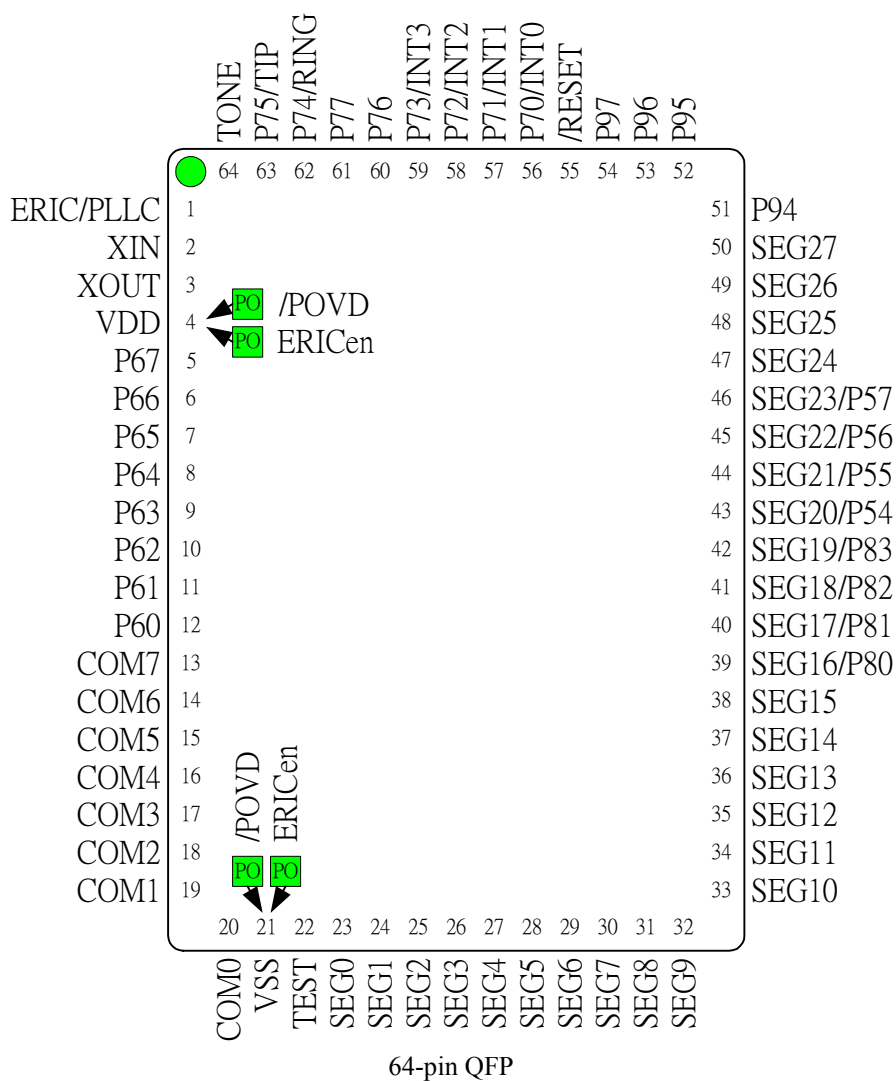
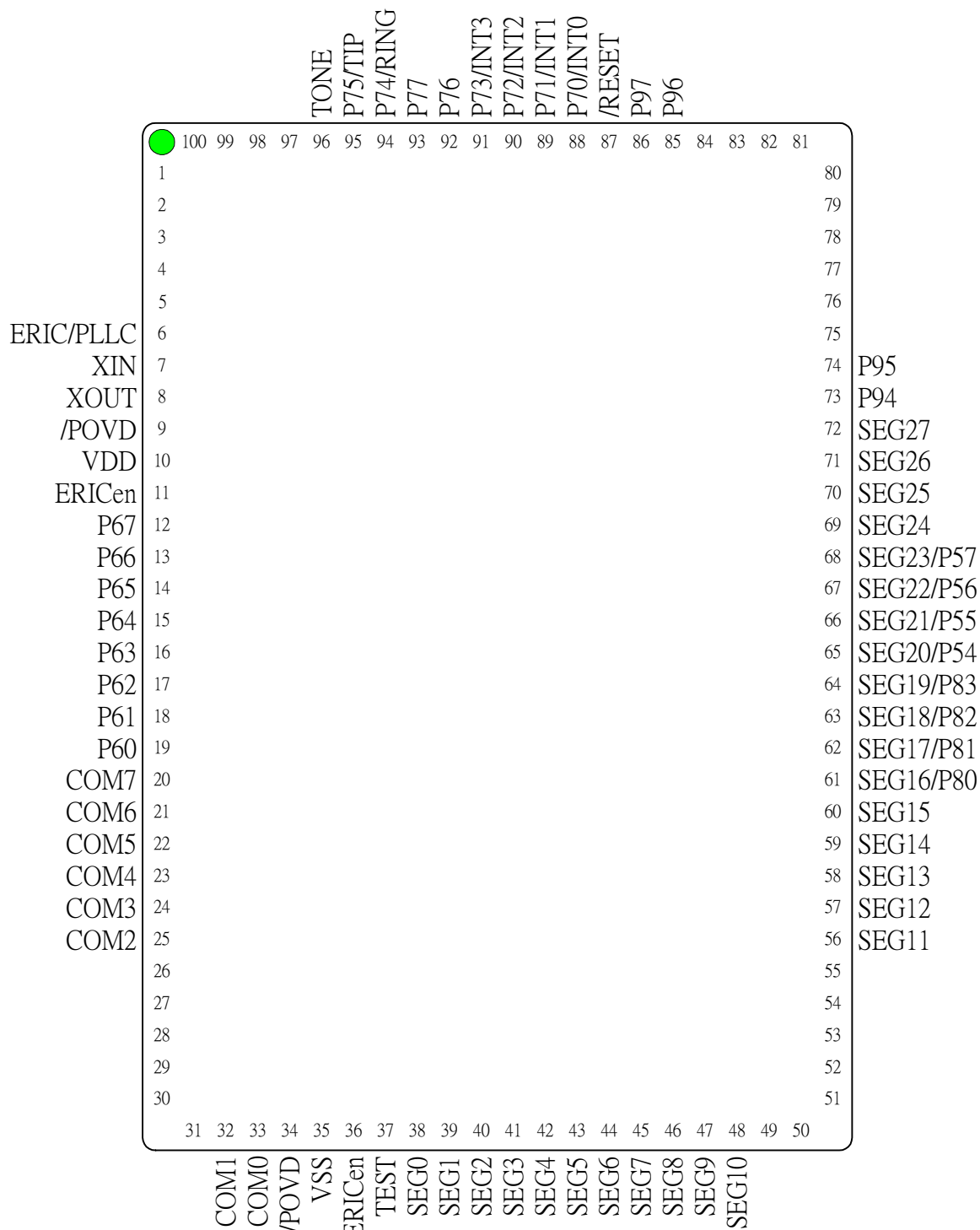


Fig.1 Pad assignment (Continued)



100-pin QFP
Other Pins without name are NC

Fig.1 Pad assignment (Continued)

The diagram illustrates the internal architecture of the AT89C51 microcontroller. A central vertical bar represents the internal bus. On the left side, connected to the bus, are the CPU, TIMING CONTROL, TIMER TCC, COUNTER1, COUNTER2, WDT, and Program ROM. On the right side, connected to the bus, are the DATA RAM, CONTROL REGISTER, LCD DRIVER, I/O PORT, and Energy Detector (DED) Programming tone gen. Bidirectional arrows indicate communication between the CPU and the bus, and between the bus and the other components. Unidirectional arrows show data flow from the LCD DRIVER and I/O PORT to the bus.

```
graph LR
    CPU[CPU] <--> Bus
    Timing[TIMING CONTROL] <--> Bus
    Timer[TIMER TCC  
COUNTER1  
COUNTER2  
WDT] <--> Bus
    ROM[Program ROM] <--> Bus
    Bus <--> DataRAM[DATA RAM  
CONTROL REGISTER]
    Bus <--> LCD[LCD DRIVER]
    Bus <--> IO[I/O PORT]
    Bus <--> DED[Energy Detector (DED)  
Programming tone gen.]
```

The diagram illustrates the internal architecture of the AT89C52 microcontroller. At the top, external pins XIN, XOUT, PLLC, and ERIC are connected to the Oscillator timing control block. A WDT timer is connected to a Prescaler, which in turn connects to the Oscillator timing control and the R1(TCC) register. The Oscillator timing control is bidirectionally connected to the Prescaler and the Control sleep and wakeup on I/O port block. The Control sleep and wakeup block is connected to the DATA RAM and the DATA & Control Bus. The Prescaler is also connected to the General RAM, which is further connected to the R4 register. The R1(TCC) register is connected to the DATA & Control Bus. The General RAM is connected to the R4 register. The WDT timer is connected to the Prescaler. The ROM is connected to the Instruction register, which is also connected to the Interrupt control block. The Instruction register is connected to the Instruction decoder, which is connected to the R2 register. The R2 register is connected to the STACK and the ALU. The ALU is connected to the R3 and R5 registers, which are also connected to the ACC register. The ACC register is connected to the ALU. The DATA & Control Bus is a central horizontal bar that connects all major components. Below the bus, there are five I/O blocks: DED Prog. tone gen. (connected to TIP, RING), LCD RAM and LCD driver (connected to COM0~COM7, SEG0~SEG7), and three I/O blocks (IOC5, R5, PORT5; IOC6, R6, PORT6; IOC7, R7, PORT7; IOC8, R8, PORT8; IOC9, R9, PORT9) connected to P54~P57, P60~P67, P70~P77, P80~P83, and P94~P97 respectively.

2005/8/12 V1.3.3

VI. Pin Descriptions

Pin	I/O	Description	Num
Power			
VDD	POWER	Chip power VDD	1
VSS	GROUND	Chip ground GND	1
Clock for MCU			
XIN	I	Input pin for 32.768kHz crystal	1
XOUT	O	Output pin for 32.768kHz crystal	1
PLLC	I	Phase locked loop capacitor, connect a capacitor 0.01u to 0.047u to the ground.	1
ERIC	I	Connect to VDD with a resister serially when in ERIC mode. This pin is shared with PLLC	1
LCD driver			
COM0..COM7	O	Common driver pins of LCD drivers	8
SEG0..SEG15 SEG24..SEG27	O	Segment driver pins of LCD drivers	20
SEG16..SEG19	O (PORT8)	Segment driver pins of LCD drivers Shared with P80 ~ P83	4
SEG20..SEG23	O (PORT5)	Segment driver pins of LCD drivers Shared with P54 ~ P57	4
DTMF			
TONE	O	Programming tone generator output	1
DED			
TIP	I (PORT75)	Differential-input Energy Detector input pin. It is non-polarity pin Shared with P75. It can be used as positive input of low battery comparator.	1
RING	I (PORT74)	Differential-input Energy Detector input pin. It is non-polarity pin Shared with P74 It can be used as negative input of low battery comparator.	1
Test			
TEST	I	Test pin into test mode, normal low	1
Reset			
/RESET	I	Reset input. Low enable	1
I/O			
P54 ~P57	I/O PORT5	PORT5 can be INPUT or OUTPUT port each bit And P54 ~ P57 are shared with segment signal	4
P60 ~P67	I/O PORT6	PORT6 can be INPUT or OUTPUT port each bit P66, P67 and P65 have open drain function	8
P70 ~P77	I/O PORT7	PORT7 can be INPUT or OUTPUT port each bit PORT7 have internal pull high function P70/INT0 ~ P73/INT3 can be interrupt signals P75, P74 is shared with TIP and RING	8
P80 ~ P83	I/O PORT8	PORT 8 can be INPUT or OUTPUT port each bit And P80 ~ P83 are shared with segment signal.	4
P94 ~ P97	I/O PORT9	PORT 9 can be INPUT or OUTPUT port each bit P96, P97 have wake-up function.	4
PAD Option			
/POVD	I	Power on voltage detector reset	2
ERICen	I	ERIC mode enable	2

When /RESET pulls to 12V, the system will be in programming mode. Then writer can program the code ROM inside the system.

No.	System Pin Name	OTP writer Pin Name	Description
4	VDD	VDD	VDD power
55	/RESET	VPP	High voltage activation pin
61	P7[7]	DINCK	Internal ssyetm clock
60	P7[6]	ACLK	External system clock
63	P7[5]	PGMB	When PGMB=0, writing action of OTP ROM activates
62	P7[4]	OEB	When OE=0, reading action of OTP ROM activates.
59	P7[3]	DATA	Serial data I/O
21	VSS	GND	Ground power

VII. Functional Descriptions

VII.1 Operational Registers

Register configuration 1:

Addr	R PAGE registers	IOC PAGE	
		IOC PAGE0	IOC PAGE1
00	INDA Indirect addressing		
01	TCCD TCC data		
02	PC Program counter		
03	STA IOC Page, Tone 1, 2 power control, Status		
04	RBSR Register bank, RSR		
05	P5IOD PORT5 I/O data, Program ROM page	P5IOC PORT5 I/O control,	
06	P6IOD PORT6 I/O data	P6IOC PORT6 I/O control	
07	P7IOD PORT7 I/O data	P7IOC PORT7 I/O control	
08	P8IOD PORT8 I/O date	P8IOC PORT8 I/O control	
09	P9IOD PORT9 I/O data	P9IOC PORT9 I/O control	
0A	MCUC CPU power saving, PLL, Main clock selection	PSW (P8 low nibble, P5) switch, LCD bias, Key scan control	DEDC LCD power saving, Low battery detect, DED control
0B	DEDO Green tone, DED output, CID RAM bank	LCDA LCD RAM address	CN1D Counter 1 data
0C	RAMA CID RAM address	LCDD LCD RAM data	CN2D Counter 2 data
0D	RAMD CID RAM data	TONE1C TONE1 control	P7PHC PORT7 pull high
0E	WUPC Wake-up control, LCD control	TONE2C TONE2 control	CNPSC Open Drain Control, CNT1,2 CLK source, CNT1,2 prescaler, LCD mode
0F	INTF Interrupt flag	INTM Interrupt mask	
10 : 1F	16 bytes Common registers		
20 : 3F	Bank0~Bank2 ² Common registers (32x8 for each bank)		

Ps. 1. Register 20~3F has bank0~bank2 only. The bank3 doesn't exist and cannot access it.

Register Configuration 2:

Addr.	R page	IOC page	Register Name	Register bit name								Power on Reset val.
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00	x		INDA	(Indirect address register)								
01	x		TCCD	(TCC data buffer)								
02	x		PC	(Program counter)								
03	x		STA	IOCPAGE	P_TONE2	P_TONE1	T	P	Z	DC	C	000xxxxx
04	x		RBSR	RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	00xxxxxx
05	x		P5IOD	P57	P56	P55	P54	PS3	PS2	PS1	PS0	xxxx0000
		0	P5IOC	IOC57	IOC56	IOC55	IOC54	0	0	0	0	11110000
		1	(non-existence)	0	0	0	0	0	0	0	0	00000000
06	x		P6IOD	P67	P66	P65	P64	P63	P62	P61	P60	xxxxxxxx
		0	P6IOC	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60	11111111
		1	(non-existence)	0	0	0	0	0	0	0	0	00000000
07	x		P7IOD	P77	P76	P75	P74	P73	P72	P71	P70	xxxxxxxx
		0	P7IOC	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70	11111111
		1	(non-existence)	0	0	0	0	0	0	0	0	00000000
08	x		P8IOD	0	0	0	0	P83	P82	P81	P80	0000xxxx
		0	P8IOC	0	0	0	0	IOC83	IOC82	IOC81	IOC80	00001111
		1	(non-existence)	0	0	0	0	0	0	0	0	00000000
09	x		P9IOD	P97	P96	P95	P94	0	0	0	0	xxxx0000
		0	P9IOC	IOC97	IOC96	IOC95	IOC94	0	0	0	0	11110000
		1	(non-existence)	0	0	0	0	0	0	0	0	00000000
0A	x		MCUC	IDLE	ENPLL	CLK2	CLK1	0	0	0	0	00000000
		0	PSW	BIASS	0	P8SL	P5S	BIAS3	BIAS2	BIAS1	SC	00000000
		1	DEDC	0	4CDR	8CR	Low_BAT	LPD	EGCLK	DEDPWR	DEDTHTD	000x0000
0B	x		DEDO	EDGE	GTONE	0	0	DEDD	0	0	CALL_1	0000x000
		0	LCDA	0	0	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0	00000000
		1	CN1D	CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10	00000000
0C	x		RAMA	CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0	00000000
		0	LCDD	LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0	xxxxxxxx
		1	CN2D	CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20	00000000
0D	x		RAMD	CIDD7	CIDD6	CIDD5	CIDD4	CIDD3	CIDD2	CIDD1	CIDD0	xxxxxxxx
		0	TONE1C	T17	T16	T15	T14	T13	T12	T11	T10	00000000
		1	P7PHC	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	00000000
0E	x		WUPC	0	/WDTE	/WUP97	/WUP96	0	LCD_C2	LCD_C1	/WUEDD	00000000
		0	TONE2C	T27	T26	T25	T24	T23	T22	T21	T20	00000000
		1	CNPSC	OP77	OP76	C2S	C1S	PSC2	PSC1	PSC0	LCDM	00000000
0F	x		INTF	EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF	00000000
		0	INTM	EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF	00000000
		1	(non-existence)	0	0	0	0	0	0	0	0	00000000

VII.2 Operational Register Detail Description

R0 (INDA: Indirect addressing register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

R1 (TCCD: TCC data buffer)

Increased by an external signal edge applied to TCC, or by the instruction cycle clock. Written and read by the program as any other register. TCC has no reload function.

R2 (PC: Program counter)

The structure is depicted in Fig.4

Generates $8k \times 13$ bit internal ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then pushes into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

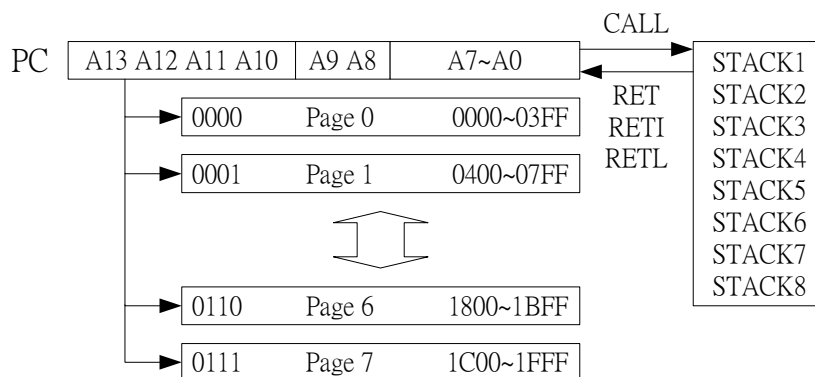


Fig.4 Program counter organization

R3 (STA: IOC Page, Tone1, 2 power control, Status register)

7	6	5	4	3	2	1	0
PAGE	P_TONE2	P_TONE1	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R-x	R-x	R/W-x	R/W-x	R/W-x

Bit 0 (C) : Carry flag

Bit 1 (DC) : Auxiliary carry flag

Bit 2 (Z) : Zero flag

Bit 3 (P) : Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) : Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	x	x : don't care

Bit 5 (P_TONE1) : Power control bit of Tone generator 1

User can use this bit to power on the tone generator 1

Bit 6 (P_TONE2) : Power control bit of Tone generator 2

User can use this bit to power on the tone generator 2

Ps. Tone frequency is controlled by IOCD and IOCE.

R3(6,5)	Tone Generator 2	Tone Generator 1
00	Power off	Power off
01	Power off	Power on
10	Power on	Power off
11	Power on	Power on

Bit 7 (PAGE) : change IOCB ~ IOCE to another Page

0/1 → PAGE0/PAGE1

R4 (RBSR: RAM bank, RAM selection for common registers R20 ~ R3F)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 3 banks for 32 registers (R20 to R3F). *The bank 3 doesn't exist and cannot access.*

(RB1, RB0)	Bank # for R20 ~ R3F
00	Bank 0
01	Bank 1
10	Bank 2
11	N/A

R5 (P5IOD: PORT5 I/O data, Program ROM page selection)

7	6	5	4	3	2	1	0
P57	P56	P55	P54	PS3	PS2	PS1	PS0
R/W	R/W	R/W	R/W	R-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 3 (PS0 ~ PS3) : Page selection bits

They should be set before JMP or CALL instruction.

Page select bits

PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
:	:	:	:	:
:	:	:	:	:
0	1	1	0	Page 6
0	1	1	1	Page 7

User can use PAGE instruction to change page and maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. EMC's compiler maintains the program page. It will change user's program by inserting instructions within program.

Bit 3 is always 0 and can't be set.

Bit 5 ~ 7 (P54 ~ P57) : 4-bit PORT5(4 ~ 7) I/O data register

R6 (P6IOD: PORT6 I/O data)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P60 ~ P67) : 8-bit PORT6(0~7) I/O data register

User can use IOC register to define input or output each bit.

R7 (P7IOD: PORT7 I/O data)

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P70 ~ P77) : 8-bit PORT7(0~7) I/O data register

User can use IOC register to define input or output each bit.

P74~P75 are shared with TIP and RING. When the bit DEDPWR is set, P74~P75 must be set as input port. Otherwise, P74~P75 and DED function will collide and not work as normal.

R8 (P8IOD: PORT8 I/O data)

7	6	5	4	3	2	1	0
0	0	0	0	P83	P82	P81	P80
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (P80 ~ P83) : 4-bit PORT8(0~3) I/O data register

Bit 4 ~ Bit 7 : unused

User can use IOC register to define input or output each bit.

R9 (P9IOD: PORT9 I/O data)

7	6	5	4	3	2	1	0
P97	P96	P95	P94	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0

Bit 0 ~ Bit 3 : unused

Bit 4 ~ Bit 7 (P94 ~ P97) : 4-bit PORT9(4~7) I/O data register

User can use IOC register to define input or output each bit.

RA (MCUC: CPU power saving, PLL, Main clock selection)

7	6	5	4	3	2	1	0
IDLE	ENPLL	CLK2	CLK1	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0

Bit 0 ~ Bit 3 : unused

Bit 4 ~ 5 (CLK1 ~ CLK2) : Main clock selection bits.

User can choose the main clock by setting CLK1 and CLK2. All the clock selections are list below. Please notice that the configuration of main clock is different in P803 mode and 805C mode. When changing the main clock, insert some NOP instruction for system stability.

ENPLL	CPU's clock		(CLK2,CLK1)	MAIN clock	
	P803A	805C		P803A	805C
0	32.768kHz	32.768kHz	(x,x)	x	x
1	1.7913MHz	447.8293kHz	(0,0)	1.7913MHz	447.8293kHz
1	14.331MHz	895.6587kHz	(0,1)	14.331MHz	895.6587kHz
1	7.1652MHz	7.1653MHz	(1,0)	7.1652MHz	7.1653MHz
1	3.5826MHz	3.5826MHz	(1,1)	3.5826MHz	3.5826MHz

When in ERIC mode, CLK1~2 will be masked. The main clock is generated by the frequency of ERIC oscillation.

Bit 6 (ENPLL) : (read/write) PLL enable/disable control

1/0 → enable/disable

The relation between 32.768kHz and main clock can see Fig.5

When in ERIC mode, ENPLL will enforce to 0. The main clock is generated by the frequency of ERIC oscillation. The sub clock is divided from the main clock and can be scale by different factor.

Bit 7 (IDLE) : Idle mode/sleep mode selection bit

1/0 → Idle mode/sleep mode.

This bit will decide SLEP instruction which mode to go.

These two modes can be waked up by TCC clock, Watch Dog timer (WDT), PORT96~97, Energy Detector output, PORT70~73 and run from "SLEP" next instruction.

P70 ~ P73 's wakeup function is controlled by IOCF P0(1,2,3) and ENI instruction.

P70 's wakeup signal is a rising edge or falling edge defined by CONT REGISTER bit7.

Port96, Port97, Port71, Port72 and Port73 's wake-up pattern is a falling edge-triggering signal.

Energy Detector wakeup and interrupt signal can be controlled by RB bit 7 (EDGE).

Wakeup signal	SLEEP mode	IDLE mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) +SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) No SLEP	RA(7,6)=(x,1) No SLEP
TCC time out, EDD	x	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	RESET	Wake-up + Next instruction	RESET	RESET
Port96, 97	RESET	Wake-up + Next instruction	x	x
PORT70~73	RESET	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt

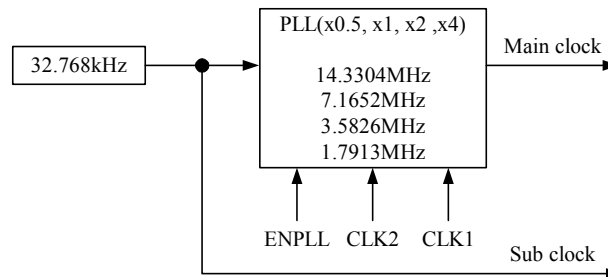


Fig.5 The relation between 32.768kHz and Main clock

RB (DEDO: Green tone, DED output, CID RAM banks)

7	6	5	4	3	2	1	0
EDGE	GTONE	0	0	DEDD	0	0	CALL 1
R/W-0	R/W-0	R-0	R-0	R-x	R-0	R-0	R/W-0

Bit 0 (CALL 1) : 2 blocks of CALLER ID RAM area

User can use 0.5K CID RAM with RC RAM address.

Bit 1 ~ 2 = 0 : unused

Bit 3 (DEDD) : Output data of Energy Detector (DED)

If input signal from TIP pin and RING pin to Energy Detector is over the threshold level setting at IOCA PAGE1 bit 0(DEDTHTD), the DED will extract the zero-crossing pulse waveform corresponding to input signal.

Bit 4 ~ Bit 5 : unused

Bit 6 (GTONE) : Green tone for programming tone generator

0/1 → disable/enable green tone function

When this function is enabled, either R3 bit5(P_TONE1) or R3 bit6(P_TONE2) is set then PLL is auto-on. At this time, TONE1 or TONE2 can be used no matter what MCU works on 32.768kHz or normal mode. When this function is disabled, TONE1 or TONE2 can only work on normal mode.

Bit 7 (EDGE) : Wake-up and interrupt triggering edge control of Energy Detector output

0/1 → Falling edge trig. / Rising edge & Falling edge trig.

RC (RAMA: CID RAM address)

7	6	5	4	3	2	1	0
CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CIDA0 ~ CIDA7) : CID RAM address

User can select Caller ID RAM address from 0 to 255.

RD (RAMD: CID RAM data buffer)

7	6	5	4	3	2	1	0
CIDD7	CIDD6	CIDD5	CIDD4	CIDD3	CIDD2	CIDD1	CIDD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CIDD0 ~ CIDD7) : CID RAM data register.

RE (WUPC: Wake-up control, LCD control)

7	6	5	4	3	2	1	0
0	/WDTE	/WUP97	/WUP96	0	LCD_C2	LCD_C1	/WUEDD
R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

Bit 0 (/WUEDD) : Wake-up control of Energy Detector (DED) output data

1/0 → enable/disable

Bit 1 ~ Bit 2 (LCD_C1 ~ LCD_C2) : LCD display enable or blanking.

The display duty change must set the (LCD_C2,LCD_C1) to (0,0).

(LCD_C2,LCD_C1)	LCD Display Control	Duty	Bias
(0,0)	Disable (turn off LCD)	(*1) (*1)	1/4 1/4
(0,1)	Blanking	:	:
(1,1)	LCD display enable	:	:

*1. 1/8 or 1/4 duty depends on IOCE PAGE1 bit0 (LCDM)

Bit 3 : unused

Bit 4 (/WUP96) : PORT9 bit6 wake-up control, 1/0 → enable/disable

Bit 5 (/WUP97) : PORT9 bit7 wake-up control, 1/0 → enable/disable

Bit 6 (/WDTE) : Watchdog timer enable control, 1/0 → enable/disable

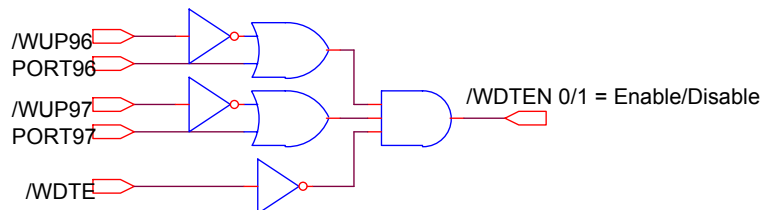


Fig.6 Wake up function and control signal

Bit 7 : unused

RF (INTF: Interrupt status register)

7	6	5	4	3	2	1	0
EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (TCIF) : TCC timer overflow interrupt flag

It will be set when TCC timer is overflow.

Bit 1 (INT0) : External INT0 pin interrupt flag

It can be used when PORT70 is set to input port.

Bit 2 (INT1) : External INT1 pin interrupt flag

It can be used when PORT71 is set to input port.

Bit 3 (INT2/INT3) : external INT2 and INT3 pin interrupt flag

It can be used when PORT72 or PORT73 is set to input port.

Bit 4 (CNT1) : 8 bit Counter1 overflow interrupt flag.

It will be set when Counter1 is overflow.

Bit 5 (CNT2) : 8 bit Counter2 overflow interrupt flag.

It will be set when Counter2 is overflow.

Bit 6 : unused

Bit 7 (EDD) : Interrupt flag of Energy Detector (DED) output data

"1" means interrupt request and "0" means non-interrupt. INT0~INT3 interrupts are edge triggering (falling edge or rising edge) which can be set by CONT bit 7 (INT_EDGE). Interrupt edge control of DED output data is set by RB bit 7(EDGE). Also see corresponding interrupt mask in IOCF register. User can read and clear.

R10~R3F (General Purpose Register)

R10~R1F : common registers

Care must be taken while programming. When R4 (bit7,bit6) = (1,1), common registers 0x10 ~ 0x1F cannot be read or written otherwise program maybe go to dead lock. ICE cannot reflect this problem. This is incompatible situation between mask and ICE.

R20~R3F (Banks 0~2) : common registers

These common are bank-controlled registers with bank 0,1,2. The bank 3 doesn't exist and cannot access.

VII.3 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
INT_EDGE	INT	TS	0	PAB	PSR2	PSR1	PSR0
R/W-1	R/W-0	R/W-1	R-0	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 → TCC/WDT

Bit 4 : unused

Bit 5(TS) : TCC signal source

0 → Instruction clock

1 → 16.384kHz

Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See Fig.5.

In ERIC mode, the instruction clock is the half of frequency of ERIC oscillation. When TS bit sets 1, the clock is the half of sub frequency divided from the frequency of ERIC oscillation.

Bit 6 (INT) : INT enable flag

0 → Interrupt masked by DISI or hardware interrupt

1 → Interrupt enabled by ENI/RETI instructions

Bit 7(INT_EDGE) : interrupt edge type of P70

0 → P70 's interruption source is a rising edge signal and falling edge signal.

1 → P70 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

IOC5 (P5IOC: PORT5 I/O control)

7	6	5	4	3	2	1	0
IOC57	IOC56	IOC55	IOC54	0	0	0	0
R/W-1	R/W-1	R/W-1	R/W-1	R-0	R-0	R-0	R-0

Bit 0 ~ Bit 3 : unused

Bit 4 ~ 7 (IOC54 ~ IOC57) : PORT5(4~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

IOC6 (P6IOC: PORT6 I/O control)

7	6	5	4	3	2	1	0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC60 ~ IOC67) : PORT6(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

IOC7 (P7IOC: PORT7 I/O control)

7	6	5	4	3	2	1	0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC70 ~ IOC77) : PORT7(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

P74~P75 are shared with TIP and RING. When the bit DEDPWR is set, P74~P75 must be set as input port.

Otherwise, P74~P75 and DED function will collide and not work as normal.

IOC8 (P8IOC: PORT8 I/O control)

7	6	5	4	3	2	1	0
0	0	0	0	IOC83	IOC82	IOC81	IOC80
R-0	R-0	R-0	R-0	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 3 (IOC80 ~ IOC83) : PORT8(0~3) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

Bit 4 ~ Bit 7 : unused

IOC9 (P9IOC: PORT9 I/O control)

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	0	0	0	0
R/W-1	R/W-1	R/W-0	R/W-0	R-0	R-0	R-0	R-0

Bit 0 ~ Bit 3 : unused

Bit 4 ~ Bit 7 (IOC94 ~ IOC97) : PORT9(4~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

IOCA (PSW, DEDC)

PAGE0 (PSW: PORT8,5 switch, LCD bias, key scan)

7	6	5	4	3	2	1	0
BIASS	0	P8SL	P5S	BIAS3	BIAS2	BIAS1	SC
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (SC) : key scan function control

0/1 → disable/enable

Once you enable this bit, all of the LCD signal will have a low pulse during a common period. This pulse has 30us width. Please use the following procedure to implement the key scan function :

1. Set PORT7 as input port
2. Set IOCD PAGE1 to enable PORT7 pull high function
3. Enable key scan function
4. Once push a key. Set RA bit 6 to enable PLL (CPU will run in the normal mode)
5. LCD and disable key scan function
6. Set P5S =0 or/and P8SL=0. PORT5 or/and PORT8 sent probe signal to PORT7 and read PORT7. Get the key.
7. Note!! A probe signal should be delay an instruction at least to another probe signal.
8. Set P5S =1 or/and P8SL=1. PORT5 or/and PORT8 as LCD signal

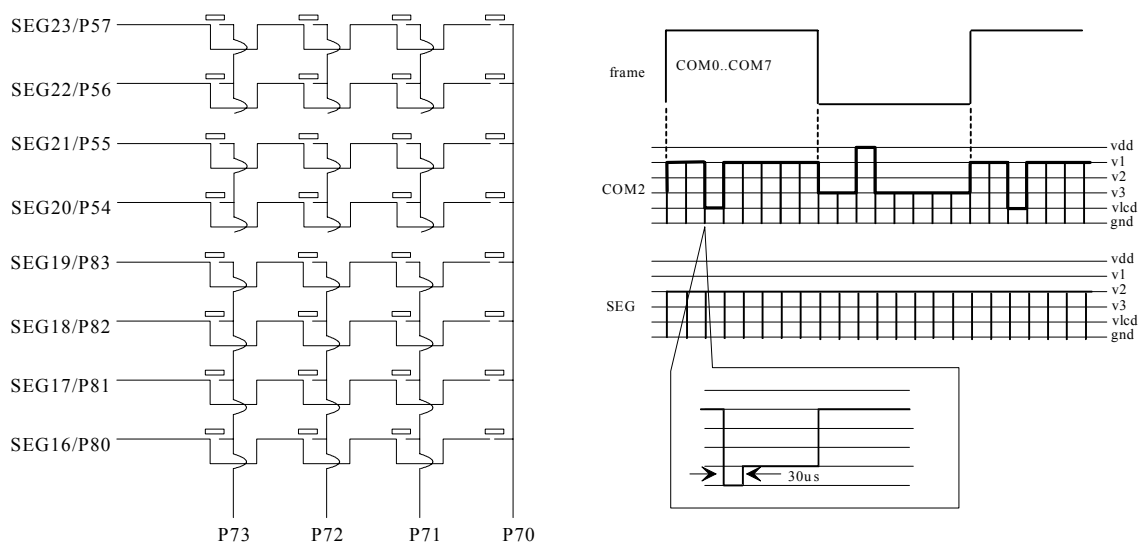


Fig.7. Key scan circuit

Bit 1 ~ 3 (BIAS1 ~ BIAS3) : LCD bias control used to choose LCD operation voltage.

(BIAS3,BIAS2,BIAS1)	Vop	VDD=5V
(0,0,0)	0.60VDD	3V
(0,0,1)	0.66VDD	3.3V
(0,1,0)	0.74VDD	3.7V
(0,1,1)	0.82VDD	4.1V
(1,0,0)	0.87VDD	4.35V
(1,0,1)	0.93VDD	4.65V
(1,1,0)	0.96VDD	4.8V
(1,1,1)	1.00VDD	5V

Bit 4 (P5S) : PORT5 nibble switch

0/1 → normal I/O port/SEGMENT output

Bit 5 (P8SL) : port8 low nibble switch

0/1 → normal I/O port P80~P83/SEGMENT output SEG16~SEG19
 Bit 6 : unused
 Bit 7 (BIASS) : Bias Select,
 0/1 → 1/4 bias / 1/3 bias

PAGE1 (DEDC: LCD power saving, Low battery detect, DED control)

7	6	5	4	3	2	1	0
0	0	CR	0	(RES)	EGCLK	DEDPWR	DEDTHTD
R-0	R-0	R/W-0	R-x	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (DEDTHTD) : The minimum detection threshold of Dual Input Energy Detector (DED)

0/1 → -45dBm/-30dBm

Bit 1 (DEDPWR) : Power control of Energy Detector (DED)

0/1 → Power off/Power on

Bit 2 (EGCLK) : Operating clock for Energy Detector (DED)

0/1 → 32.768kHz/3.5826MHz

This bit is used to select operating clock for Energy Detector (DED). When this bit is set to “1”, the PLL is also enabled regardless of RA bit 6 (ENPLL) value. At this time, the Energy detector works at high frequency mode. When this bit is set to “0”, the Energy Detector works at sub frequency mode. The difference between high frequency mode and sub frequency is as follows.

ENPLL	EGCLK	Energy Detector status	PLL status
0	0	32.768kHz operating clock	PLL is disabled
	1	Normal detection Small current consumption	PLL is enabled
1	x	3.5826MHz operating clock Accurate detection More current consumption	PLL is enabled

Ps. “x” means don’t care

In ERIC mode, the PLL will be off. When EGCLK is 1, the operating clock of Energy Detector is the frequency of ERIC oscillation, otherwise, the operating clock is sub frequency divided from ERIC oscillation.

Bit 3 (RES) : Reserved bit for factory test only. It has to be clear to zero or remain default value.

Bit 4 : unused

Bit 5 (CR) : LCD DC current saving

0/1 → normal DC current drive/half DC current drive

When this bit is set to 1, the LCD driving ability will be reducing to the half than normal current drive but it can save power.

Bit 6~7 : unused

IOCB (LCDA, CNID)

PAGE0 (LCDA: LCD RAM address)

7	6	5	4	3	2	1	0
0	0	0	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0
R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 4 (LCDA0 ~ LCDA4) : LCD RAM address

The LCD display data is stored in the data RAM. The relation of data area and COM/SEG pin is as below:

COM7 ~ COM0	Segment
00H (Bit7 ~ Bit0)	SEG0
01H	SEG1
:	:
1AH	SEG26
1BH	SEG27

COM7 ~ COM0	Segment
1CH	(empty)
:	:
1FH	(empty)

Bit 5 ~ Bit 7 = 0 : unused

PAGE1 (CN1D: Counter 1 preset)

7	6	5	4	3	2	1	0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

8-bit up counter (COUNTER1) preset and read out register. (write = preset)

In P803 mode, COUNTER1 has reload function. But in 805C mode, it has no reload function. And after an interrupt, it will count from "00".

IOCC (LCDD, CN2D)

PAGE0 (LCDD: LCD RAM data buffer)

7	6	5	4	3	2	1	0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 : LCD RAM data

For 8-COM mode, bit0 ~ bit7 are used. For 4-COM mode, only bit0 ~ bit3 are used.

PAGE1 (CN2D: Counter 2 preset)

7	6	5	4	3	2	1	0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

8-bit up-counter (COUNTER2) preset and read out register. (write = preset)

In P803 mode, COUNTER2 has reload function. But in 805C mode, it has no reload function. And after an interrupt, it will count from "00".

IOCD (TONE1C, P7PHC)

PAGE0 (TONE1C: TONE1 frequency control)

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (T10 ~ T17) : TONE1 frequency control bits

Clock source = 111957Hz and Freq. = 111957Hz / N, where N = 0 ~ 255 is divider value for T17 ~ T10

Tone generator 1's frequency divider. Please run in normal mode.

T17~T10 = '11111111' → Tone generator 1 will has 439Hz SIN wave output

:

T17~T10 = '00000010' → Tone generator 1 will has 55978Hz SIN wave output

T17~T10 = '00000001' → Tone generator1 will has 111957Hz

T17~T10 = '00000000' → no used

PAGE1 (P7PHC: PORT7 pull high control)

7	6	5	4	3	2	1	0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 7 (PH0 ~ PH7) : PORT7(0~7) pull high control bits

0/1 → Disable internal pull-high/enable internal pull-high
These control bits are used to enable the pull-high of PORT7(0 ~ 7) pins.

IOCE (TONE2C, CNPSC)

PAGE0 (TONE2C: TONE2 frequency control)

7	6	5	4	3	2	1	0
T27	T26	T25	T24	T23	T22	T21	T20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (T20 ~ T27) : TONE2 frequency control bits

Clock source = 111957Hz and Freq. = 111957Hz / N, where N = 0 ~ 255 is divider value for T27 ~ T20

Tone generator 2's frequency divider. Please run in normal mode.

T27~T20 = '11111111' → Tone generator 2 will has 439Hz SIN wave output.

:

T27~T20 = '00000010' → Tone generator 2 will has 55978Hz SIN wave output.

T27~T20 = '00000001' → Tone generator 2 will has 111957Hz SIN wave output.

T27~T20 = '00000000' → no used

		TONE2 (IOCE) High group freq.			
		1203.8 (0X5D)	1332.8(0X54)	1473.1(0X4C)	1646.4(0X44)
TONE1(IOCD,	699.7Hz(0x0A0)	1	2	3	A
IOCA PAGE1)	772.1Hz(0x091)	4	5	6	B
Low group freq.	854.6Hz(0x083)	7	8	9	C
	940.8Hz(0x077)	*	0	#	D

PAGE1 (CNPSC: Open-drain control, Counter 1,2 clock source and prescaler, LCD mode)

7	6	5	4	3	2	1	0
OP77	OP76	C2S	C1S	PSC2	PSC1	PSC0	LCDM
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (LCDM) : LCD mode control for 8-COM, 1/8 duty or 4-COM, 1/4 duty selection

0 → 8-COM mode selection and COM0 ~ COM7 are enabled

1 → 4-COM mode selection and COM0 ~ COM3 are enabled

Bit 1 ~ 3 (PSC0~PSC2) : Counter1 prescaler setting

reset = (0,0,0)

(PSC2,PSC1,PSC0)	Scaler ratio
(0,0,0)	1:1
(0,0,1)	1:2
(0,1,0)	1:4
(0,1,1)	1:8
(1,0,0)	1:16
(1,0,1)	1:32
(1,1,0)	1:64
(1,1,1)	1:128

Bit 4 (C1S) : Counter1 source

0/1 → 32.768kHz/MAIN clock if enable

In ERIC mode, the clock source will be replaced by sub frequency (0) and the frequency of ERIC oscillation (1).

Bit 5 (C2S) : Counter2 source

In the normal mode:

0/1 → 32.768kHz/Main clock if enable, scale=1:1

In ERIC mode, the clock source will be replaced by sub frequency (0) and the frequency of ERIC oscillation (1).

Bit 6 (OP76) : P76 open-drain control

0/1 → disable/enable
Bit 7 (OP77) : P77 open-drain control
0/1 → disable/enable

IOCF (INTM)

PAGE0 (INTM: Interrupt Mask Register)

7	6	5	4	3	2	1	0
EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 5,7 : interrupt enable bit
1/0 → enable/disable interrupt
Bit 6 : unused
IOCF Register is readable and writable. They work with RF registers.

PAGE1

Non-existence. Always keep this bit to "0". Don't set it to "1" to prevent causing problem

VII.4 TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8-bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.
- See the prescaler ratio in CONT register.
- Fig. 8 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

In ERIC mode, the instruction clock is the half of frequency of ERIC oscillation. When TS bit sets 1, the clock is the half of sub frequency divided from the frequency of ERIC oscillation.

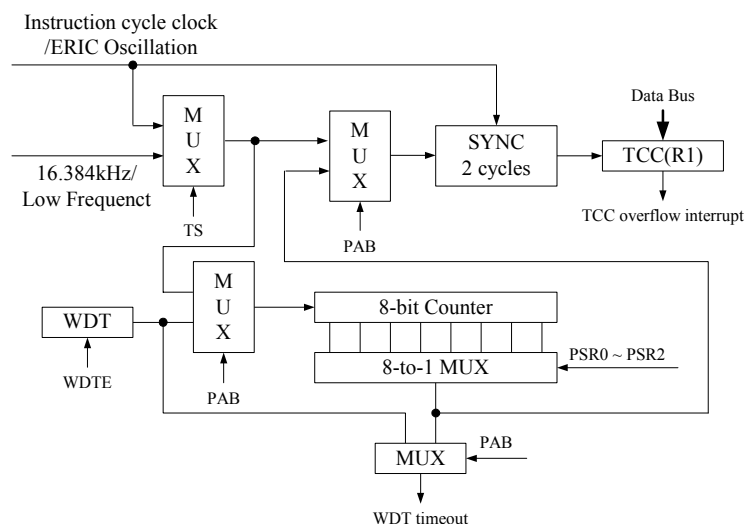


Fig.8 Block diagram of TCC WDT

VII.5 I/O Ports

The I/O registers, Port5 ~ Port 9, are bi-directional tri-state I/O ports. Port 7 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC6 ~ IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.9.

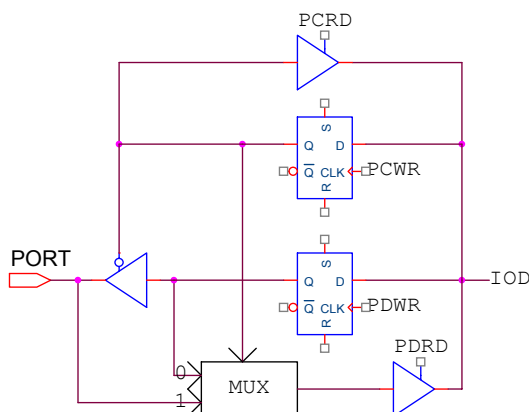


Fig.9 Circuit of I/O port and I/O control register

VII.6 RESET and Wake-up

The RESET can be caused by

- (1) External /RESET pin
- (2) Power on reset or Power on voltage detector reset (/POVD reset)
- (3) WDT timeout. (if enabled and in GREEN or NORMAL mode)

Note that only Power on reset, or only Power on voltage detector reset in Case(2) is enabled in the system by CODE Option bit. If /POVDs disabled, Power on reset is selected in Case (2). Refer to Fig.10.

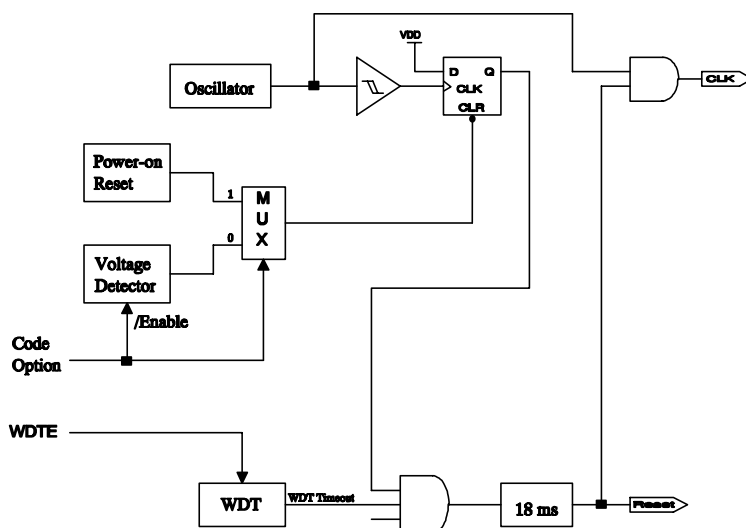


Fig.10 Block diagram of Reset of controller

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".

- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)

R5 = "xxxx0000"	IOC5 = "1111xxxx"	
R6 = PORT	IOC6 = "11111111"	
R7 = PORT	IOC7 = "11111111"	
R8 = PORT	IOC8 = "11111111"	
R9 = PORT	IOC9 = "11111111"	
RA = "00110000"	Page0 IOCA = "00000000"	Page1 IOCA = "00000000"
RB = "0000x000"	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000"	Page0 IOCC = "xxxxxxxx"	Page1 IOCC = "00000000"
RD = "xxxxxxxx"	Page0 IOCD = "00000000"	Page1 IOCD = "00000000"
RE = "x0000000"	Page0 IOCE = "00000000"	Page1 IOCE = "00000000"
RF = "00000000"	IOCF = "00000000"	

The controller can be awakened from SLEEP mode or IDLE mode (execution of "SLEP" instruction, named as SLEEP mode or IDLE mode) by (1) TCC time out (IDLE mode only) (2) WDT time-out (if enabled) (3) external input at PORT9 (4) Energy detector (DED) output data. The three cases will cause the controller to be wake-up and run from next instruction in IDLE mode, reset in SLEEP mode. After CPU is wake-up, user should control Watchdog in case of reset in GREEN mode or NORMAL mode. The last three should be open RE register before into SLEEP mode or IDLE mode. The first one case will set a flag in RF bit 0. And it will go to address 0x08 when TCC generates an interrupt.

VII.7 Interrupt

The Caller ID IC has internal interrupts which are falling edge triggered, as follows: TCC timer overflow interrupt (internal) , two 8-bit counters overflow interrupt .

If these interrupt sources change signal from high to low, then RF register will generate '1' flag to corresponding register if you enable IOCF register.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are four external interrupt pins including INT0, INT1, INT2 and INT3. And four internal counters interrupt available.

External interrupt INT0, INT1, INT2, INT3 signals are from PORT7 bit0 to bit3. If IOCF is enable then these signal will cause interrupt, or these signals will be treated as general input data.

After reset, the next instruction will be fetched from address 000H and the instruction interrupt is 001H and the hardware interrupt is 008H.

TCC will go to address 0x08 in GREEN mode or NORMAL mode after time out. And it will run next instruction from "SLEP" instruction and then go to address 0x08 in IDLE mode. These two cases will set a RF flag.

VII.8 Instruction Set

Instruction set has the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
- (2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

Instruction binary	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C

0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1	1110	1000	kkkk	1E8k	PAGE k	K→R5	None
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

VII.9 System Option

VII.9.1 CODE Option Register

The IC has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution and can be set when downloading the program code.

12	11	10	9	8	7	6	5	4	3	2	1	0
						SFDIV2	SFDIV1	SFDIV0		P803ON		PTB

Bit 0 (PTB) : Protection Bit

0 → enable

1 → disable (default)

When PTB bit sets, the program code in the code ROM isn't readable. Otherwise, the program code can be read from the code ROM. The default is disable.

Bit 2 (P803ON): P803 mode enable

0 → 805C Mode

1 → P803 Mode (default)

If P803ON bit set, the system runs in P803 mode. Otherwise, the system runs in 805C mode. Please refer Sec. VII.13 "Difference Between P803 And 805C Mode" for more detail.

Bit 4~6 (SFDIV2~0): Scale factor of main frequency

In ERIC mode, the sub frequency is divided from the frequency of ERIC oscillation. These three bits set up the scale factor of division. Be careful to choose the main frequency and scale factor. Because the improper sub frequency will cause some function failure. Please refer VII.15 "ERIC Mode" for more detail.

SFDIV2	SFDIV1	SFDIV0	Scale factor
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64

SFDIV2	SFDIV1	SFDIV0	Scale factor
1	1	0	1:128
1	1	1	1:256

Bit 1, Bit 3, Bit 7 ~ Bit 12 : unused

VII.9.2 PAD Option

There are two PAD options on the system, /POVD and ERICen. One pad option contains two pads. One is on the side of VSS and the other is on the side of VDD. User can choose what signal should be connect to the PAD options. Then the option pad will bind to VDD or VSS during the bonding the chip.

	ERICen	/POVD
0	Crystal mode	Power on voltage detector off
1	ERIC mode	Power on voltage detector on

ERICen : ERIC mode enable

Pull low → Crystal mode

Pull high → ERIC mode

If this pin pulls low, the system runs in Crystal mode. The external crystal supplies the system clock.

Otherwise, the system runs in ERIC mode. The system clock is generated by RC oscillation with an external resistor. Please refer VII.15 “ERIC Mode” for more detail.

/POVD : Power on voltage detector reset enable pin

Pull low → enable

Pull high → disable

For VDD = 3.3V, the /POVD reset voltage

/POVD	2.2 V /POVD reset	1.6V power on reset	sleep mode current
0	yes	no	15uA
1	no	yes	1uA

Ps. When /POVD is disabled, the CPU reset is by power on reset circuit. When /POVD is enabled, the CPU reset is by /POVD reset circuit.

VII.10 Energy Detector (DED)

The Energy Detector is differential input and zero crossing detector namead as DED. It can detect any incoming AC signal above its threshold level and output corresponding zero-crossing frequency pulse. For very low power concern, there is no any signal filtering circuit in DED circuit so the user need to have his software algorithm to judge incoming signal by reading its output DEDD bit. For this energy detector, the user can set it's minimum detection threshold level at -30dBm or -45dBm by DEDTHD bit. All the minimum detection value can be achieved under input capacitor around 1000pF ~ 4700pF and input resistor around 22k ~ 100k ohms. The energy detector has power control by IOCA PAGE1 bit 1 (DEDPWR).

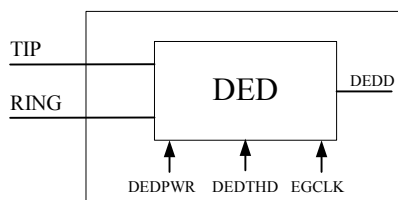


Fig.11 DED diagram

Register bits of Energy Detector:

Register bits	Descriptions
RB bit 3 (DEDD)	DEDD : Output data of DED
RB bit 7 (EDGE)	EDGE : edge control of DED output data 0/1 => Falling edge trig. / Rising edge trig. & Falling edge trig.
RE bit 0 (/WUEDD)	/WUEDD : Wake-up control of DED output data 1/0 => enable/disable
RF bit 7 (EDD)	EDD : Interrupt flag of DED output data
IOCF bit 7 (EDD)	EDD : Interrupt mask of DED output data 1/0 → enable/disable interrupt of EDD output data
IOCA PAGE1 bit 0 (DEDTHD)	DEDTHD : Minimum detection threshold of DED 0/1 → -45dBm/-30dBm
IOCA PAGE1 bit 1 (DEDPWR)	DEDPWR : Power control of DED 0/1 → power off/power on
IOCA PAGE1 bit 2 (EGCLK)	Bit 2 (EGCLK) : Operating clock for DED 0/1 → 32.768kHz/3.5826MHz

In ERIC mode, when the EGCLK sets 0, the operating clock will be the sub frequency divided from the frequency of ERIC oscillation. Otherwise, the operating clock will be the frequency of ERIC oscillation.

VII.11 LCD Driver

The Caller ID IC can drive LCD directly and has 28 segments and 8 commons that can drive 28*8 dots totally. LCD block is made up of LCD driver; display RAM, segment output pins, common output pins and LCD operating power supply pins.

The outputs of commons and segments equipped with buffer. So the LCD driver has bigger driving capacity than EM78805C, which means EM78P803 can drive bigger LCD panel than EM78805C.

Duty, bias, the number of segment, the number of common and frame frequency are determined by LCD mode register. LCD control register.

The basic structure contains a timing control which uses the basic frequency 32.768KHz to generate the proper timing for different duty and display access. RE register is a command register for LCD driver, the LCD display (disable, enable, blanking) is controlled by LCD_C and the driving duty and bias is decided by LCD_M and the display data is stored in data RAM which address and data access controlled by registers RC and RD.

In ERIC mode, the PLL is off and there is no 32.768kHz clock in the system. The sub frequency is divided from main clock generated from ERIC oscillation by the scale factor listed in Sec. VII.9.1. It means that the sub frequency depends on the main clock. If user wants to use the function of LCD driver in the system, user should design a suitable system clock and scale factor after chose the LCD panel. Or, equipped with a proper LCD panel after decided what frequency the system runs on. If sub frequency is too fast or too slow, there will be some unexpected condition happened on the LCD panel.

The following table lists the recommend main frequency with proper scale factor. User can adjust the main frequency for different types of LCD panel.

Main Frequency	Scale Factor
64 kHz	2
128 kHz	4
256 kHz	8
512 kHz	16
1M Hz	32
2M Hz	64
4M Hz	128
8M Hz	256

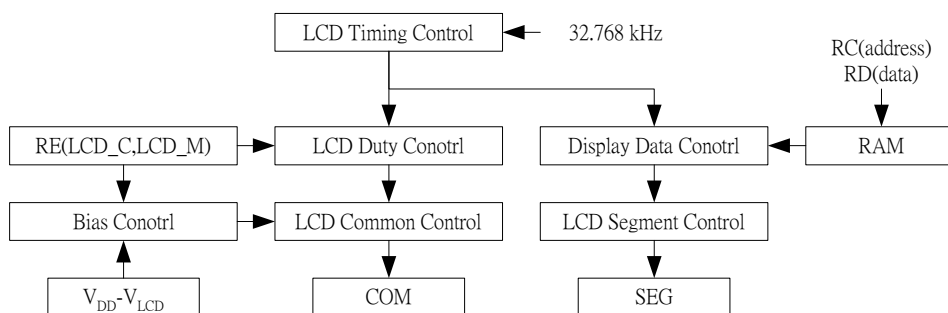


Fig.12 LCD driver control

VII.11.1 LCD Driver Control

RE(LCD Driver Control)(initial state "00000000")

7	6	5	4	3	2	1	0
					LCD_C2	LCD_C1	

Bit 1 ~ 2 (LCD_C1, LCD_C2) : LCD display enable or blanking

The display duty change must set the (LCD_C2, LCD_C1) to (0,0).

(LCD_C2, LCD_C1)	LCD Display Control	duty	bias
(0,0)	Disable(turn off LCD)	(*1)	1/4
(0,1)	Blanking	:	:
(1,1)	LCD display enable	:	:

*1. 1/8 or 1/4 duty depends on IOCE PAGE1 bit0 (LCDM)

VII.11.2 LCD display area

The LCD display data is stored in the data RAM. The relation of data area and COM/SEG pin is as below:
The relation of data area and COM/SEG pin is as below:

COM7 ~ COM0	Segment
00H (Bit7 ~ Bit0)	SEG0
01H	SEG1
:	:
1AH	SEG26
1BH	SEG27
1CH	(empty)
:	:
1FH	(empty)

IOCB(LCD Display RAM address)

7	6	5	4	3	2	1	0
-	-	-	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

* Bit 0 ~ Bit 5 : select LCD Display RAM addresses up to 27.

IOCC (LCD Display data) : Bit 0 ~ Bit 7 are LCD data.

VII.11.3 LCD COM and SEG signal

COM signal : The number of COM pins varies according to the duty cycle used, as following: in 1/8 duty mode

	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
1/8	o	o	o	o	o	o	o	o
1/4	o	o	o	o	x	x	x	x

x : open, o : select,

SEG signal: The 28 segment signal pins are connected to the corresponding display RAM address 0 to 27. The high bit and the low bit (bit7 down to bit0) are correlated to COM7 to COM0 respectively. For 8-COM mode, COM7 to COM0 and LCD RAM IOCC PAGE0 bit0~7 are used. For 4-COM mode, COM3 to COM0 and LCD RAM only IOCC PAGE0 bit0~bit3 are used

When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0, a non-select signal is sent to the corresponding segment pin.

*COM, SEG and Select/Non-select signal is shown as following. In the figure, the VLCD is equal to VDD-VOP. It means that VLCD is higher than GND except VOP=VDD.

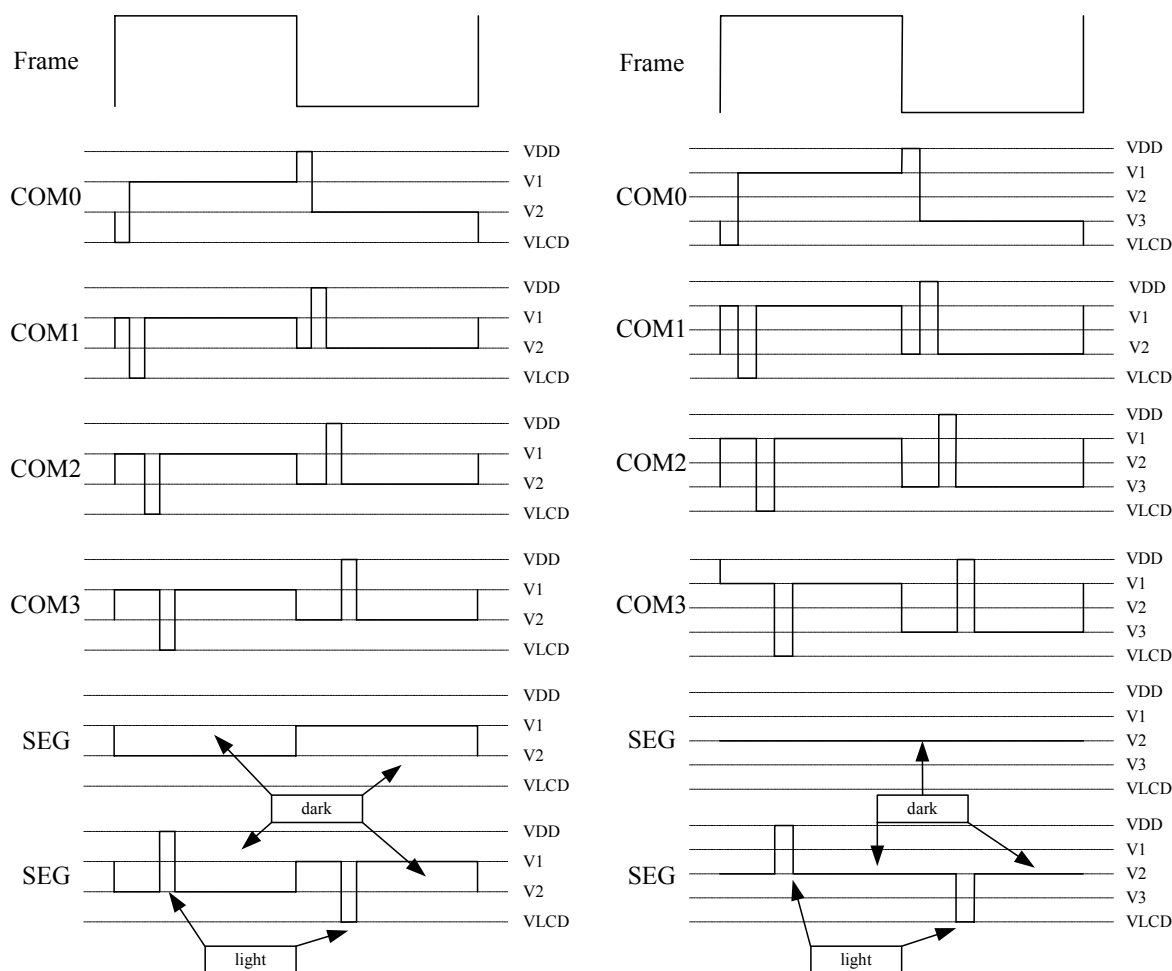


Fig.13 LCD waveform, 1/3 bias & 1/4 bias, 1/8 duty or 1/4 duty

VII.11.4 LCD power saving

For some application, it needs more power concerning and only small LCD dots or little LCD driving required. User can use the LCD power saving function in this application. Some bits setting will let LCD driver less current consumption. Please refer to IOCA PAGE1 bit5 (CR) for details.

VII.12 Difference Between P803A And 805C Mode

The following table shows the difference between EM78805C, EM78P803A and EM78R803. EM78P803A and EM78R803 comes from EM78805C. So they have many features as almost the same as EM78805C. The P803ON option is designed for who want to develop EM78805C application in EM78P803A and EM78R803. The P803ON option bit switches P803 mode and 805C mode and will affect those item which is different in EM78805 and EM78P(R)803.

	EM78805C	EM78P803A	EM78R803
ROM size	12k x 13b	8k x 13b	16k x 13b
Max. I/O	22	28	28
Main Clock	3.5826MHz x 1/8, 1/4, 1, 2	3.5826MHz x 1/2, 1, 2, 4 and ERIC mode	3.5826MHz x 1/2, 1, 2, 4 and ERIC mode
LCD (Max. Seg.x Com.)	24 x 8/4 1/4 Bias	28 x 8/4 1/3, 1/4 Bias	28 x 8/4 1/3, 1/4 Bias

Those items which will be different in mode switching are discussed as following:

- ROM Size**
Because ROM size in EM78P803A is smaller than EM78805C, whatever the P803ON bit set or clear, ROM size will not change. In EM78R803, ROM size is bigger than EM78805C. When the P803ON pin pulls high, ROM size is 16k x 13b; otherwise, the ROM size is 12k x 13b.
- I/O**
There are maximum 28 I/Os in EM78P803A and EM78R803. When P803ON bit sets, user can use all of 28 I/Os. But when P803ON bit cleared, user can only use maximum 22 I/Os which are as the same as EM78805C. other I/O which don't exist in EM78805C are not writable and return zero after reading.
- Main Clock**
The configuration of main clock is different in EM78805C and EM78P803A and EM78R803. When the P803ON bit cleared, the configuration of main clock will change to the configuration which is as the same as EM78805C.
- LCD Driver**
The number of segment in EM78P803A and EM78R803 is more than EM78805C. When the P803ON bit cleared, user can access only 24 segments and 1/4 bias.

ENPLL	CPU's clock		(CLK2,CLK1)	MAIN clock	
	P803A	805C		P803A	805C
0	32.768kHz	32.768kHz	(x,x)	x	x
1	1.7913MHz	447.8293kHz	(0,0)	1.7913MHz	447.8293kHz
1	14.331MHz	895.6587kHz	(0,1)	14.331MHz	895.6587kHz
1	7.1652MHz	7.1653MHz	(1,0)	7.1652MHz	7.1653MHz
1	3.5826MHz	3.5826MHz	(1,1)	3.5826MHz	3.5826MHz

VII.13 ERIC Mode

The system has an optional RC mode. In this ERIC mode, user can connect PLLC to VDD with a resistor serially. Then the system will generate a clock signal internally by an internal capacitor and external resistor on PLLC pin. User can use only one resistor to replace the crystal oscillator in order to reduce PCB area and cost.

In ERIC mode, the main frequency is provided by ERIC oscillation and the sub frequency is provided by the main frequency through the scaler. User can configure the scaler with different factors in order to get the suitable match with peripheral of system (like LCD driver, dual tone generator) and main frequency. For example, for low power application with LCD display, user can choose the frequency 1MHz with scale factor 32. The sub frequency will be about 32kHz. With this frequency, the LCD panel can work well.

In the other hand, user can choose a suitable sub frequency which is different from 32kHz (For example, high frequency LCD panel). Then choose the right Main frequency and set the scale factor correctly. But be careful, the sub frequency you choose cannot let the other function work well (For example, tone generator). User can refer following table to get 32kHz sub frequency.

The formula of ERIC frequency is $f=1/(R \times 5.25 \times 10^{-12})$. For example, when R=100k Ohm, main frequency is about 1.9MHz. The following table shows the suggested resistor and approximate main frequency. The scaler doesn't work when in crystal mode. In crystal mode, the sub frequency is always 32kHz. The following tables shows the suggested serial connected resistor and generated main frequency, scale factor and sub frequency

Ext. Resistor	RC Frequency	Scale Factor	Sub. Frequency
1.5M	127k	4	31.8k
750k	254k	8	31.8k
360k	529k	16	33.1k
180k	1059k	32	33.1k
91k	2110k	64	33k
47k	4054k	128	31.7k
22k	8662k	256	33.8k

In ERIC mode, the main and sub frequency act at the same time. Thus, the operating modes of system are only normal mode and sleep mode.

The frequency of ERIC oscillator affected by operating voltage. The higher operating voltage the MCU has, the faster frequency the ERIC oscillator generates. According to our laboratory test, the following table shows the highest frequency in different operating voltage. Notice that it is our laboratory measured data. It is probably different in practical situation. And it will vary from different EM78801s. The resistance shows in the table might not be suitable for the formula of ERIC oscillation mentioned before. The formula has a bit changed because the frequency is too fast.

	Power	ERIC Oscillation	Serial Resistance
1	2.2V	6.84MHz	30.13k
2	2.6V	9.96MHz	20.29k
3	3V	11.63MHz	18.4k
4	4V	15.11MHz	13.98k
5	5V	18.12MHz	11.75k
6	5.5V	19.27MHz	11.02k

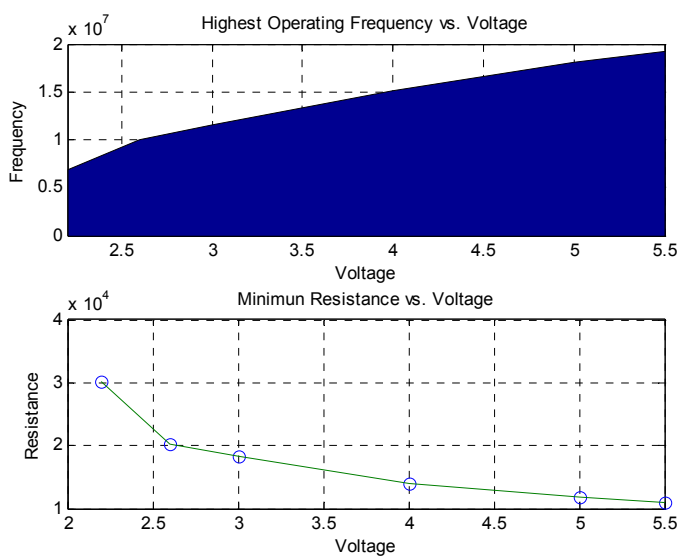


Fig.14 Frequency vs. operating voltage

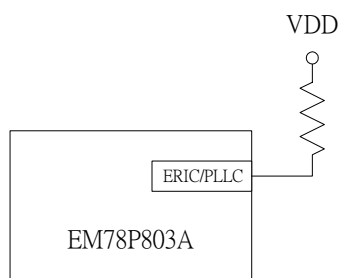


Fig.15 Circuit of ERIC mode

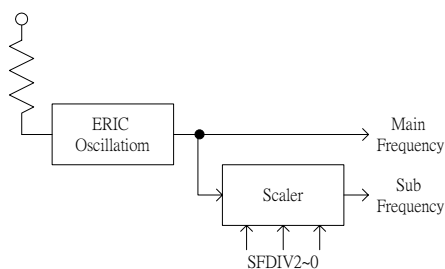


Fig.16 Block diagram of ERIC oscillation

VIII. Absolute Operation Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.3 To 6	V
Input Voltage	Vin	-0.5 to VDD +0.5	V
Operating Temperature Range	Ta	0 to 70	°C

IX. DC Electrical Characteristic

(Ta = 25°C, AVDD=VDD=5V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DC Supply Voltage	VDD	Main Clock = 7.1652MHz	2.8		5.5	V
		Main Clock = 14.331MHz	4.5		5.5	V
Input Voltage	Vin		-0.5		VDD+0.5	V
Operating Temperature	Ta		0		70	°C
Input leakage current for input pins	IIL1	VIN = VDD, VSS			±1	μA
Input leakage current For bi-directional pins	IIL2	VIN = VDD, VSS			±1	μA
Input high voltage	VIH		2.5			V
Input low voltage	VIL				0.8	V
Input high threshold voltage	VIHT	/RESET, TCC	2.0			V
Input low threshold voltage	VILT	/RESET, TCC			0.8	V
Clock input high voltage	VIHX	OSCI	3.5			V
Clock input low voltage	VILX	OSCI			1.5	V
Output high voltage for (port5,6,7,8)	VOH1	IOH = -1.6mA	2.4			V
Output high voltage for PORT9	VOH2	IOH = -6mA	2.4			V
Output low voltage for (Port5, 6,7,8)	VOL1	IOH = 1.6mA			0.4	V
Output low voltage for Port9	VOL2	IOH = 6mA			0.4	V
Common voltage drop	V _{COM}	I _O = ±50 uA			2.9	V
Segment voltage drop	V _{SEG}	I _O = ±50 uA			3.8	V
Pull-high current	IPH	Pull-high active input pin at VSS	-13.2	-13.4	-13.8	μA
Power down current (SLEEP mode)	ISB1	All input and I/O pin at VDD, output pin floating, WDT disabled, POVD disable, other circuit disable.		0.64	0.8	μA
Low clock current (IDLE mode) POVD disable	ISB3	CLK=32.768KHz,TONE block disable, All input and I/O pin at VDD, output pin floating, WDT disabled, LCD enable		35	45	μA
Low clock current (IDLE mode) POVD enable				40	60	uA
Low clock current (GREEN mode)	ISB2	CLK=32.768KHz,TONE block disable, All input and I/O pin at VDD, output pin floating, WDT disabled, LCD enable, POVD disable		28.16	50	μA
Operating supply current (Normal mode)	ICC1	/RESET=High, CLK=3.5826MHz, output pin floating, other analog circuits disabled		1.39	1.6	mA
Tone generator reference voltage	Vref2		0.5	0.6	0.7	VDD

* This specification are subject to be changed without notice.

Energy Detector (DED) (Ta=0°C ~ 70°C, VDD=3.3V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{DED}	Operating current for Energy Detector	Fclk=32.768kHz Not including MCU and other parts		15	20	uA

XI. AC Electrical Characteristic

CPU instruction timing (Ta = 25°C, AVDD=VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.582MHz		60 550		us ns
Device delay hold time	Tdrh			18		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C	16-30%	18	16+30%	ms

Note 1: N= selected prescaler ratio.

Timing characteristic (AVDD=VDD=5V, Ta=+25°C)

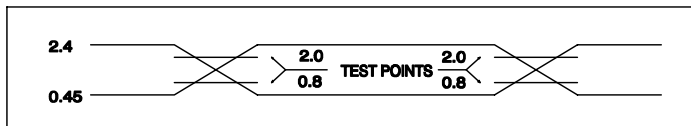
Description	Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic					
Crystal start up	32.768kHz	Tosc	400	1500	ms
	3.579MHz PLL		5	10	us
Timing characteristic of reset					
The minimum width of reset low pulse	Trst	3			uS
The delay between reset and program start	Tdrs		18		mS

DED AC Characteristic (Vdd=+5V, Ta=+25°C)

Characteristic	Min	Typ	Max	Unit
Input sensitivity TIP and RING for DED, DEDTHD bit=0		-45	--	dBm
Input sensitivity TIP and RING for DED, DEDTHD bit=1		-30	--	dBm

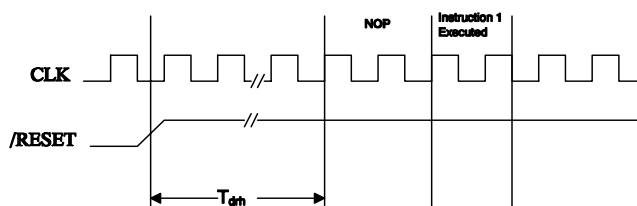
XII. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

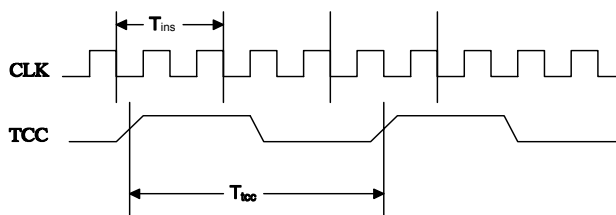


Fig.15 AC timing

XIII. Application Circuit

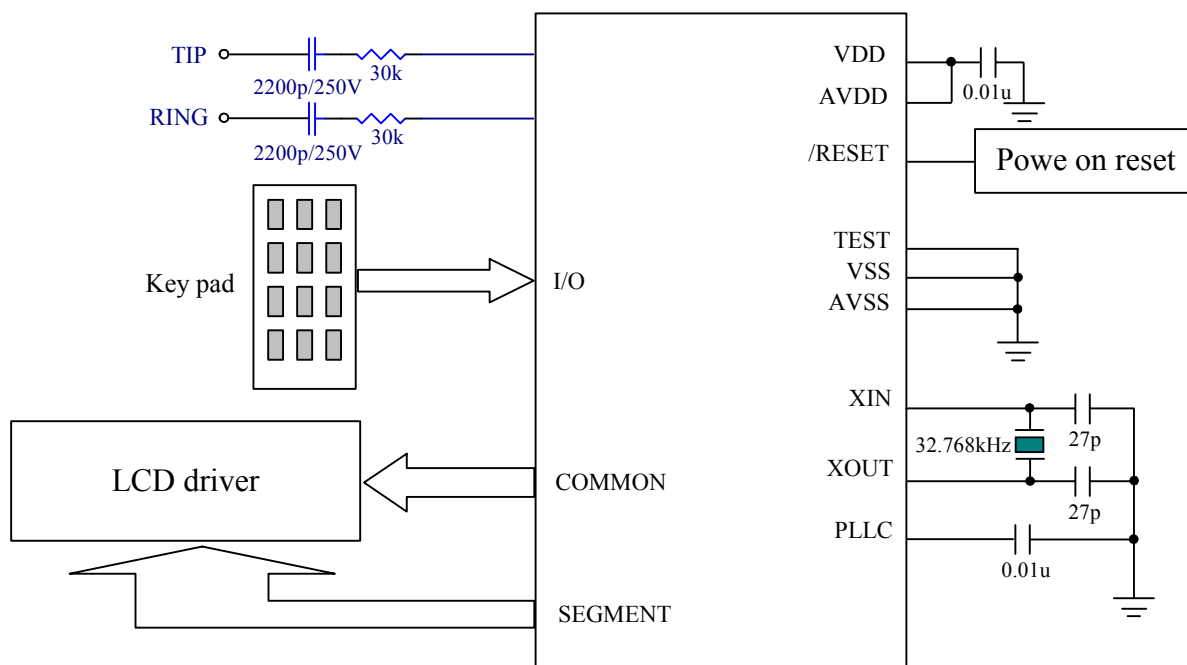


Fig.16 Application circuit

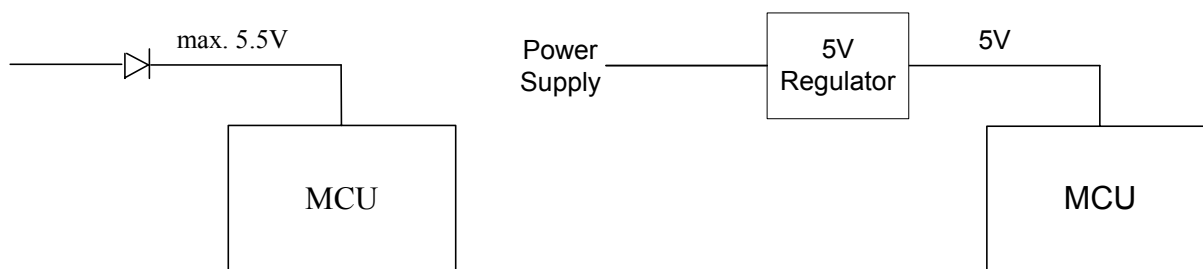


Fig.17 Power Concern in Application