EM78807

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.5

ELAN MICROELECTRONICS CORP.

March 2006

Trademark Acknowledgments:
IBM is a registered trademark and PS/2 is a trademark of IBM.
Windows is a trademark of Microsoft Corporation.
ELAN and ELAN logo are trademarks of ELAN Microelectronics Corporation.

The contents of this specification are subject to change without further notice. ELAN Microelectronics assumes no responsibility concerning the accuracy, adequacy, or completeness of this specification. ELAN Microelectronics makes no commitment to update, or to keep current the information and material contained in this specification. Such information and material may change to conform to each confirmed order.

In no event shall ELAN Microelectronics be made responsible for any claims attributed to errors, omissions, or other inaccuracies in the information or material contained in this specification. ELAN Microelectronics shall not be liable for direct, indirect, special incidental, or consequential damages arising from the use of such information or material.

The software (if any) described in this specification is furnished under a license or nondisclosure agreement, and may be used or copied only in accordance with the terms of such agreement.

ELAN Microelectronics products are not intended for use in life support appliances, devices, or systems. Use of ELAN Microelectronics product in such applications is not supported and is prohibited.
NO PART OF THIS SPECIFICATION MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE EXPRESSED WRITTEN PERMISSION OF ELAN MICROELECTRONICS.

ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation Road 1
Hsinchu Science Park
Hsinchu, Taiwan 30077
Tel: +886 3 563-9977
Fax: +886 3 563-9966
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Rm. 1005B, 10/F Empire Centre
68 Mody Road, Tsimshatsui
Kowloon , HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780
elanhk@emc.com.hk

USA:
Elan Information Technology Group (U.S.A.)
1821 Saratoga Ave., Suite 250
Saratoga, CA 95070
USA
Tel: +1 408 366-8225
Fax: +1 408 366-8220

Europe:
Elan Microelectronics Corp. (Europe)
Siewerdtstrasse 105
8050 Zurich, SWITZERLAND
Tel: +41 43 299-4060
Fax: +41 43 299-4079
http://www.elan-europe.com

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
SSMEC Bldg., 3F, Gaoxin S. Ave.
Shenzhen Hi-Tech Industrial Park
Shenzhen, Guandong, CHINA
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500

Shanghai:
Elan Microelectronics Shanghai, Ltd.
23/Bldg. #115 Lane 572, Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA
Tel: +86 21 5080-3866
Fax: +86 21 5080-4600

Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2005/01/24
0.2	1. Changed the Voice ROM from 210K×5 to 300K×4 and relative register bits 2. Changed the product name from 78807C to 78807 3. Reduced the D/A minimum output current from 0.625mA to 0.3125mA. Modified the least 3 current adjustment.	2005/01/25
0.3	1. Made a big change on the pin configuration for customer application use 2. Modified and added relative register due to pin configuration change 3. Added important application	2005/01/27
0.4	Updated R5 and R6 register title description	2005/02/01
0.5	1. Modified the Main Feature particularly the Clock part 2. Modified the General description 3. Revised the IOC5 Page 1 Bits 4~6 definition 4. Rearranged the whole spec pages 5. Added Idle mode back to the spec	2005/02/03
0.6	Revise bit location of PSW3 in User Application Note	2005/02/14
0.7	1. Revise current table of IOC5 PAGE1 bit0~3(VOL0~VOL3) 2. Revise IOC9 PAGE1 voice ROM data type from R/W to R 3. Change definition of R7 PAGE1 bit6 (PSW8) = 0 by adding DED disabled	2005/03/02
1.0	1. Revised the MCU operating voltage range and DAC description in the Features section 2. Changed all unused bits as read only 3. Corrected the power-on reset value on some registers 4. Corrected some description bugs 5. Revised the description in User Application Note item “3” and “4 (1), 4(2)” 6. Re-arranged the pages of the document 7. Updated the Application circuit	2005/04/08
1.1	1. Clarified the description in User Application Note item “3” 2. Updated the IOCA Page 1 Bit 3 description	2005/04/28

Doc. Version	Revision Description	Date
1.2	1. Added Bit 1(CDAR) for the Code Option Register for current D/A. 2. Modified the current D/A reference current value from “0” to “0 or 0.3125mA” option while setting VOL3 ~ VOL0 =0. This option is controlled by Code Option Register Bit 1(CDAR) 3. Revised the spec description: (1) Revised "PS9" to "PSW9" in Item 4 of User Application Note (2) Revised "Fig.4" to "Fig.3" (3) Revised "Bit 0 I :" to "Bit 0 (C)" (4) Removed the note in R4 register (5) Removed "Bit 4: unused" and revised "Bits 5~7" to "Bits 4~7" (6) Revised “Fig.16" to "Fig.4" in CONT Bit 5 (7) Revised "Bit 0 ~ Bit 3" to "Bit 4~Bit 6" in IOC5 Page 1 (8) Revised “IOC6 Page 1,"Page 1 (Voice ROM ddress (16~18))" to "Page 1 (VRAH: Voice ROM address(16~18))" (9) Revised "VRAH" to "VRAM" in IOC7 (10) Revised the no. of keyscan steps (11) Modified "1.5826MHz" to "3.5826MHz" in EGCLK register (12) Revised the description "has 60 segments and 16 commons that can drive 60*16 dots totally" to "has 40 segments and 8 commons that can drive 40*8 dots totally" (13) Removed “For VDD = 3.3V, the /POVD reset voltage” in section 7.9 Code Option Register	2005/05/05
1.3	Modified the spec description: 1. Modified the voice ROM size from 300K×4 to 304K×4 2. Modified (IOC6~IOC8) Page 1 description about voice ROM	2005/07/08
1.4	Updated the pin configuration	2005/08/17
1.5	1. Deleted the descriptions for ICE807C 2. Modified the note on the I/O port description	2006/03/31

1 Introduction

The EM78807 is an 8-bit CID (Caller Identification) RISC architecture microprocessor with low power, high speed CMOS technology integrated onto a single chip. It contains a Watchdog Timer (WDT), RAM, ROM, programmable real time clock /counter, internal interrupt, power down mode, LCD driver, Energy Detector (DED), large voice ROM for midi data, Current DAC and tri-state I/O. It provides a single chip solution to design a CID with calling message display.

2 Feature

- Single power supply
  - Operating voltage range:
    - 2.6V ~ 3.6V (Normal mode, 17.913 MHz)
    - 2.2V ~ 3.6V (Normal mode, 447.829kHz~14.331 MHz)
    - 2.0V ~ 3.6V (Sleep/Green mode)
- CPU
  - 8-bit RISC kernel
  - Single instruction cycle commands
- Clock
  - 32.768kHz clock source
  - Built-in PLL to generate main clock 3.5826MHz x 0.125, 0.25, 0.5, 1, 2, 3, 4 and 5
- Timer and Counter
  - Watchdog: Programmable free running on-chip watchdog timer
  - TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler
  - Counter 1: 8-bit counter with 8-bit prescaler can be an interrupt source
  - Counter 2: 8-bit counter with 8-bit prescaler can be an interrupt source
- Memory
  - 16K × 13 bits on chip program ROM
  - 304K × 4 bits on-chip voice ROM (max. timing from voice ROM enable to its data finish = 1.25 µs)
  - 0.5K × 8 bits on chip CID RAM
  - 144 × 8 bits common registers

- I/O
  - 2 output/38 bidirectional tri-state I/O ports (5 independent I/O)
  - I/O with internal Pull high, wake-up and interrupt functions
- Operation mode

  Selectable three modes (Main clock is generated by internal PLL)

Mode	CPU Status	Main Clock	32.768kHz Clock Status
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- Interrupt
  - Selectable signal sources and overflow interrupt
  - Stack: 8 levels stack for subroutine nesting
  - 8 interrupt source: 4 external, 4 internal
- Reset
  - Power on reset, /POVD reset (by Code option) or external /RESET pin
- DAC
  - 10-bit current DAC
  - Programmable for DTMF tone generation by software
  - Two output pins can be multiplexed for midi or DTMF tone output
- CID
  - Differential-input Energy Detector (DED) for line energy detection
- LCD
  - LCD operation voltage chosen by software
  - Common driver pins: 8 (COM- ~ COM7) or 4 (COM0 ~ COM3)
  - Segment driver pins: 40 (SEG0 ~ SEG39)
  - 1/4 bias with output buffer
  - 1/4 duty or 1/8 duty
- Package
  - 64-pin die (EM78807CH)

3 Application

- Caller ID simple phone units for FSK/DTMF dual system with midi application
- Applications for LCD dots with less than 8x40/4x40 and few I/Os
- Applications for many I/Os with less than 40 and no LCD display

4 Pin Configuration

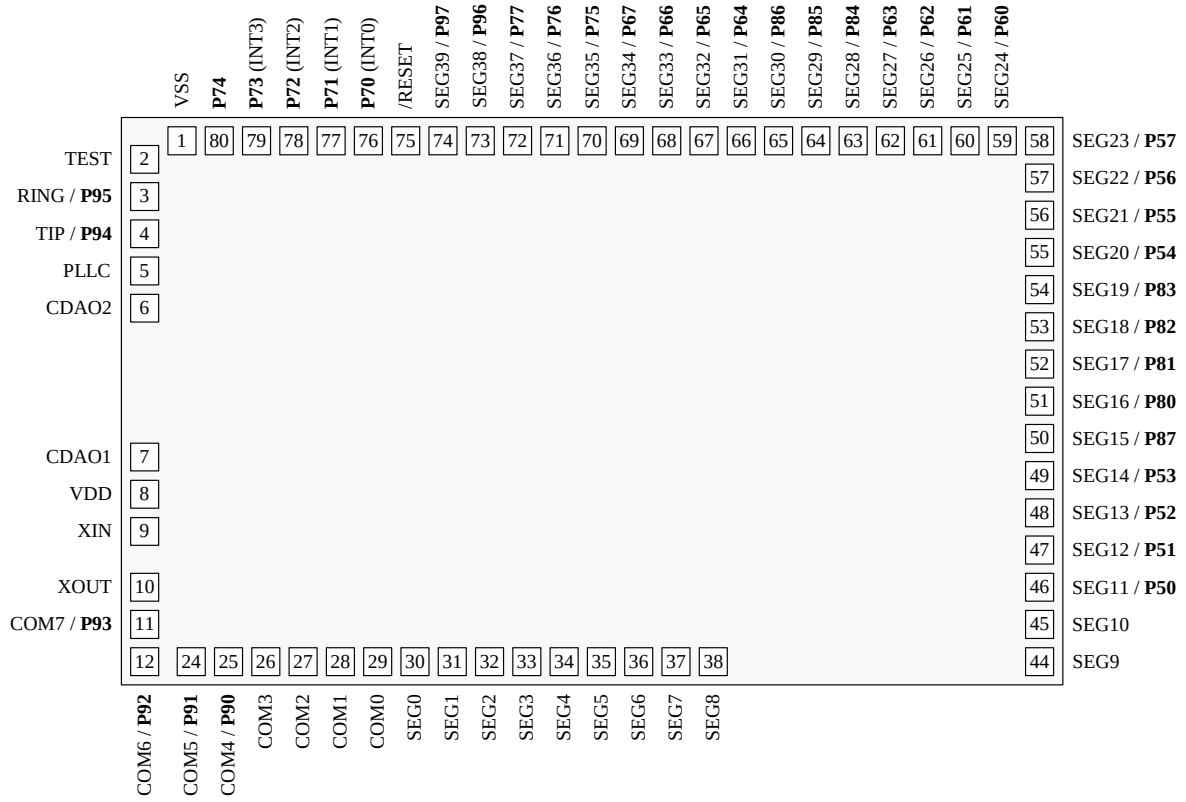


Fig 4-1 64-Pin Die Pin Assignment

5 Block Diagram

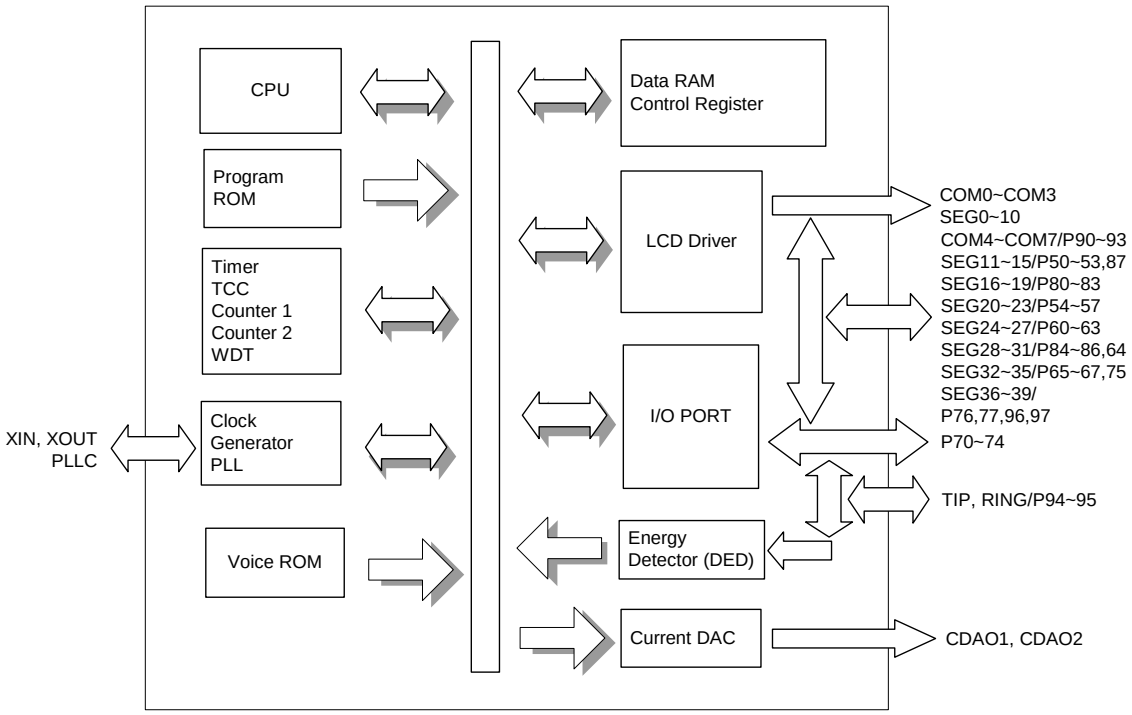


Fig 5-1 Block Diagram

6 Pin Description

Pin	I/O	Description	Num
Power			
VDD	PWR	Power VDD	1
VSS	GND	Ground GND	1
Clock for MCU			
XIN	I	Input pin for 32.768kHz crystal	1
XOUT	O	Output pin for 32.768kHz crystal	1
PLLC	I	Phase locked loop capacitor, connect a capacitor 0.01µ to 47µ to GND.	1
ERIC	I	Serially connect to VDD with a resistor when in ERIC mode. This is pin-shared with PLLC.	1
LCD Driver			
COM0~COM4	O	Common driver pins of LCD drivers	8
COM5~COM7	O (Port 9)	Common driver pins of LCD drivers These are pin-shared with P90 ~ P93.	4
SEG0~SEG10	O	Segment driver pins of LCD drivers	11
SEG11~SEG15	O (Port 5, 8)	Segment driver pins of LCD drivers These are pin-shared with P50 ~ P53, P87.	5
SEG16~SEG19	O (Port 8)	Segment driver pins of LCD drivers These are pin-shared with P80 ~ P83.	4
SEG20~SEG23	O (Port 5)	Segment driver pins of LCD drivers These are pin-shared with P54 ~ P57.	4
SEG24~SEG27	O (Port 6)	Segment driver pins of LCD drivers These are pin-shared with P60 ~ P63.	4
SEG28~SEG31	O (Port 8, 6)	Segment driver pins of LCD drivers These are pin-shared with P84 ~ P86, P64.	4
SEG32~SEG35	O (Port 6, 7)	Segment driver pins of LCD drivers These are pin-shared with P65 ~ P67, P75.	4
SEG36~SEG39	O (Port 7, 9)	Segment driver pins of LCD drivers These are pin-shared with P76 ~ P77, P96 ~ 97.	4
DED			
TIP	I (Port 9)	Differential-input Energy Detector, non-polarity pin This is pin-shared with P94	1
RING	I (Port 9)	Differential-input Energy Detector, non-polarity pin This is pin-shared with P95	1
Current DAC			
CDAO1	O	Current DA multiplexed output 1	1
CDAO2	O	Current DA multiplexed output 2	1
Test			
TEST	I	Test pin in test mode, normal low.	1
Reset			
/RESET	I	Reset input, Low enable	1

Pin	I/O	Description	Num
I/O			
P50 ~ P57	I/O Port 5	Port (0~1) are output only. Each bit in Port 5 (2~7) can be input or output port P50 ~ P57 are pin-shared with segment signals.	4
P60 ~ P67	I/O Port 6	Each bit in Port 6 can be input or output port. P60 ~ P67 are pin-shared with segment signals.	8
P70 ~ P77	I/O Port 7	Each bit in Port 7 can be input or output port. Port 7 has internal pull-high function. P76 ~ P77 have open drain function. P70/INT0 ~ P73/INT3 can be interrupt signals. P75 ~ P77 are pin-shared with segment signals.	6
P80 ~ P87	I/O Port 8	Each bit in Port 8 can be input or output port. P80 ~ P87 are pin-shared with segment signals.	4
P90 ~ P97	I/O Port 9	Each bit in Port 9 can be input or output port. P96, P97 have wake-up function. P90 ~ P93 are pin-shared with common signals. P94 ~ P95 are pin-shared with DED inputs. P96 ~ P97 are pin-shared with segment signals.	2

7 Function Description

7.1 Operational Registers

Register Configuration:

Addr	R Page Registers		IOC Page	
	R Page 0	R Page 1	IOC Page 0	IOC Page 1
00	**INDA** Indirect addressing			
01	**TCCD** TCC data			
02	**PC** Program Counter			
03	**STA** IOC Page, Status			
04	**RBSR** Register Bank, RSR			
05	**P5IOD** Port 5 high nibble I/O data, Program page	**CDADH** CDA input data high 8 bits	**P5IOC** Port 5 I/O Control, (P76, P77) open drain	**CDAC** Clear CDA, ASPCM rate and volume control
06	**P6IOD** Port 6 I/O data	**CDADL** CDA input data low 2 bits	**P6IOC** Port 6 I/O Control	**VRAH** VROM addr (16~17)
07	**P7IOD** Port 7 I/O data	**P5LIOD** Port 5 low nibble I/O data, port switch	**P7IOC** Port 7 I/O Control	**VRAM** VROM addr (8~15)
08	**P8IOD** Port 8 I/O date		**P8IOC** Port 8 I/O Control	**VRAL** VROM addr (0~7)

Addr	R Page Registers		IOC Page	
	R Page 0	R Page 1	IOC Page 0	IOC Page 1
09	**P9IOD** Port 9 I/O data		**P9IOC** Port 9 I/O Control	**VRD** VROM data
0A	**MCUC** CPU power saving, PLL, Main clock, VROM status, R page		**PSW** (P9, P8 low nibble, P5) switch, LCD bias, Key scan control	**DEDC** DAC stop, LCD mode, ROM & DA switch, DED control
0B	**RAMB** DED edge, DED output, CID RAM bank		**LCDA** LCD RAM address	**CN1D** Counter 1 data
0C	**RAMA** CID RAM address		**LCDD** LCD RAM data	**CN2D** Counter 2 data
0D	**RAMD** CID RAM data		Not existing	**P7PHC** Port 7 pull high
0E	**WUPC** CDA output selection, Port 8 high nibble, Switch, Wake-up control, LCD control		Not existing	**CNPSC** CNT1, 2 CLK source, CNT1, 2 prescaler
0F	**INTF** Interrupt flag		**INTM** Interrupt mask	
10 : 1F	16 bytes Common registers			
20 : 3F	Bank 0~Bank 3 Common registers (32×8 for each bank)			

Register Table:

No.	R Pg.	IOC Pg.	Register Name	Reg. Bit Name								PWR on RST Val.
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00	×	-	INDA	Indirect Address Register								-
01	×	-	TCCD	TCC data buffer								-
02	×	-	PC	Program Counter								-
03	×	-	STA	IOCPAGE	0	0	T	P	Z	DC	C	000×××××
04	×	-	RBSR	RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	00××××××
05	0	-	P5HIOD	P57	P56	P55	P54	PS3	PS2	PS1	PS0	××××0000
	1	-	CDADH	CDAD9	CDAD8	CDAD7	CDAD6	CDAD5	CDAD4	CDAD3	CDAD2	00000000
	-	0	P5IOC	IOC57	IOC56	IOC55	IOC54	0	0	0	0	11110000
	-	1	CDAC	0	0	0	0	0	0	0	0	00000000
06	0	-	P6IOD	P67	P66	P65	P64	P63	P62	P61	P60	××××××××
	1	-	CDADL	0	0	0	0	0	0	CDAD1	CDAD0	00000000
	-	0	P6IOC	IOC67	IOC66	IOC65	IOC64	IOC63	IOC63	IOC61	IOC60	11111111
	-	1	VRAH	0	0	0	0	0	VRA17	VRA17	VRA16	00000000
07	0	-	P7IOD	P77	P76	0	0	P73	P72	P71	P70	××××××××
	1		P5LIOD	PSW9	PSW8	PSW4	PSW1	P53	P52	P51	P50	1101××××
	-	0	P7IOC	IOC77	IOC76	0	0	IOC73	IOC73	IOC71	IOC70	11111111
	-	1	VRAM	VRA15	VRA14	VRA13	VRA12	VRA11	VRA10	VRA9	VRA8	00000000
08	×	-	P8IOD	P87	P86	P85	P84	P83	P82	P81	P80	××××××××
	-	0	P8IOC	IOC87	IOC86	IOC85	IOC84	IOC83	IOC83	IOC81	IOC80	11111111
	-	1	VRAL	VRA7	VRA6	VRA5	VRA4	VRA3	VRA2	VRA1	VRA0	00000000
09	×	-	P9IOD	P97	P96	P95	P94	P93	P92	P91	P90	××××××××
	-	0	P9IOC	IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90	1111××××
	-	1	VRD	0	0	0	0	VRD3	VRD2	VRD1	VRD 0	00000000
0A	×	-	MCUC	IDLE	ENPLL	CLK2	CLK1	CLK0	0	STA_VR	RPAGE	00000010
	-	0	PSW	PSW7	PSW6	PSW2	PSW3	BIAS3	BIAS2	BIAS1	SC	00000000
	-	1	DEDC	/DASTOP	0	0	LCDM	1	EGCLK	DEDPWR	DEDPWR	00001000
0B	×	-	RAMB	EDGE	0	0	0	DEDD	0	0	CALL_1	0000×000
	-	0	LCDA	0	0	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0	00000000
	-	1	CN1D	CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10	00000000
0C	×	-	RAMA	CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0	00000000
	-	0	LCDD	LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0	××××××××
	-	1	CN2D	CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20	00000000
0D	×	-	RAMD	CIDD7	CIDD6	CIDD5	CIDD4	CIDD3	CIDD2	CIDD1	CIDD0	××××××××
	-	0	Does not exist									
	-	1	P7PHC	PH7	PH6	0	0	PH3	PH2	PH1	PH0	00000000
0E	×	-	WUPC	DAOSEL	/WDTE	/WUP97	/WUP96	PSW5	LCD_C2	LCD_C1	/WUEDD	00000000
	-	0	Does not exist									
	-	1	CNPSC	CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0	00000000
0F	×	-	INTF	EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF	00000000
	-	0	INTM	EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF	00000000

7.2 Operational Registers Detail Description

7.2.1 R0 (INDA: Indirect Addressing Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov   A, @0x20    ;store a address at R4 for indirect addressing
Mov   0x04, A
Mov   A, @0xAA    ;write data 0xAA to R20 at bank0 through R0
Mov   0x00, A
```

7.2.2 R1 (TCCD: TCC Data Buffer)

This is incremented by an external signal edge applied to TCC, or by the instruction cycle clock. Written and read by the program as any other register. TCC has no reload function.

7.2.3 R2 (PC: Program Counter)

The Program Counter Organization structure is depicted in Fig 7-1.

The configuration structure generates 12K × 13 bit external ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then pushes into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address to be added to the current PC, and contents of the ninth and tenth bits do not change. The most significant bits (A10~A13) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

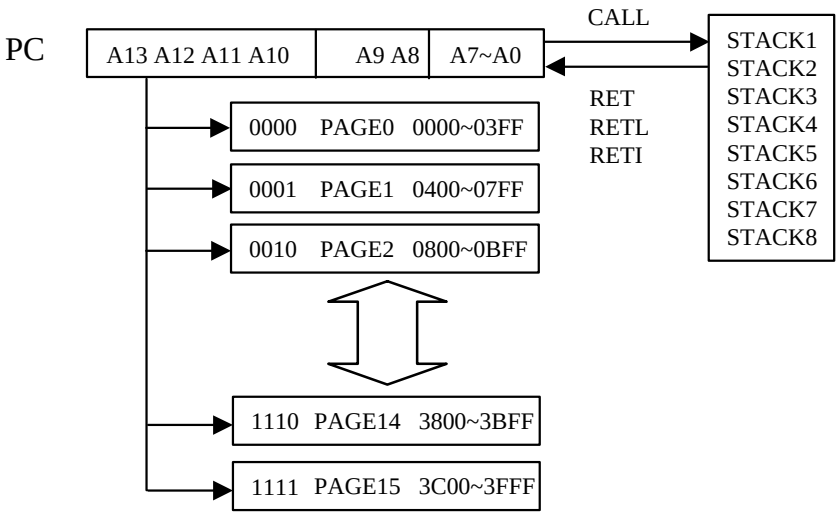


Fig 7-1 Program Counter Organization

The ROM size is 8K × 13bits. User does not need to use the A13 bit (PS3 in R5). The PS3 and PS2 bits in R5 are not writable and always return a zero after reading.

7.2.4 R3 (STA: IOC Page, Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCPAGE	0	0	T	P	Z	DC	C
R/W-0	R-0	R-0	R	R	R/W	R/W	R/W

Bit 0 (C): Carry flag

Bit 1 (DC): Auxiliary carry flag

Bit 2 (Z): Zero flag

Bit 3 (P): Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T): Time-out bit

Set to 1 by the "SLEP" & "WDTC" command, or during power up and reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	x	x : don't care

Bit 5 ~ Bit 6: unused

Always keep this bit to "0". Do not set it to "1" to prevent causing problems.

Bit 7 (IOCPAGE): change IOC5 ~ IOCE to another Page

"**0**" : IOCPage 0

"**1**" : IOCPage 1

7.2.5 R4 (RBSR: RAM Bank, RAM Selection for Common Registers R20 ~ R3F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5): Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1): Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the four banks of the 32 registers (R20 to R3F).

7.2.6 R5 (P5IOD, CDADH)

7.2.6.1 Page 0 (P5HIOD: Port 5 High Nibble I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	PS3	PS2	PS1	PS0
R/W	R/W	R/W	R/W	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 3 (PS0 ~ PS3): Page selection bits

These should be set before JMP or CALL instruction.

Page select bits

PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
:	:	:	:	:
:	:	:	:	:
1	0	1	0	Page 10
1	0	1	1	Page 11

User can use the PAGE instruction to change page and maintain the program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. The program page is maintained by EMC's compiler. It will change user's program by inserting instructions within the program.

Bit 4 ~ 7 (P54 ~ P57): 4-bit Port 5 I/O data register

7.2.6.2 Page 1 (CDADH: Current DAC Input Data Buffer High 8 Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CDAD9	CDAD8	CDAD7	CDAD6	CDAD5	CDAD4	CDAD3	CDAD2
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CDAD9 ~ CDAD2): Current D/A input data buffer high 8 bits

7.2.7 R6 (P6IOD, CDADL)

7.2.7.1 Page 0 (P6IOD: Port 6 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P60 ~ P67): 8-bit Port 6 (0~7) I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.7.2 Page 1 (CDADL: Current D/A Input Data Buffer Low 2 Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	CDAD1	CDAD0
R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (CDAD0 ~ CDAD1) : Current D/A input data buffer low 2 bits

Bit 2 ~ Bit 7: unused bits, read only

Always keep this bit to "0". Do not set it to "1" to prevent causing problems.

7.2.8 R7 (P7IOD, P5LIOD)

7.2.8.1 Page 0 (P7IOD: Port 7 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P70 ~ P77): 8-bit Port 7 I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.8.2 Page 1 (P5LIOD: Port 5 Low Nibble I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW9	PSW8	PSW4	PSW1	P53	P52	P51	P50
R/W-1	R/W-1	R/W-0	R/W-1	R/W	R/W	R/W	R/W

Bits 0 ~ 3 (P50 ~ P53) : 4-bit Port 5 I/O data register

P5 (0~1) are output port only but P5 (2~3) are bi-directional I/O. User can use IOC5 (2~3) register to define whether input or output for P5 (2~3).

Bit 4 (PSW1): Port Switch 1 for multiplexing I/O port and LCD segment

PSW1=0 → switch to P50~P53, P87

PSW1=1 (default) → switch to SEG11~SEG15

Bit 5 (PSW4) : Port Switch 4 for multiplexing I/O port and LCD segment

PSW4=0 (default) → switch to P60~P3

PSW4=1 → switch to SEG24~SEG27

Bit 6 (PSW8) : Port Switch 8 for multiplexing I/O port and DED input

PSW1=0 → switch to P94, P95 and power down DED block (DED function disabled)

PSW1=1 (default) → switch to TIP, RING

Bit 7 (PSW9): Port Switch 9 for multiplexing I/O port and LCD common

PSW4=0 → switch to P90~P93

PSW4=1 (default) → switch to COM4~COM7

7.2.9 R8 (P8IOD: Port 8 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P80 ~ P87): 8-bit Port 8 I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.10 R9 (P9IOD: Port 9 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97): 8-bit Port 9 I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.11 RA (MCUC: CPU Power Saving, PLL, Main Clock Selection, R Page)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	ENPLL	CLK2	CLK1	CLK0	0	STA_VR	RPAGE
R/W-0	R/W-0	R/W-0	R/W-0	RW-0	R-0	R-1	RW-0

Bit 0 (RPAGE): change R Page 5 to another page

"**0**" : R5 Page 0

"**1**" : R5 Page 1

Bit 1 (STA_VR): status flag for voice ROM operation

"**0**" : voice ROM busy

"**1**" : voice ROM data ready

When this flag is "0", the bus of voice ROM is busy and process its data. When this flag is "1", the bus of voice ROM is standby and its data is ready then user can read the data at this time.

Bit 2 = 0 : *unused bit, read only*

Always keep this bit to "0". Do not set it to "1" to prevent causing problems.

Bit 3 ~ 5 (CLK0 ~ CLK2): Main clock selection bits.

User can choose different frequency for the main clock by setting CLK1 and CLK2. All the clock selection are list below. When changing the main clock frequency, insert some NOP instruction for system stability.

PLLEN	CLK2	CLK1	CLK0	Sub Clock	Main Clock	CPU Clock
1	0	0	0	32.768kHz	447.829kHz	447.829kHz (Normal mode)
1	0	0	1	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	0	32.768kHz	1.791MHz	1.791MHz (Normal mode)
1	0	1	1	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	1	0	0	32.768kHz	7.165MHz	7.165MHz (Normal mode)
1	1	0	1	32.768kHz	10.747MHz	10.747MHz (Normal mode)
1	1	1	0	32.768kHz	14.331MHz	14.331MHz (Normal mode)
1	1	1	1	32.768kHz	17.913MHz	17.913MHz (Normal mode)
0	don't care	-	don't care	32.768kHz	don't care	32.768kHz (Green mode)

Bit 6 (ENPLL): PLL power control bit which is CPU mode control register

"**0**" : disable PLL

"**1**" : enable PLL

If PLL is enabled, the CPU will operate in normal mode (high frequency). Otherwise, it will run in green mode (low frequency, 32768 Hz).

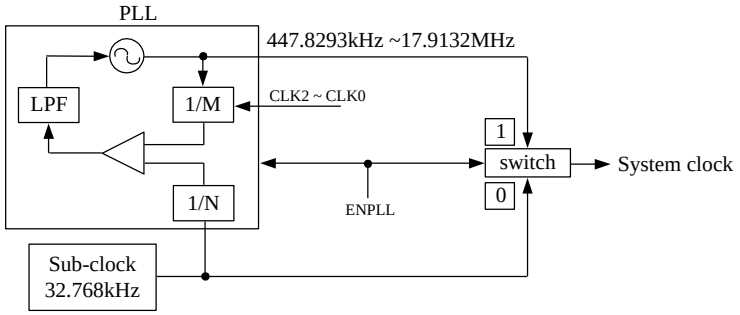


Fig 7-2 Correlation between 32.768kHz and Main Clock

Bit 7: unused

Always keep this bit to "0", Do not set it to "1" to prevent causing problems.

It can be waked up by a Watchdog timer (WDT), Ports 96~97, Ports 70~73 and run from “SLEP” next instruction.

Wake-up Signal	Sleep Mode	Green Mode	Normal Mode
	RA (7, 6)=(0, 0)+ SLEP	RA (7, 6)=(x, 0) not SLEP	RA (7, 6)=(x, 1) not SLEP
TCC time out EDD	x	Interrupt	Interrupt
WDT time out	RESET	RESET	RESET
Ports 96, 97	RESET	x	x
Ports 70~73	RESET	Interrupt	Interrupt

P70 ~ P73's wake-up function is controlled by IOCF P0 (1, 2, 3) and ENI instruction. P70's wake-up signal is a rising edge or falling edge defined by CONT Register Bit 7. Port 96, Port 97, Port 71, Port 72 and Port 73's wake-up pattern is a falling edge-trigger signal.

Energy Detector (DED) wakeup and interrupt signal can be controlled by RB Bit 7 (EDGE).

7.2.12 RB (RAMB: DED Output, CID RAM Banks)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EDGE	0	0	0	DEDD	0	0	CALL_1
R/W-0	R-0	R-0	R-0	R	R-0	R-0	R/W-0

Bit 0 (CALL_1): two blocks of Caller ID RAM area

By setting this bit from 0 to 1, user can use the 0.5K CID RAM with RC RAM address.

Bit 1 ~ Bit 2: unused, read only

Always keep this bit to “0”. Do not set it to “1” to prevent causing problems.

Bit 3 (DEDD): Output data of Energy Detector (DED)

If input signal from TIP pin and RING pin to Energy Detector is over the threshold level, setting at IOCA Page 1 Bit 0 (DEDTHD), the DED will extract the zero-crossing pulse waveform corresponding to input signal.

Bit 4 ~ Bit 6: unused, read only

Always keep this bit to “0”. Do not set it to “1” to prevent causing problems.

Bit 7 (EDGE): Wake-up and interrupt trigger edge control of Energy Detector (DED) output

"**0**" : Falling edge trigger

"**1**" : Rising edge & Falling edge trigger

7.2.13 RC (RAMA: CID RAM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CIDA0 ~ CIDA7): Caller ID (CID) RAM address

User can select Caller ID RAM address from 0 to 255.

7.2.14 RD (RAMD: CID RAM Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CIDD7	CIDD6	CIDD5	CIDD4	CIDD3	CIDD2	CIDD1	CIDD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CIDD0 ~ CIDD7): Caller ID RAM data register.

7.2.15 RE (WUPC: CDA Output Selection Wake-up Control, LCD Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAOSEL	/WDTE	/WUP97	/WUP96	PSW5	LCD_C2	LCD_C1	/WUEDD
R/W-0	R/W-0	R/W-0	R/W-0	RW-0	R/W-0	R/W-0	R/W-0

Bit 0 (/WUEDD) : Wake-up control of Energy Detector (DED) output data

"**0**" : Disable

"**1**" : Enable

Bit 1 ~ Bit 2 (LCD_C1 ~ LCD_C2): LCD display enable or blanking.

The display duty change must set the (LCD_C2, LCD_C1) to (0, 0).

(LCD_C2, LCD_C1)	LCD Display Control	Duty Bias
(0, 0)	Disable (turn off LCD)	1/4*
(0, 1)	Blanking	:
(1, 1)	LCD display enable	:

*1/8 or 1/4 duty depends on IOCE Page 1 Bit 0 (LCDM)

Bit 3 (PSW5) : Port Switch 5 for multiplexing I/O port and LCD segment

PSW5=0 → switch to P84~P86, P64

PSW5=1 (not allowed to set for ICE807C) → switch to SEG28~SEG31

For ICE807C, always keep this bit to default value "0" to avoid malfunction.

Bit 4 (/WUP96): Port 9 Bit 6 wake-up control, 1/0 → enable/disable

Bit 5 (/WUP97): Port 9 Bit 7 wake-up control, 1/0 → enable/disable

Bit 6 (/WDTE): Watchdog Timer enable control, 1/0 → enable/disable

Bit 7 (DAOSEL): Current D/A output selection

"**0**" : Current D/A output to “CDAO1” pin

"**1**" : Current D/A output to “CDAO2” pin

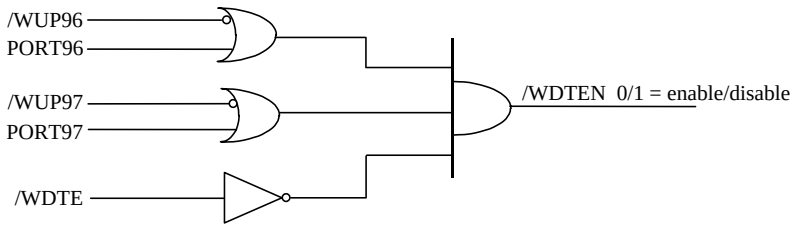


Fig 7-3 Wake-up Function and Control Signal

7.2.16 RF (INTF: Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (TCIF): TCC timer overflow interrupt flag

It will be set when TCC timer overflows.

Bit 1 (INT0): External INT0 pin interrupt flag

It can be used when Port 70 is set as input port.

Bit 2 (INT1): External INT1 pin interrupt flag

It can be used when Port 71 is set as input port.

Bit 3 (INT2/INT3): external INT2 and INT3 pin interrupt flag

It can be used when Port 72 or Port 73 is set as input port.

Bit 4 (CNT1): 8 bit Counter 1 overflow interrupt flag.

It will be set when Counter 1 overflows.

Bit 5 (CNT2): 8 bit Counter 2 overflow interrupt flag.

It will be set when Counter 2 overflows.

Bit 6 = 0 : unused bit and always “0”, read only

Bit 7 (EDD): Interrupt flag of Energy Detector (DED) output data

"1" means interrupt request and "0" means non-interrupt. INT0~INT3 interrupts are edge triggered (falling edge or rising edge) which can be set by CONT Bit 7 (INT_EDGE). Interrupt edge control of DED output data is set by RB Bit 7 (EDGE). See corresponding interrupt mask in IOCF register. User can read and clear.

7.2.17 R10~R3F (General Purpose Register)

R10~R3F (Banks 0~3) are all general purpose registers.

7.3 Special Purpose Registers

7.3.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

7.3.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	0	PAB	PSR2	PSR1	PSR0
R/W-1	R/W-0	R/W-1	R-0	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 2 (PSR0 ~ PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler assigned bit

"**0**" : TCC
"**1**" : WDT

Bit 4: unused

Bit 5 (TS) TCC signal source

"**0**" : instruction clock
"**1**" : 16.38kHz

Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See Fig 7-2.

Bit 6 (INT): INT enable flag

"**0**" : interrupt masked by DISI or hardware interrupt
"**1**" : interrupt enabled by ENI/RETI instructions

Bit 7(INT_EDGE): interrupt edge type of P70

"**0**" : P70 's interrupt source is a rising edge signal and falling edge signal
"**1**" : P70 's interrupt source is a falling edge signal

CONT register is readable (CONTR) and writable (CONTW).

7.3.3 IOC5 (P5IOC, CDAC)

7.3.3.1 Page 0 (P5IOC: Port 5 I/O Control, P7 (7, 6) Open Drain)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	OP77	OP76
R/W-1	R/W-1	R/W-1	R/W-1	RW-1	RW-1	R/W-0	R/W-0

Bit 0 ~ Bit 1 (OP76 ~ OP77) : P76 ~ P77 open-drain control

"**0**" : disable

"**1**" : enable

Bit 2 ~ 7 (IOC52 ~ IOC57): Port 5 I/O direction control register

"**0**" : put the relative I/O pin as output

"**1**" : put the relative I/O pin into high impedance

7.3.3.2 Page 1 (CDAC: Clear CDA Data, Current D/A Reference Current Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLDA	0	0	0	VOL3	VOL2	VOL1	VOL0
R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (VOL0 ~ VOL3): Current D/A reference current control

VOL3 ~ VOL0	Reference Current (mA)
0000	***0 or (5 x 1/16 mA = 0.3125mA)***
0001	5 x 2/16 mA = 0.625 mA
0010	5 x 3/16 mA = 0.9375 mA
0011	5 x 4/16 mA = 1.25 mA
0100	5 x 5/16 mA = 1.5625 mA
0101	5 x 6/16 mA = 1.875 mA
0110	5 x 7/16 mA = 2.1875 mA
0111	5 x 8/16 mA = 2.5 mA
1000	5 x 9/16 mA = 2.8125 mA
1001	5 x 10/16 mA = 3.125 mA
1010	5 x 11/16 mA = 3.4375 mA
1011	5 x 12/16 mA = 3.75 mA
1100	5 x 13/16 mA = 4.0625 mA
1101	5 x 14/16 mA = 4.375 mA
1110	5 x 15/16 mA = 4.6875 mA
1111	5 mA

Note: In setting VOL3 ~ VOL0 = 0, the reference current is dependent on Bit 1 (CDAR) value. Refer to Section 7.9 on Code Option Register.

Bit 4 ~ Bit 6: unused bits and always “0”, read only

Bit 7 (CLDA) : Current D/A data clear enable control

"**0**" : disable

"**1**" : enable

When this bit is set (enabled), the internal Current D/A data will be cleared and its output will go to ground level with CDAO pin connecting a resistor to ground. After setting this bit, remember to clear (disable) it again otherwise it will keep the output to ground level no matter if the voice ROM is playing or not.

7.3.4 IOC6 (P6IOC, VRAH)

7.3.4.1 Page 0 (P6IOC : Port 6 I/O Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC60 ~ IOC67): Port 6 I/O direction control registers

"**0**" : put the relative I/O pin as output

"**1**" : put the relative I/O pin into high impedance

7.3.4.2 Page 1 (VRAH: Voice ROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	VRA18	VRA17	VRA16
R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (VRA16 ~ VRA18) : Voice ROM address register bit

Bit 3 ~ Bit 7 = 0 : undefined bits and always “0”, read only

Voice ROM address can access a maximum of 304k-1, where k = 1024. Addresses over these are non-existent.

7.3.5 IOC7 (P7IOC, VRAM)

7.3.5.1 Page 0 (P7IOC: Port 7 I/O Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC70 ~ IOC77): Port 7 I/O direction control register

"**0**" : put the relative I/O pin as output

"**1**" : put the relative I/O pin into high impedance

7.3.5.2 Page 1 (VRAM: Voice ROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRA15	VRA14	VRA13	VRA12	VRA11	VRA10	VRA9	VRA8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (VRA8 ~ VRA15): voice ROM address register bit

Voice ROM address can access a maximum of 304k-1, where k = 1024. Addresses over these are non-existent.

7.3.6 IOC8 (P8IOC, VRAL)

7.3.6.1 Page 0 (P8IOC : Port 8 I/O Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC80 ~ IOC87): Port 8 I/O direction control register

"**0**" : put the relative I/O pin as output

"**1**" : put the relative I/O pin into high impedance

7.3.6.2 Page 1 (VRAL: Voice ROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRA7	VRA6	VRA5	VRA4	VRA3	VRA2	VRA1	VRA0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (VRA0 ~ VRA7) : Voice ROM address register bit

Voice ROM address can access a maximum of 304k-1, where k = 1024. Addresses over these are non-existent.

7.3.7 IOC9 (P9IOC, VRD)

7.3.7.1 PAGE 0 (P9IOC: Port 9 I/O Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97): Port 9 I/O direction control register

"**0**" : put the relative I/O pin as output

"**1**" : put the relative I/O pin into high impedance

7.3.7.2 Page 1 (VRD: Voice ROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	VRD3	VRD2	VRD1	VRD0
R-0	R-0	R-0	R-0	R	R	R	R

Bit 0 ~ Bit 3 (VRD0 ~ VRD3) : 4-bit Voice ROM data register

Bit 4 ~ Bit 7 =0 : unused bits and always “0”, read only

7.3.8 IOCA (PSW, DEDC)

7.3.8.1 Page 0 (PSW: Ports 7, 9, 8, 5 Switch, LCD Bias, Key Scan)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW7	PSW6	PSW2	PSW3	BIAS3	BIAS2	BIAS1	SC
RW-0	RW-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (SC): Key scan control function

"**0**" : disable the Key scan control function

"**1**" : enable the Key scan control function

Once this bit is enabled, all of the LCD signals will have a low pulse during a common period. This pulse has 30µs width.

Use the following procedure to implement the key scan function:

1. Set Port 7 as an input port
2. Set IOCD Page 1 to enable Port 7 pull-high function
3. Enable key scan function
4. Push a key once. Set RA Bit 6 to enable the PLL (CPU will run in normal mode)
5. Disable the key scan function
6. Set I/Os shared with LCD segment's port switch PSW =0. For example, set PSW2=0 and/or PSW3=0. Port 5 and/or Port 8 sent probe signal to Port 7 and read Port 7. Get the key.
7. Note that a probe signal should delay an instruction at least to another probe signal.
8. Set PSW2 =1 and/or PSW3=1. Port 5 and/or Port 8 as LCD signal

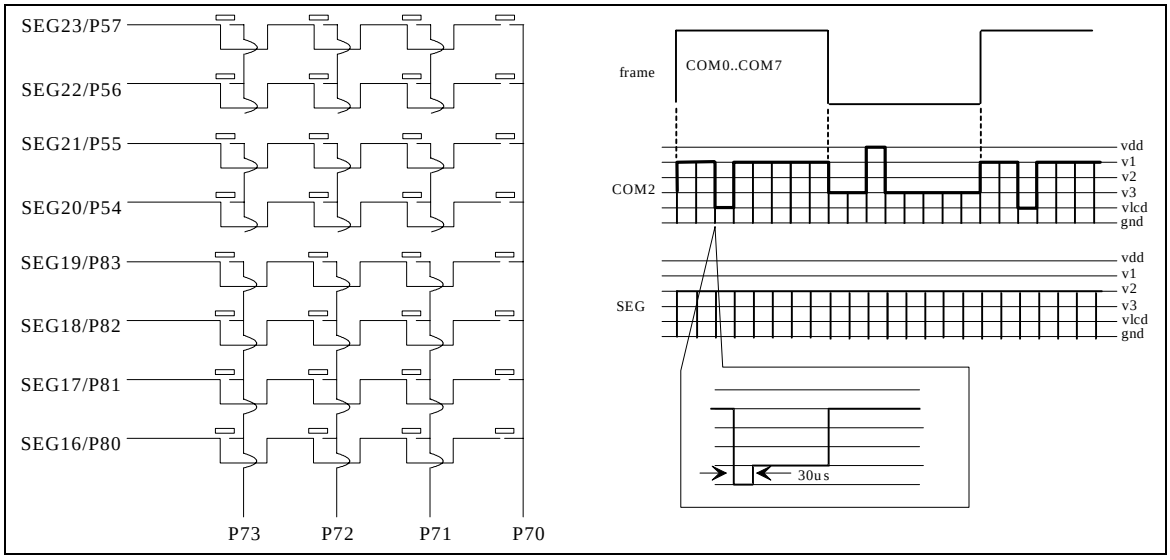


Fig 7-4 Key Scan Circuit

Bit 1 ~ 3 (BIAS1 ~ BIAS3): LCD bias control is used to choose the LCD operation voltage.

(BIAS3, BIAS2, BIAS1)	Vop (VDD 3.3V)	VDD=3.3V
(0,0,0)	0.60VDD	1.98V
(0,0,1)	0.66VDD	2.18V
(0,1,0)	0.74VDD	2.44V
(0,1,1)	0.82VDD	2.71V
(1,0,0)	0.87VDD	2.87V
(1,0,1)	0.93VDD	3.07V
(1,1,0)	0.96VDD	3.17V
(1,1,1)	1.00VDD	3.30V

Bit 4 (PSW3): Port Switch 3 for multiplexing I/O port and LCD segment

PSW3=0 → switch to P54~P57

PSW3=1 → switch to SEG20~SEG23

Bit 5 (PSW2): Port Switch 2 for multiplexing I/O port and LCD segment

PSW2=0 → switch to P80~P83

PSW2=1 → switch to SEG16~SEG19

Bit 6 (PSW6): Port Switch 6 for multiplexing I/O port and LCD segment

PSW6=0 → switch to P65~P67, P75

PSW6=1 *(not allowed to set for ICE807C* → switch to SEG32~SEG35

For ICE807C, always keep this bit to default value “0” to avoid malfunction.

Bit 7(PSW7) : Port Switch 7 for multiplexing I/O port and LCD segment

PSW7=0 → switch to P76~P77, P96~P97

PSW7=1 *(not allowed to set for ICE807C)* → switch to SEG36~SEG39

For ICE807C, always keep this bit to default value "0" to avoid malfunction.

7.3.8.2 Page 1 (DEDC: DAC Power Control, LCD Mode, DED Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/DASTOP	0	0	LCDM	1	EGCLK	DEDPWR	DEDTHD
R/W-0	R-0	R-0	R/W-0	R-1	R/W-0	R/W-0	R/W-0

Bit 0 (DEDTHD): The minimum detection threshold of Dual Input Energy Detector (DED)

"**0**" : -45dBm

"**1**" : -30dBm

Bit 1 (DEDPWR) : Power control of Energy Detector (DED)

"**0**" : Power off

"**1**" : Power on

Bit 2 (EGCLK) : Operating clock for Energy Detector (DED)

"**0**" : 32.768kHz

"**1**" : 3.5826MHz

This bit is used to select the operating clock for the Energy Detector (DED). When this bit is set to "1", the PLL is also enabled regardless of RA Bit 6 (ENPLL) value. At this time, the Energy detector works at high frequency mode. When this bit is set to "0", the Energy Detector works at low frequency mode. The difference between high frequency mode and low frequency is as follows.

EGCLK	ENPLL	Energy Detector Status	PLL Status
0	0	32.768kHz operating clock	PLL is disabled
-	1	Normal detection Small current consumption	PLL is enabled
1	x	3.5826MHz operating clock Accurate detection More current consumption	PLL is enabled

Note: "x" means don't care

Bit 3: unused bit and always "1", read only

Bit 4 (LCDM): LCD mode control for 8-COM, 1/8 duty or 4-COM, 1/4 duty selection

"**0**" : 8-COM mode selection and COM0 ~ COM7 are enabled

"**1**" : 4-COM mode selection and COM0 ~ COM3 are enabled

Bit 5 ~ Bit 6: unused bits and always "0", read only

Bit 7 (DASTOP): D/A stop conversion and power down

"**0**" : Disable and power down D/A

"**1**" : Enable and power on D/A

7.3.9 IOCB (LCDA, CN1D)

7.3.9.1 Page 0 (LCDA: LCD RAM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 5 (LCDA0 ~ LCDA5): LCD RAM address

The LCD display data is stored in the data RAM. The correlation between data area and COM/SEG pin is shown below:

COM7 ~ COM0	Segment
00H (Bit 7 ~ Bit 0)	SEG0
01H	SEG1
:	:
:	:
26H	:
27H	SEG39
28H ~ 1FH	(empty)

Bit 6 ~ Bit 7 = 0: unused and always “0”, read only

7.3.9.2 Page 1 (CN1D: Counter 1 Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17): Counter 1’s buffer that user can read and write

Counter 1 is an 8-bit up-counter preset and read out register (write = preset). Counter 1 has reload function. After an interrupt, it will reload the preset value.

7.3.10 IOCC (LCDD, CN2D)

7.3.10.1 Page 0 (LCDD: LCD RAM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (LCDD0 ~ LCDD7): LCD data buffer for LCD RAM read or write

7.3.10.2 Page 1 (CN2D: Counter 2 Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN20 ~ CN27): Counter 1’s buffer that user can read and write

Counter 2 is an 8-bit up-counter preset and read out register (write = preset). Counter 1 has reload function. After an interrupt, it will reload the preset value.

7.3.11 IOCD (P7PHC, Port 7 Pull-high Control)

- Page 0

  IOCD Page 0 does not exist and always returns a zero after reading.

- Page 1 (P7PHC: Port 7 Pull-high Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 7 (PH0 ~ PH7): Port 7 pull-high control bits

"**0**" : disable internal pull-high control bit

"**1**" : enable internal pull-high control bit

These control bits are used to enable the pull-high of Port 7 pins.

7.3.12 IOCE (CNPSC)

- Page 0

  IOCE Page 0 does not exist and always returns a zero after reading.

- Page 1 (CNPSC: Counters 1, 2 clock source and Prescaler)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 2 (C1_PSC1~ C2_PSC2) : Counter 1 prescaler setting

Reset = (0,0,0)

(C1_PSC2, C1_PSC1, C1_PSC0)	Prescaler Ratio
(0,0,0)	1:1
(0,0,1)	1:2
(0,1,0)	1:4
(0,1,1)	1:8
(1,0,0)	1:16
(1,0,1)	1:32
(1,1,0)	1:64
(1,1,1)	1:128

Bit 3 (CNT1S): Counter 1 source

"**0**" : 32.768 kHz

"**1**" : Instruction clock, where instruction clock period = 2 × Main clock period

Bit 4 ~ 6 (C2_PSC1~ C2_PSC2): Counter 2 prescaler setting

Reset = (0,0,0)

(C2_PSC2,C2_PSC1,C2_PSC0)	Scaler ratio
(0,0,0)	1:1
(0,0,1)	1:2
(0,1,0)	1:4
(0,1,1)	1:8
(1,0,0)	1:16
(1,0,1)	1:32
(1,1,0)	1:64
(1,1,1)	1:128

Bit 7 (CNT2S): Counter 2 source

"**0**" : 32.768 kHz

"**1**" : Instruction clock, where instruction clock period = 2 × Main clock period

7.3.13 IOCF (INTM: Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EDD	0	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bits 0 ~ 5, Bit 7: interrupt enable bit

"**0**" : disable interrupt

"**1**" : enable interrupt, where instruction clock period = 2 × Main clock period

Bit 6 = 0 : unused bit and always “0”, read only

IOCF Register is readable and writable, works with RF registers.

7.4 TCC/WDT Prescaler

An 8-bit counter is provided as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8 bit counter available either for TCC or WDT is determined by the status of Bit 3 (PAB) of the CONT register.
- See the prescaler ratio in the CONT register.
- Fig. 7-5 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to the TCC each time there is an instruction execution.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

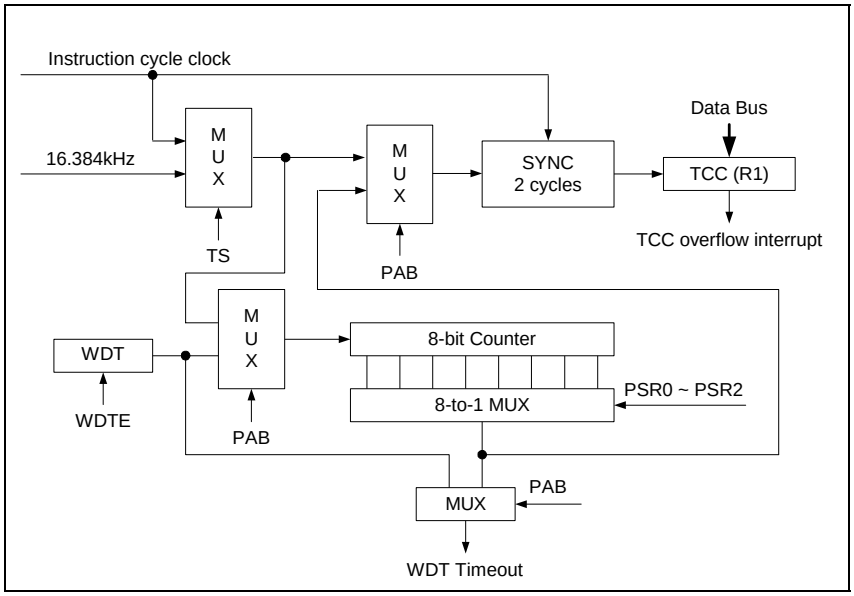


Fig 7-5 Block Diagram of TCC WDT

7.5 I/O Ports

The I/O registers, Port 5 ~ Port 9, are bi-directional tri-state I/O ports. Port 7 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC6 ~ IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig 7-6.

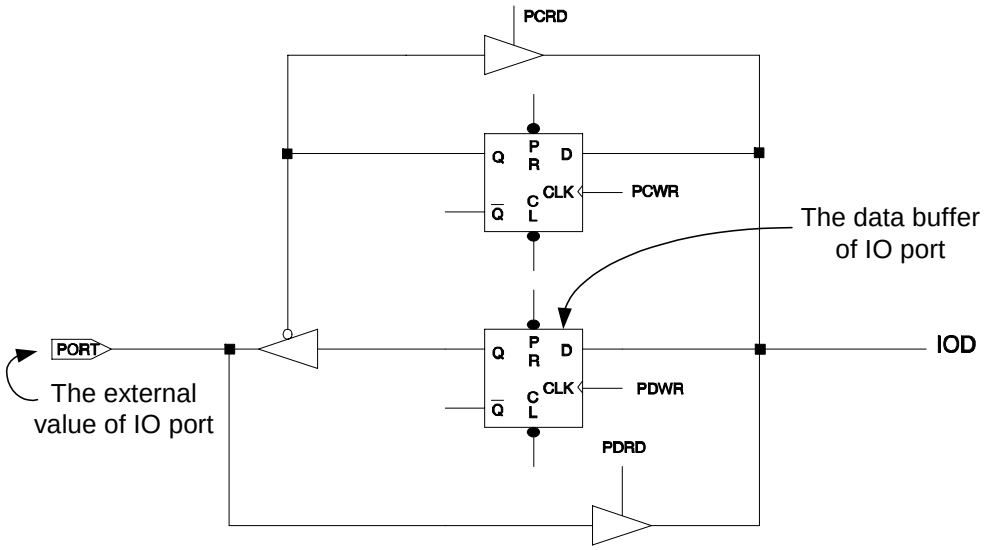


Fig 7-6 I/O Port and I/O Control Register Circuits

It should be noted that for an output port, several instructions operate with the external value instead of the data buffer of the relative IO port. For example, user puts Port 7 as an output port and set the data buffer (R7 Page 0) to “0xFF”, but the external value of Port 7 Bit 0 is still low voltage (maybe this pin is connected to a large loading device or a pull-low circuit). For this situation, the result of instruction “MOV A, 0x07” will be “0xFE” instead of “0xFF”. The affected instructions are listed as shown below:

SUB R, A	SUB A, R	DECA R	DECR
OR A, R	OR R, A	AND A, R	AND R, A
XOR A, R	XOR R, A	ADD A, R	ADD R, A
MOV A, R	MOV R, R	COMA R	COM R
INCA R	INC R	DJZA R	DJZ R
RRCA R	RRC R	RLCA R	RLC R
SWAPA R	SWAP R	JZA R	JZ R
BC R, b	BS R, b	JBC R, b	JBS R, b

7.6 Reset and Wake-up

A Reset can be caused by

1. External /RESET pin
2. Power-on reset or Power-on voltage detector reset (/POVD reset)
3. WDT timeout. (if enabled and in Green or Normal mode)

Note that only Power-on reset, or only Power-on voltage detector reset in Case (2) is enabled in the system by Code Option bit. If /POVD is disabled, Power-on reset is selected in Case (2). Refer to Fig 7-7.

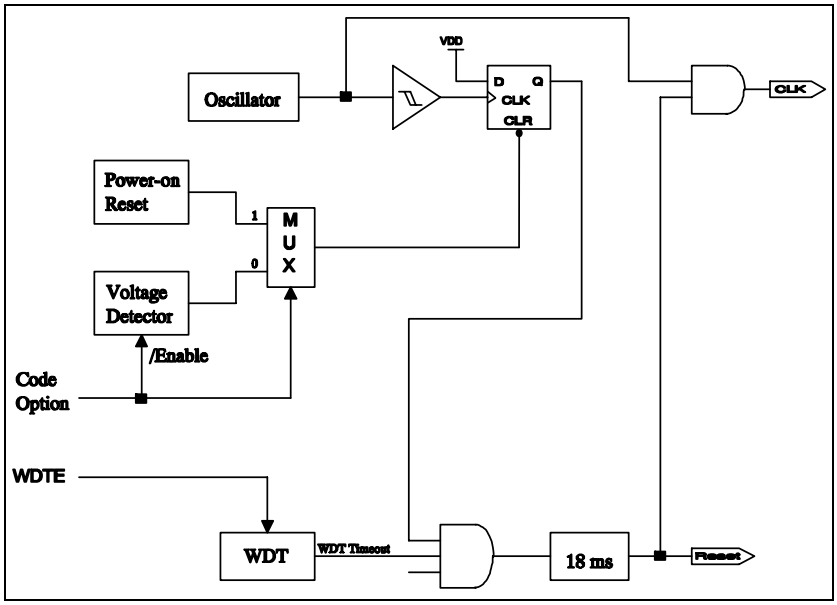


Fig 7-7 Controller Reset Block Diagram

Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power is on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The following table shows the status of the other registers (Bit 7 ~ Bit 0):

R5 = "xxxx0000"	IOC5 = "1111xxxx"	
R6 = Port	IOC6 = "11111111"	
R7 = Port	IOC7 = "11111111"	
R8 = Port	IOC8 = "11111111"	
R9 = Port	IOC9 = "11111111"	
RA = "00110000"	Page0 IOCA = "00000000"	Page1 IOCA = "00000000"
RB = "0000x000"	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000"	Page0 IOCC = "xxxxxxxx"	Page1 IOCC = "00000000"
RD = "xxxxxxxx"	Page0 IOCD = "00000000"	Page1 IOCD = "00000000"
RE = "x0000000"	Page0 IOCE = "00000000"	Page1 IOCE = "00000000"
RF = "00000000"	IOCF = "00000000"	

The controller can be awakened from Sleep mode or Idle mode (execution of “SLEP” instruction) by (1) TCC time out (Idle mode only), (2) WDT time-out (if enabled), (3) external input at Port 9, and (4) Energy detector (DED) output data. The four cases will cause the controller to wake up and proceed with the next instruction in Idle mode, and reset in Sleep mode. After the CPU wakes up, user should control the Watchdog in case of reset in Green mode or Normal mode. The last three should be opened in the RE register before going into Sleep mode or Idle mode. The first case will set a flag in RF Bit 0. It will go to address 0x08 when TCC generates an interrupt.

7.7 Interrupt

The EM78807 has internal interrupts, namely; TCC timer overflow interrupt and two 8-bit counters overflow interrupt. These are falling edge triggered.

If these interrupt sources change signal from high to low, then the RF register will generate a '1' flag to the corresponding register if the IOCF register is enabled.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) occur, it will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared by software before leaving the interrupt service routine, and before enabling other interrupts to avoid recursive interrupts.

There are four external interrupt pins including INT0, INT1, INT2 and INT3. And four internal counters interrupt available.

External interrupt INT0, INT1, INT2, INT3 signals are from Port 7 Bit 0 to Bit 3. If IOCF is enabled, then these signals will cause interrupt, or these signals will be treated as general input data.

After a reset, the next instruction will be fetched from address 000H, the instruction interrupt is 001H and the hardware interrupt is 008H.

TCC will go to address 0x08 in Green mode or Normal mode after time out. These two cases will set an RF flag.

7.8 Instruction Set

The instruction set has the following features:

- Every bit of any register can be set, cleared, or tested directly.
- The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Legend:

R = Register designator that specifies which one of the 64 registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None
0 0000 0010 0000	0020	TBL	R2+A → R2 Bits 9,10 do not clear	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1 1110 1000 kkkk	1E8k	PAGE k	K->R5	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

7.9 Code Option Register

The IC has one Code option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution and can be set when downloading the program code.

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	-	-	-	-	CDAR	/POVD

Bit 0 (/POVD): Power-on voltage detector reset

"**0**" : enable

"**1**" : disable

/POVD	1.8V /POVD Reset	1.6V Power-on Reset	Sleep Mode Current
0	yes	no	6μA
1	no	yes	1μA

Note: When /POVD is disabled, the CPU reset is by power-on reset circuit. When /POVD is enabled, the CPU reset is by /POVD reset circuit.

Bit 1 (CDAR): Current D/A reference current control option

Control option for IOC5 Page 1 Bit 3 ~ Bit 0 (VOL3 ~ VOL0) = 0. This code option won't effect the reference current value for VOL3 ~ VOL0 = 1 ~ 15.

0 → set to 0.3125mA

VOL3 ~ VOL0	Reference Current (mA)
0000	5 x 1/16 mA = 0.3125 mA

1 → set to 0

VOL3 ~ VOL0	Reference Current (mA)
0000	0

7.10 Energy Detector (DED)

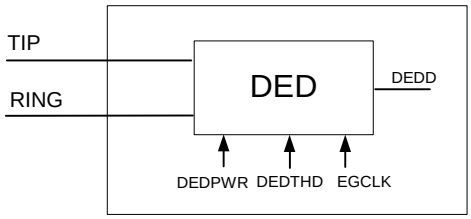


Fig 7-8 DED Diagram

The Energy Detector is differential input and zero crossing detector named as DED. It can detect any incoming AC signal above its threshold level and output corresponding zero-crossing frequency pulse. For very low power concern, there is no signal filtering circuit in the DED circuit so user needs to have his software algorithm to determine incoming signal by reading its output DEDD bit. For this energy detector, user can set its minimum detection threshold level at –30dBm or –45dBm by DEDTHD bit. All the minimum detection value can be achieved under input capacitor around 1000pF ~ 4700pF and input resistor around 22K ~ 100 KΩ. The energy detector has power control by IOCA Page 1 Bit 1 (DEDPWR).

Energy Detector Register bits:

Register Bits	Descriptions
RB Bit 3 (DEDD)	DEDD : Output data of DED
RB Bit 7 (EDGE)	EDGE : edge control of DED output data **0** : Falling edge trigger **1** : Rising edge trigger & Falling edge trigger
RE Bit 0 (/WUEDD)	/WUEDD : Wake-up control of DED output data **0** : disable **1** : enable
RF Bit 7 (EDD)	EDD : Interrupt flag of DED output data
IOCF Bit 7 (EDD)	EDD : Interrupt mask of DED output data **0** : disable interrupt of EDD output data **1** : enable interrupt of EDD output data
IOCA Page 1 Bit 0 (DEDTHD)	DEDTHD : Minimum detection threshold of DED **0** : -45dBm **1** : -30dBm
IOCA Page 1 Bit 1 (DEDPWR)	DEDPWR : Power control of DED **0** : power off **1** : power on
IOCA Page 1 Bit 2 (EGCLK)	Bit 2 (EGCLK) : Operating clock for DED **0** : 32.768kHz **1** : 3.5826MHz

7.11 LCD Driver

The system can drive an LCD directly, which has 40 segments and 8 commons that can drive a total of 40×8 dots. LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating power supply pins.

The duty, bias, number of segments, number of commons and frame frequency are determined by the LCD mode register and LCD control register.

The basic structure contains a timing control which uses the basic frequency of 32.768 kHz to generate the proper timing for different duty and display access. The RE register is a command register for the LCD driver, the LCD display (disable, enable, blanking) is controlled by LCD_C and the driving duty and bias is determined by LCD_M and the display data is stored in the data RAM of which address and data access is controlled by registers RC and RD.

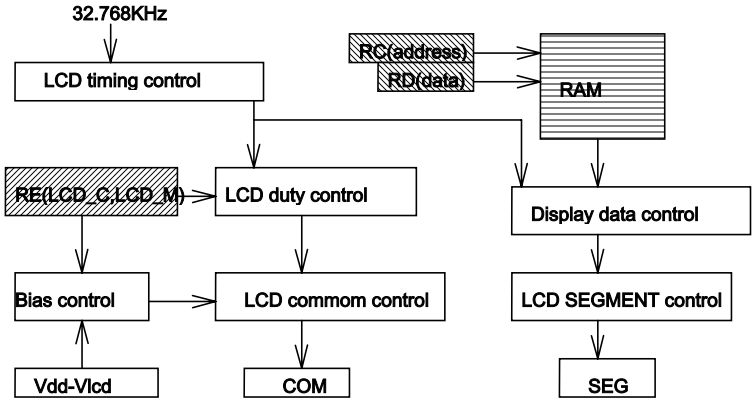


Fig 7-9 LCD Driver Control

7.11.1 LCD Driver Control

RE (LCD Driver Control) (Initial state "00000000")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	LCD_C2	LCD_C1	-

Bits 1 ~ 2 (LCD_C1, LCD_C2) : LCD display enable or blanking

The display duty change must set the (LCD_C2, LCD_C1) to (0, 0).

(LCD_C2, LCD_C1)	LCD Display Control	Duty Bias
(0, 0)	Disable(turn off LCD)	1/4 *
(0, 1)	Blanking	:
(1, 1)	LCD display enable	:

* 1/8 or 1/4 duty depends on IOCE Page 1 Bit 4 (LCDM)

7.11.2 LCD Display Area

The LCD display data is stored in the data RAM. The correlation between data area and COM/SEG pin is shown below:

COM7 ~ COM0	Segment
00H (Bit 7 ~ Bit 0)	SEG0
01H	SEG1
:	:
:	:
26H	:
27H	SEG39
28H ~ 1FH	(empty)

IOCB (LCD Display RAM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

Bit 0 ~ Bit 5: select LCD Display RAM addresses up to 39.

IOCC (LCD Display data): Bit 0 ~ Bit 5 are LCD data. The LCD RAM can be read or written to, whether enabled or disabled.

7.11.3 LCD COM and SEG Signal

COM signal: The number of COM pins varies according to the duty cycle used, as shown in the following:

1/8 duty or 1/4 duty mode

	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
1/8	o	o	o	o	o	o	o	o
1/4	o	o	o	o	x	x	x	x

Note: x: open **o:** select

SEG signal: The 40 segment signal pins are connected to the corresponding display RAM address 0 to 39. The high bit and the low bit (Bit 7 down to Bit 0) are correlated to COM7 to COM0 respectively. For 8-COM mode, COM7 to COM0 and LCD RAM IOCC Page 0 Bits 0~7 are used. For 4-COM mode, COM3 to COM0 and LCD RAM only IOCC Page 0 Bit 0~Bit 3 are used.

When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0, a non-select signal is sent to the corresponding segment pin.

COM, SEG and Select/Non-select signal is shown as follows:

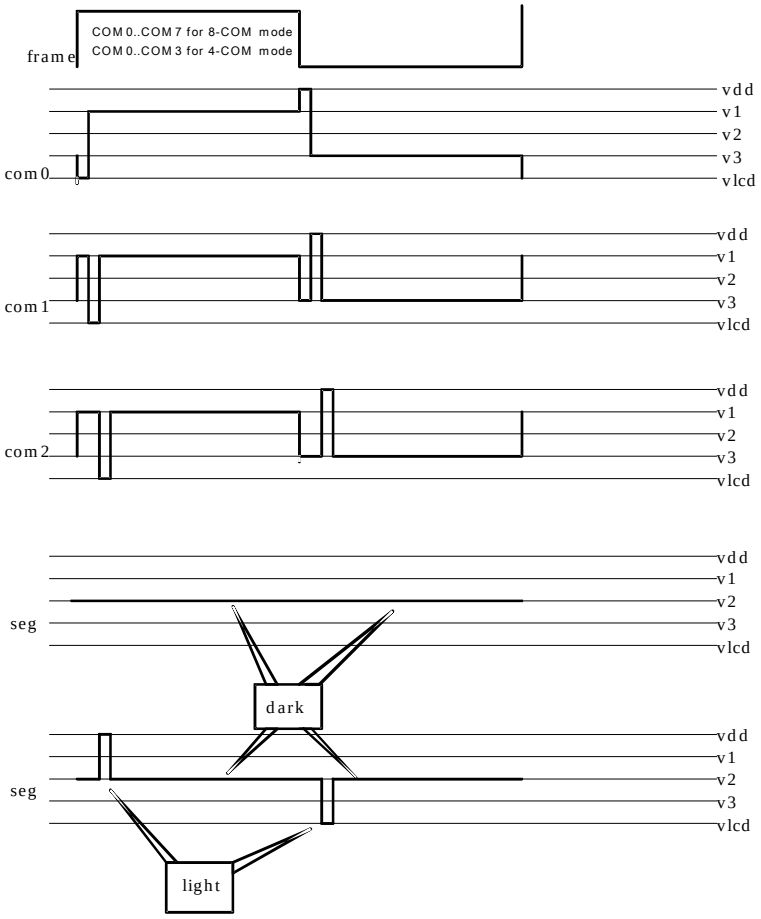


Fig 7-10 LCD Waveform 1/4 bias, 1/8 duty or 1/4 duty

8 Electrical Characteristic

8.1 Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.3 to 6	V
Input Voltage	Vin	-0.5 to VDD +0.5	V
Operating Temperature Range	Ta	0 to 70	°C

8.2 DC Electrical Characteristic

Ta = 0°C ~ 70°C, VDD=3.3V ± 5%, VSS=0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage Current for input pins	IIL1	VIN = VDD, VSS	-	-	±1	μA
Input Leakage Current for bi-directional pins	IIL2	VIN = VDD, VSS	-	-	±1	μA
Input High Voltage	VIH	-	2.5	-	-	V
Input Low Voltage	VIL	-	-	-	0.8	V
Input High Threshold Voltage	VIHT	/RESET, TCC, RDET1	2.0	-	-	V
Input Low Threshold Voltage	VILT	/RESET, TCC, RDET1	-	-	0.8	V
Clock Input High Voltage	VIHX	OSCI	3.5	-		V
Clock Input Low Voltage	VILX	OSCI	-	-	1.5	V
Output High Voltage for Ports 5, 6, 7, 8	VOH1	IOH = -1.6mA	2.4	-	-	V
Output High Voltage for Port 9	VOH2	IOH = -6.0mA	2.4	-	-	V
Output Low Voltage for Ports 5, 6, 7, 8	VOL1	IOH = 1.6mA	-	-	0.4	V
Output Low Voltage for Port 9	VOL2	IOH = 6.0mA	-	-	0.4	V
Com Voltage Drop	V_{com}	Io = ±50 μA	-	-	2.9	V
Segment Voltage Drop	V_{seg}	Io = ±50 μA	-	-	3.8	V
LCD Drive Reference Voltage	V_{LCD}	Contrast Adjustment	-	-	-	-
Pull-high Current	IPH	Pull-high active input pin at VSS	-	-15	-20	μA
Power down current (Sleep mode) POVD disabled	ISB1	All input and I/O pins at VDD, Output pin floating, WDT disabled	-	1	4	μA
Power down current (Sleep mode) POVD enabled			-	5	15	
Low clock current (Green mode) POVD disabled	ISB2	CLK=32.768kHz, Tone block disabled, All input and I/O pins at VDD, Output pin floating, WDT disabled, LCD disabled,	-	35	50	μA
Low clock current (Green mode) POVD enabled			-	45	65	

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low clock current (Green mode) DED enabled POVD disabled	ISB4	CLK=32.768kHz, All input and I/O pins at VDD, Output pin floating, WDT disabled, LCD disabled, Other analog circuits disabled	-	55	75	µA
Low clock current (Green mode) DED enabled POVD enabled			-	65	90	
Operating supply current (Normal mode)	ICC	/RESET=High, CLK=3.5826MHz, Output pin floating, Other analog circuits disabled	-	0.48	1.0	mA

Energy Detector (DED) (Ta=0°C ~ 70°C, VDD=3.3V ± 5%, VSS=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IDED	Operating current for Energy Detector	Fclk=32.768kHz Not including MCU and other parts	-	15	20	µA

Current D/A (Ta=0°C ~ 70°C, VDD=3.3V ± 5%, VSS=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC	Max. output current for current D/A volume control	IOC5 Page 1 Bits 0~3 =1111	3	5	6	mA

8.3 AC Electrical Characteristic

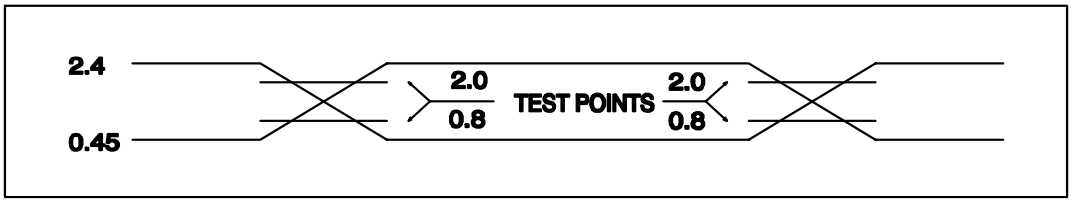
(Ta = 0°C ~ 70°C, VDD = 3.3V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	D_{clk}	-	45	50	55	%
Instruction cycle time	T_{ins}	32.768kHz 3.582MHz	-	60 550	-	µs ns
Device delay hold time	T_{drh}	-	-	18	-	ms
TCC input period	T_{tcc}	*	(Tins+20)/N	-	-	ns
Watchdog timer period	T_{wdt}	Ta = 25°C	-	18	-	ms
Delay from Phase 3 end to INSEND active	T_{diea}	Cl = 100pF	-	-	30	ns
Delay from Phase 4 end to INSEND active	T_{diei}	Cl = 100pF	-	-	30	ns
INSEND Pulse width	T_{iew}	-	30	-	-	ns
Delay from Phase 4 end to CA Bus valid	T_{dca}	Cl = 100pF	-	-	30	ns
ROM data access time	T_{acc}	-	100	-	-	ns
ROM data setup time	T_{cds}	-	20	-	-	ns
ROM data hold time	T_{cdh}	-	20	-	-	ns
Delay time of CA-1	T_{cda} -1	Cl = 100pF	-	-	30	ns

Note: * N = selected prescaler ratio

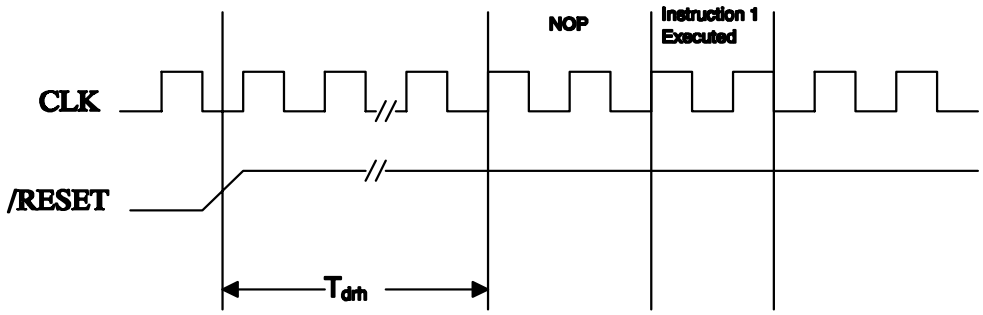
9 Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

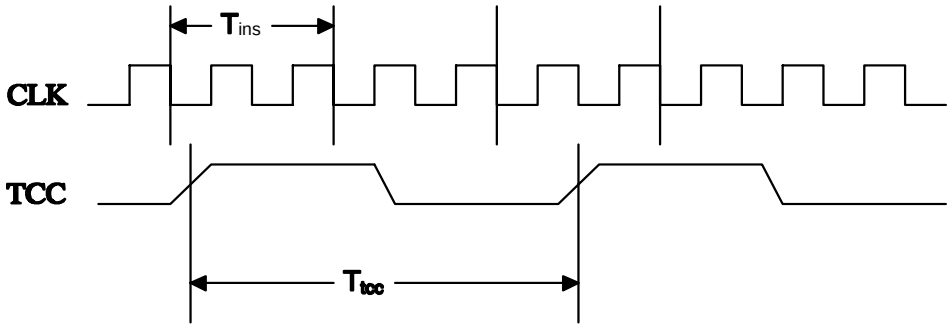


Fig 9-1 AC Timing

10 Application Circuit

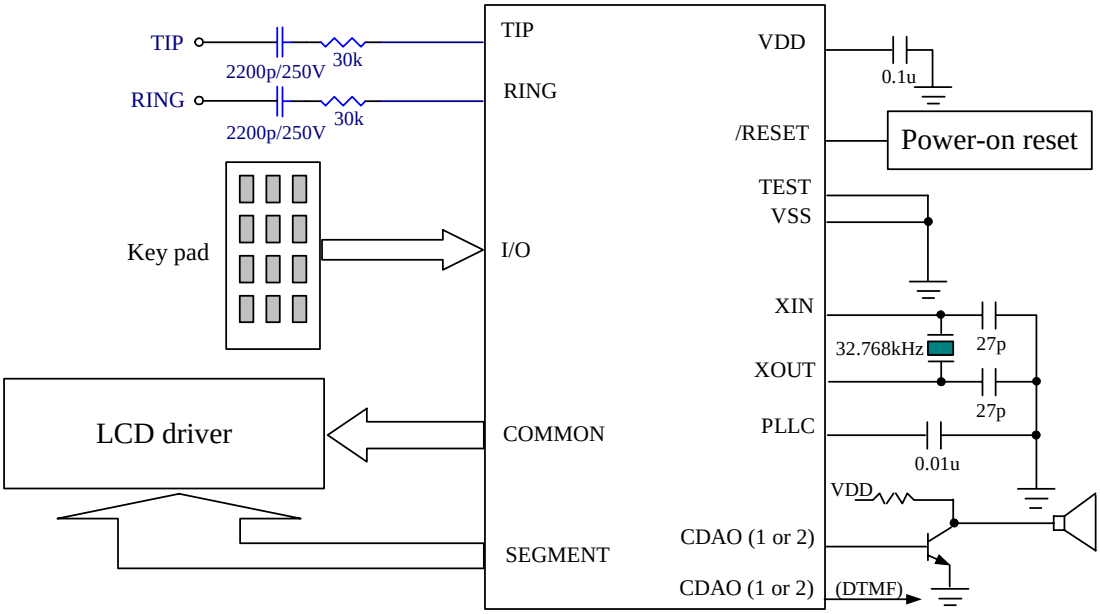


Fig 10-1 Application Circuit

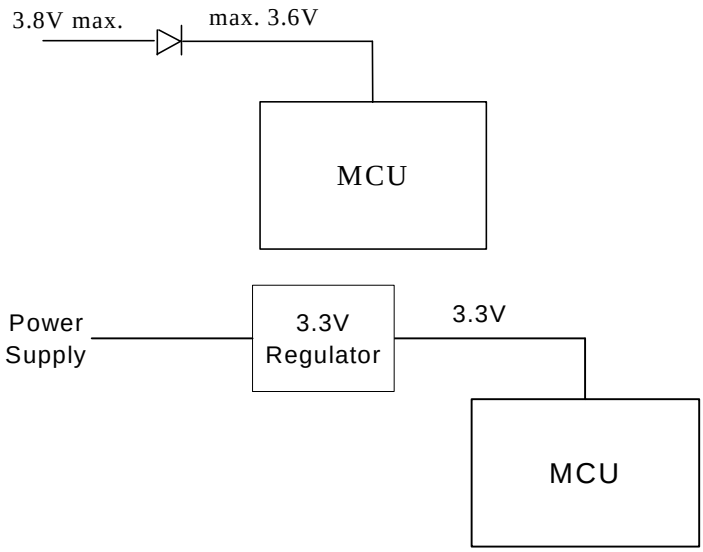


Fig 10-2 Power Flow in Applications

APPENDIX

A User Application Note

Before using this IC, read the following descriptions and take note of the important points.

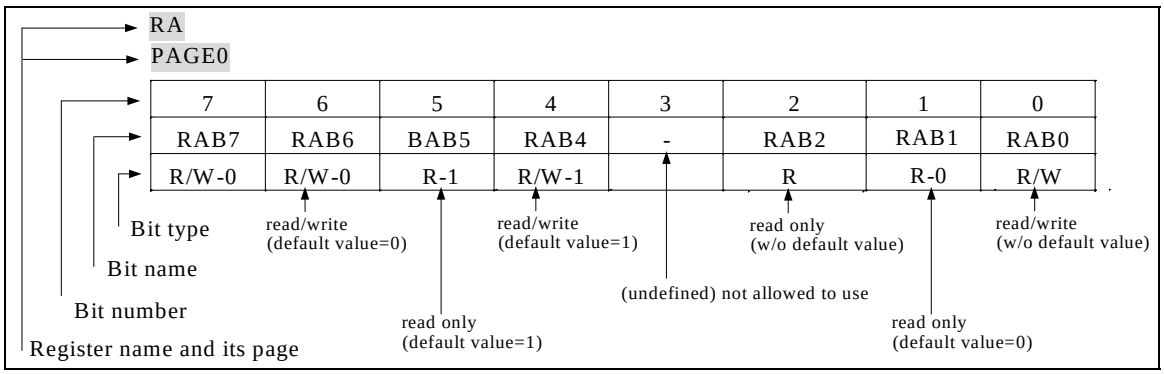
1. There are some undefined or not existing bits in the registers. User needs to be cautious in dealing with those bits while programming and should not use them as data to execute logic or math operations, since those bits have no relative functions and have never been tested. Different symbols are used to distinguish them.

   "**0**" or "**1**" → value always equal to 0 or value always equal to 1, (not existent, read only)

   "-" → value unknown, (not existent) undefined bits are not allowed for use.

   "×" → (general purpose) undefined bits are not allowed for use as RAM or other data read, write or read/write.

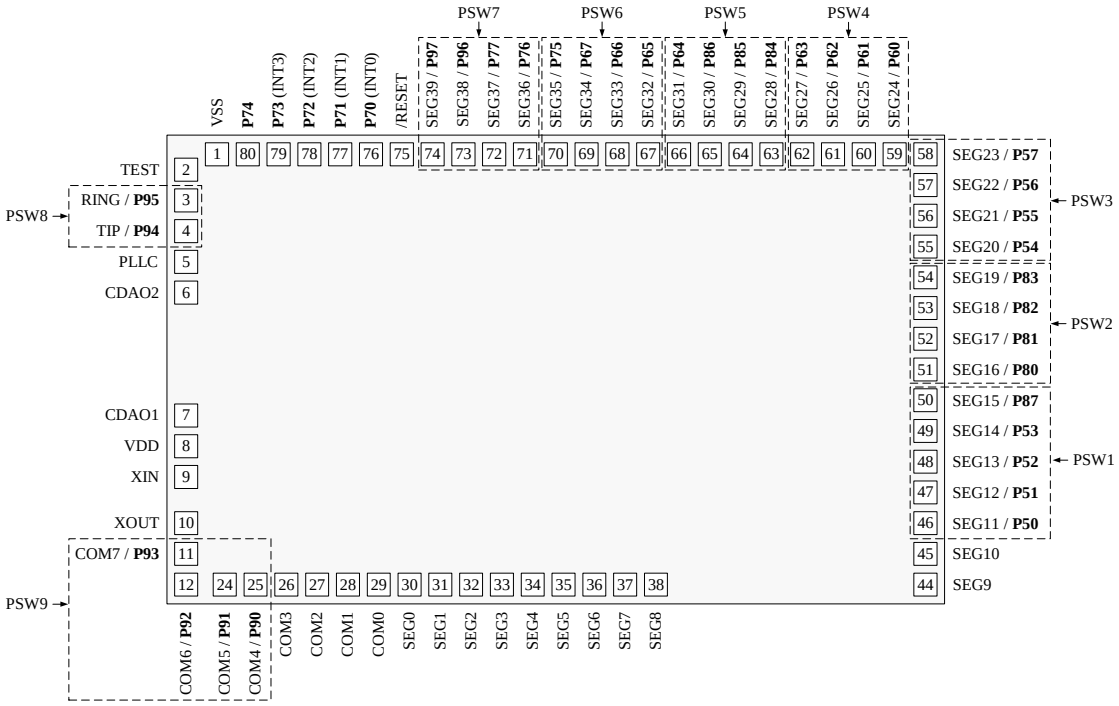
2. The following are the register's descriptions such as bit type, bit name, bit number, etc.



3. Port Switch Control

The register control bits PSW1 ~ PSW9 are used to set shared I/Os. The number for these control bits corresponds to the pin sequence, which can be easily set by user.

*Full functional port switch for **ICE807** in all applications*



Port switch definition for ICE807:

Name	Bit Location	Value	Pin Function
PSW1	R7 Page 1 Bit 4	0	I/Os : P50 ~ P53, P87
		1 (default)	LCD segments : SEG11 ~ SEG15
PSW2	IOCA Page 0 Bit 5	0 (default)	I/Os : P80 ~ P83
		1	LCD segments : SEG16 ~ SEG19
PSW3	IOCA Page 0 Bit 4	0 (default)	I/Os : P54 ~ P57
		1	LCD segments : SEG20 ~ SEG23
PSW4	R7 Page 1 Bit 5	0 (default)	I/Os : P60 ~ P63
		1	LCD segments : SEG24 ~ SEG27
PSW5	RE Bit 3	0 (default)	I/Os : P84 ~ P86, P64
		1	LCD segments : SEG28 ~ SEG31
PSW6	IOCA Page 0 Bit 6	0 (default)	I/Os : P65 ~ P67, P75
		1	LCD segments : SEG36 ~ SEG35
PSW7	IOCA Page 0 Bit 7	0 (default)	I/Os : P76 ~ P77, P96 ~ P97
		1	LCD segments : SEG37 ~ SEG39
PSW8	R7 Page 1 Bit 6	0	I/Os : P94 ~ P95
		1 (default)	DED inputs : TIP, RING
PSW9	R7 Page 1 Bit 7	0	I/Os : P90 ~ P93
		1 (default)	LCD commons : COM4 ~ COM7