EM78806B

8-BIT MICRO-CONTROLLER

Version 5.0

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Version History

Specification Revision History	
Version	Content
EM78806B	
4.2	Update pin description on P60~P67
4.3	Update feature description
4.4	Add “ASPCM maximum sampling rate up to 16k” to feature
4.5	Change “VII. Instruction Set” for PAGE instruction’s Instruction Binary from “…0kkk” to “…kkkk”.
4.6	1.Change pin configuration for pin 1 ~ 3 2.Remove asynchronous programming tone generator for FSK tone generation
4.7	Change pin configuration for pin 1,2,4,5,6
4.8	1.Add green tone function for programming tone generator. Add RB bit6(GTONE) for green tone function 2.Add clear Current DA function. Add IOC5 PAGE1 bit7(CLDA) for clear Current DA function.
4.9	Add 64-pin QFP, 80-pin QFP package and revise pin configuration
5.0	Remove Idle mode

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. Always keep RA bit7 = 0. Don't set it to "1" to prevent causing problem.

I. General Description

The EM78806B is an 8-bit CID (Call Identification) RISC type microprocessor with low power , high speed CMOS technology . Integrated onto a single chip are on_chip watchdog (WDT) , RAM , ROM , programmable real time clock /counter , internal interrupt , power down mode , LCD driver , Energy Detector (DED) , Tone generator , ASPCM voice synthesizer, voice ROM, Current D/A and tri-state I/O. It provides a single chip solution to design a CID of calling message display .

II. Feature

CPU

- Operating voltage range : 2.2V 3.6V
- 16k x 13 on chip program ROM
- 1.1K×8 on chip RAM
- Up to 26 bi-directional tri-state I/O ports (18 independent I/O)
- 8 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC) with 8-bit pre-scaler
- Two sets of 8-bit counters can be interrupt sources
- Selective signal sources and overflow interrupt
- Programmable free running on chip watchdog timer
- 99.9% single instruction cycle commands
- Three modes (Main clock is generated by internal PLL 3.5826MHz x 0.125, 0.25, 2 or 1.)

Mode	CPU	Main clock	32.768kHz clock
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- Input port wake up function
- CPU reset : power on reset or /POVD reset (by code option), external /RESET pin
- 8 interrupt sources (4 external, 4 internal)
- IO Port interrupt, pull high, wake-up and open drain functions
- External sub-clock frequency is 32.768KHz
- Key scan function

PROGRAMMING TONE GENERATORS

- Operation Volltage 2.2V 3.6V
- Programming Tone1 and Tone2 dual tone generators (DTMF)
- 8-bit programming Tone1 generators
- 8-bit programming Tone2 generator

CID

- Energy Detector (DED) for line energy detection

CID number telling

- 40kx5 on-chip voice ROM
- ASPCM maximum sampling rate up to 16k
- About 6 sec ASPCM voice synthesizer for 6.5536k sampling rate
- 8-bit D/A resolution for voice output

LCD

- LCD operation voltage chosen by software
- Common driver pins : 8
- Segment driver pins : 24
- 1/4 bias
- 1/8 duty

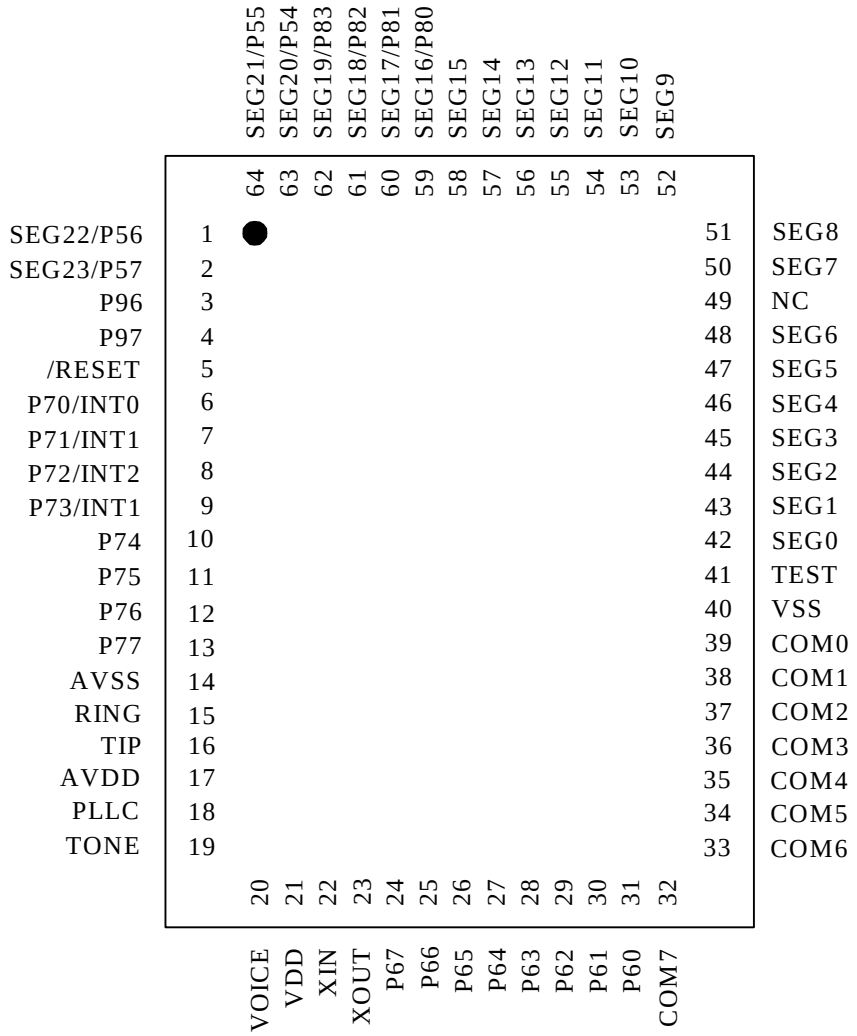
PACKAGE

- 63-pin die (EM78806BH), 64-pin QFP (EM78806BAQ), 80-pin QFP (EM78806BBQ)

III.Application

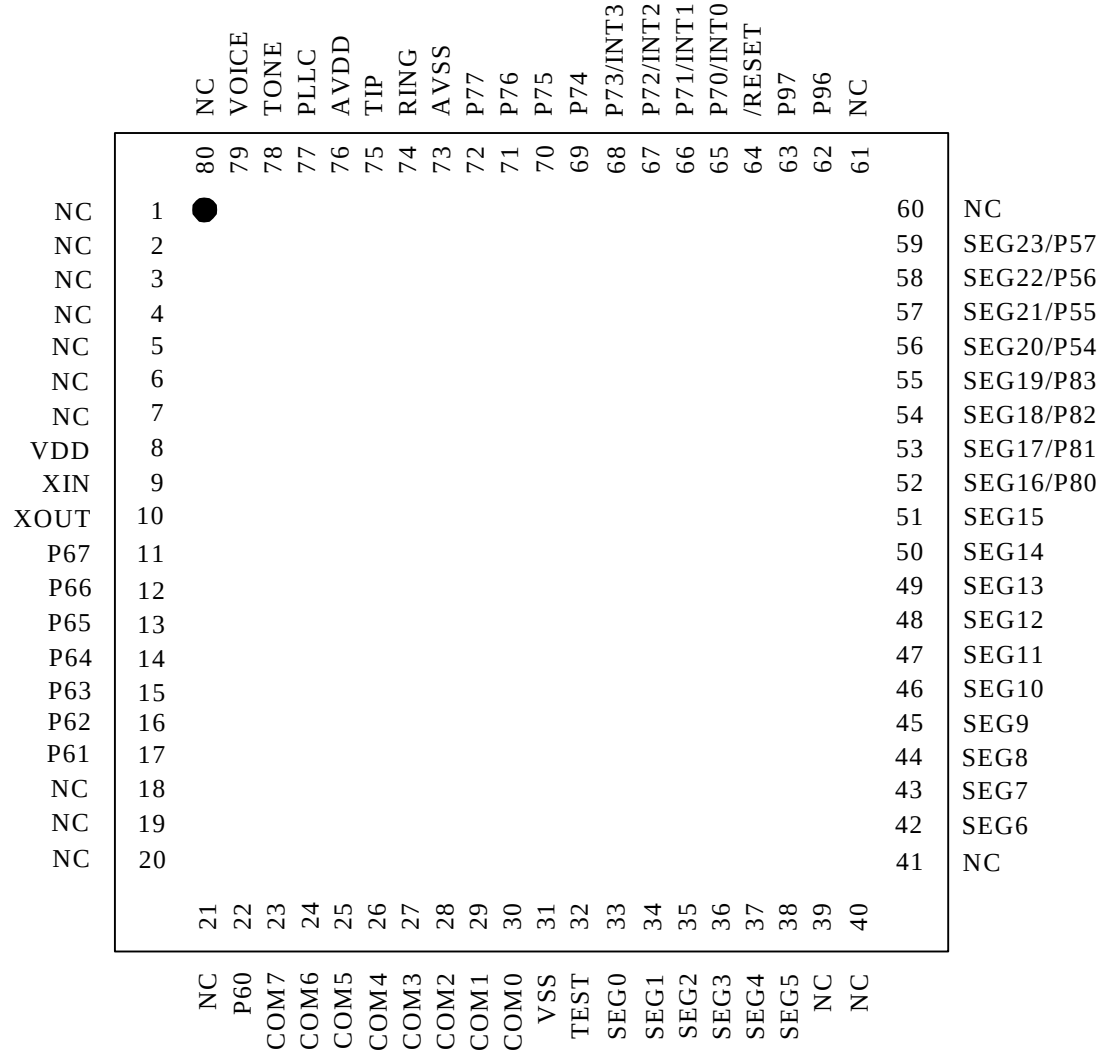
Caller ID adjunct box or phone units for FSK/DTMF CID dual system development.

IV. Pin Configuration



63-die or 64-pin QFP

Fig.1a Pin assignment



80-pin QFP

Fig.1b Pin assignment

V. Functional Block Diagram

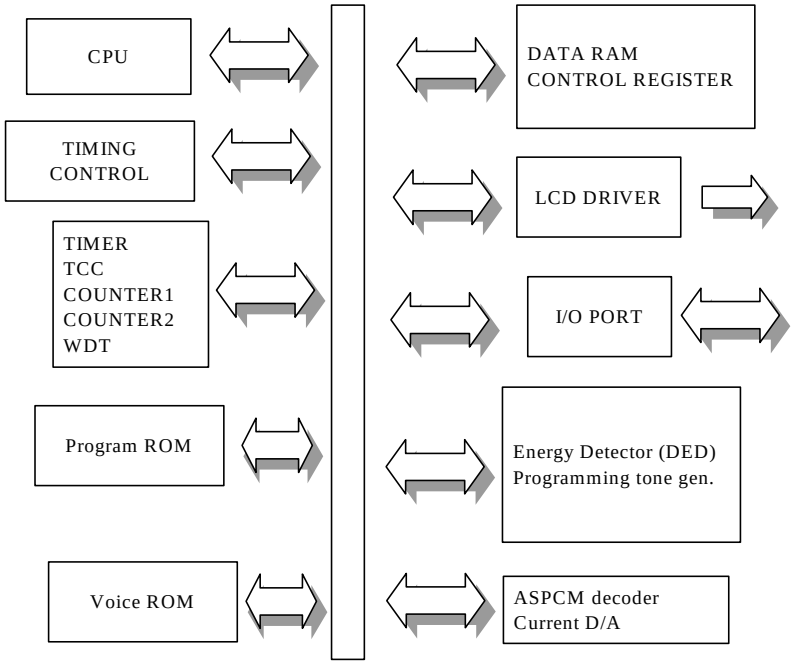


Fig.2 Block diagram1

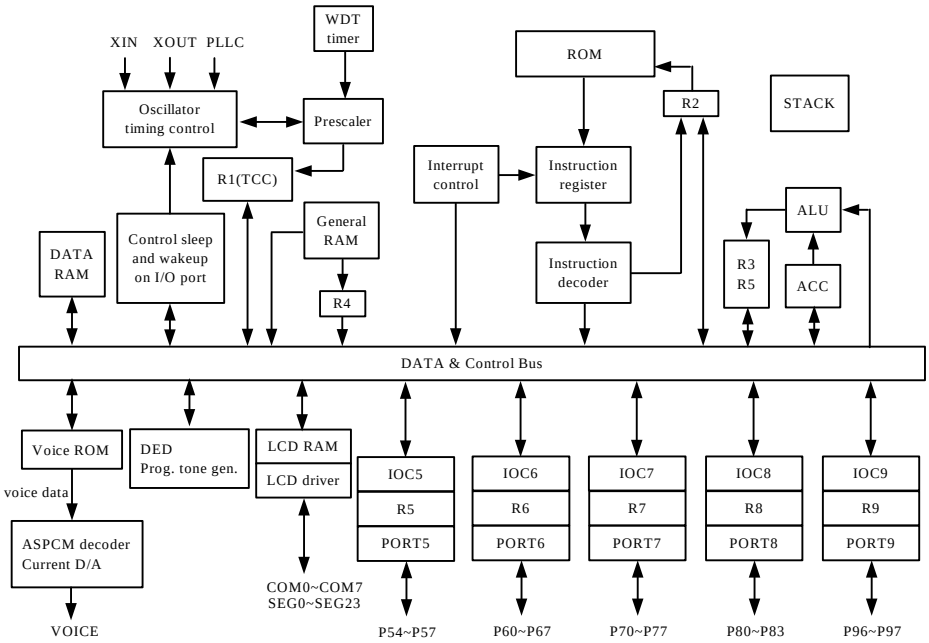


Fig.3 Block diagram2

VI. Pin Descriptions

PIN	I/O	DESCRIPTION
VDD AVDD	POWER	digital power analog power
VSS AVSS	GROUND	digital ground analog ground
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
COM0..COM7	O	Common driver pins of LCD drivers
SEG0...SEG15 SEG16...SEG19 SEG20..SEG23	 O (PORT8) O (PORT5)	Segment driver pins of LCD drivers Shared with P80 ~ P83 Shared with P54 ~ P57
PLLC	I	Phase loop lock capacitor, 0.01u to 0.047u with AVSS
INT0..INT3	PORT7(0..3)	PORT7(0)~PORT7(3) signal can be interrupt signals.
P54 ~P57	PORT5	PORT5 can be INPUT or OUTPUT port each bit. And P54 ~ P57 are shared with segment signal.
P60 ~P67	PORT6	PORT6 can be INPUT or OUTPUT port each bit.
P70 ~P77	PORT7	PORT7 can be INPUT or OUTPUT port each bit. Internal Pull high function. P76,P77 have open drain function
P80 ~ P83	PORT8	PORT 8 can be INPUT or OUTPUT port each bit. And P80 ~ P83 are shared with segment signal.
P96 ~ P97	PORT9	PORT 9 can be INPUT or OUTPUT port each bit. P96,P97 have wake-up function.
TEST	I	Test pin into test mode , normal low
VOICE	O	D/A output for ASPCM voice synthesizer
TONE	O	Tone generator's output
/RESET	I	Reset. Low reset.
TIP	I	Differential Energy Detector input pin. It is a non-polarity pin
RING	I	Differential Energy Detector input pin. It is a non-polarity pin

VII. Functional Descriptions

VII.1 Operational Registers

Register configuration

	R PAGE registers	IOC PAGE registers	
Addr	R PAGE0	IOC PAGE0	IOC PAGE1
00	Indirect addressing		
01	TCC		
02	PC		
03	Page, , Tone1,2 power control, Status		
04	RAM bank, RSR		
05	PORT5 I/O data, Program ROM page	PORT5 I/O control	ASPCM rate control, Volume control,
06	PORT6 I/O data	PORT6 I/O control	
07	PORT7 I/O data	PORT7 I/O control	VROM address(8~15)
08	PORT8 I/O date	PORT8 I/O control	VROM address(0~7)
09	PORT9 I/O data	PORT9 I/O control	VROM data
0A	CPU power saving, PLL, Main clock	(P8 low nibble,P5) switch,LCD bias, Key scan control	D/A power control, D/A clear, DED control
0B	Green tone, ASPCM control, DED output, CID RAM bank	LCD RAM address	Counter 1 data
0C	CID RAM address	LCD RAM data	Counter 2 data
0D	CID RAM data	TONE1 control	Port7 pull high
0E	Wake-up control, LCD control	TONE1 control	(P76,P77) open drain, CNT1,2 clk source, CNT1,2 prescaler
0F	Interrupt flag	Interrupt mask	
10	16 bytes Common registers		
:			
1F			
20	Bank0~Bank3 Common registers (32x8 for each bank)		
:			
3F			

VII.2 Operational Register Detail Description

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

R1 (TCC)

Increased by an external signal edge applied to TCC, or by the instruction cycle clock.
Written and read by the program as any other register.

R2 (Program Counter)

The structure is depicted in Fig.4
Generates 16K × 13 External ROM addresses to the relative programming instruction codes.
"JMP" instruction allows the direct loading of the low 10 program counter bits.
"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".
"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
"TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

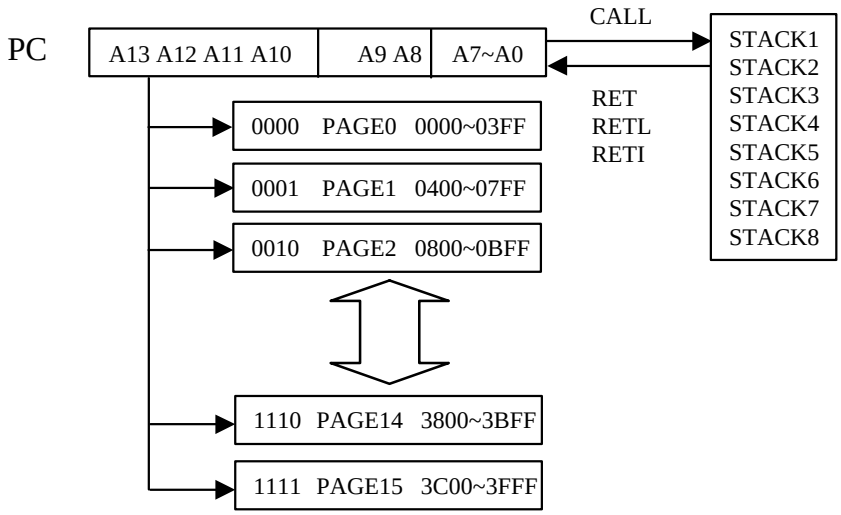


Fig.4 Program counter organization

R3 (Page, Tone1,2 power control, Status register)

7	6	5	4	3	2	1	0
PAGE	P_TONE2	P_TONE1	T	P	Z	DC	C

Bit 0 (C) : Carry flag
Bit 1 (DC) : Auxiliary carry flag
Bit 2 (Z) : Zero flag
Bit 3 (P) : Power down bit.
Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
Bit 4 (T) : Time-out bit
Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode	0	1	
/RESET wake up from sleep	1	0	
power up	1	1	
Low pulse on /RESET	x	x	X : don't care

Bit 5 (P_TONE1) : Power control bit of Tone generator 1
User can use this bit to power on the tone generator 1
Bit 6 (P_TONE2) : Power control bit of Tone generator 2
User can use this bit to power on the tone generator 2
Ps. Tone frequency is controlled by IOCD and IOCE.

R3(6,5)	Tone generator 2	Tone generator 1
00	Power off	Power off
01	Power off	Power on
10	Power on	Power off
11	Power on	Power on

Bit 7 (PAGE) : change IOCB ~ IOCE to another page
0/1 ➔ PAGE0/PAGE1

R4 (RAM bank, RAM selection for common registers R20 ~ R3F)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F
RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F
These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F)..
Please refer to Fig.4 control register configuration for details.

R5 (PORT5 I/O data, Program page selection)

7	6	5	4	3	2	1	0
P57	P56	P55	P54	PS3	PS2	PS1	PS0

Bit 0 ~ 3 (PS0 ~ PS3) : Page selection bits
They should be set before JMP or CALL instruction.
Page select bits

PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
:	:	:	:	:
:	:	:	:	:
1	1	1	0	Page 14
1	1	1	1	Page 15

User can use PAGE instruction to change page and maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. The program page is maintained by EMC's complier. It will change user's program by inserting instructions within program.

Bit 4 : unused

Bit 5 ~ 7 (P54 ~ P57) : 4-bit PORT5(4 ~ 7) I/O data register

R6 (PORT6 I/O data)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

Bit 0 ~ Bit 7 (P60 ~ P67) : 8-bit PORT6(0~7) I/O data register
User can use IOC register to define input or output each bit.

R7 (PORT7 I/O data)

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70

Bit 0 ~ Bit 7 (P70 ~ P77) : 8-bit PORT7(0~7) I/O data register
User can use IOC register to define input or output each bit.

R8 (PORT8 I/O data)

7	6	5	4	3	2	1	0
x	x	x	x	P83	P82	P81	P80

Bit 0 ~ Bit 3 (P80 ~ P83) : 4-bit PORT8(0~3) I/O data register
User can use IOC register to define input or output each bit.
Bit 4 ~ Bit 7 : unused

R9 (PORT9 I/O data)

7	6	5	4	3	2	1	0
P97	P96	x	x	x	x	x	x

Bit 0 ~ Bit 5 : unused
Bit 6 ~ Bit 7 (P96 ~ P97) : 2-bit PORT9(6~7) I/O data register
User can use IOC register to define input or output each bit.

RA (CPU power saving, PLL, Main clock selection)

7	6	5	4	3	2	1	0
x	ENPLL	CLK2	CLK1	x	x	x	x

Bit 0 ~ Bit 3 : unused
Bit 4 ~ 5 (CLK1 ~ CLK2) : Main clock selection bits.
User can choose the main clock by setting CLK1 and CLK2. All the clock selections are list below.

(CLK2,CLK1)	MAIN clock	/358E	CPU's clock
(0,0)	447.8293kHz	1	447.8293kHz
(0,1)	895.6587kHz	1	895.6587kHz
(1,0)	7.1653MHz	1	7.1653MHz
(1,1)	3.5826MHz	1	3.5826MHz
(0,0)	X	0	32768HZ
(0,1)	X	0	32768HZ
(1,0)	X	0	32768HZ
(1,1)	X	0	32768HZ

Bit 6 (ENPLL) : (read/write) PLL enable/disable control
1/0 ➔ enable/disable
The relation between 32.768kHz and main clock can see Fig.5

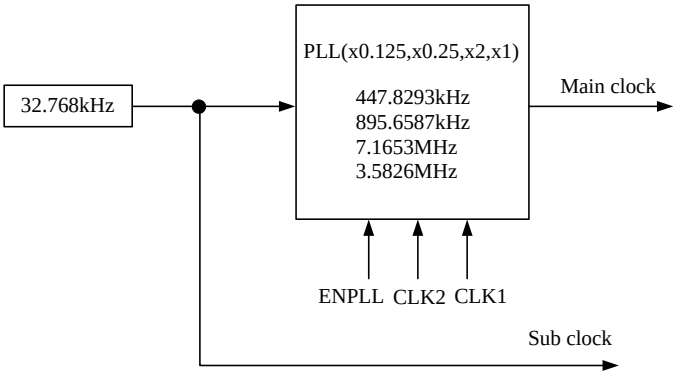


Fig.5 The relation between 32.768kHz and Main clock

Bit 7 : unused

Always keep this bit to "0". Don't set it to "1" to prevent causing problem..

It can be waked up by Watch Dog timer (WDT), PORT96~97, PORT70~73 and run from "SLEP" next instruction.

Wakeup signal	SLEEP mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out EDD	X	Interrupt	Interrupt
WDT time out	RESET	RESET	RESET
Port96,97	RESET	X	X
PORT70~73	RESET	Interrupt	Interrupt

P70 ~ P73 's wakeup function is controlled by IOCF(1,2,3) and ENI instruction.
P70 's wakeup signal is a rising edge or falling edge defined by CONT REGISTER bit7.
Port96, Port97, Port71, Port72 and Port73 's wake-up pattern is a falling edge triggering signal.
Energy Detector (DED or SED) wakeup and interrupt signal can be controlled by RB bit 7 (EDGE).

RB (Green tone, ASPCM control, DED output, CID RAM banks)

7	6	5	4	3	2	1	0
EDGE	GTONE	PLAY	S/P	DEDD	x	CALL_2	CALL_1

Bit 0 ~ 1 (CALL_1 ~ CALL_1) : 8 blocks of CALLER ID RAM area
From (0,0) to (1,1), user can use 1.0K CID RAM with RC RAM address.

Bit 2 : unused

Bit 3 (DEDD) : Output data of Energy Detector (DED)
If input signal from TIP pin and RING pin to Energy Detector is over the threshold level setting at IOCA PAGE1 bit 0(DEDTHD), the DED will extract the zero-crossing pulse waveform corresponding to input signal.

Bit 4 (S/P) : setting for voice stop-playing or voice pause-playing
0/1 ➔ voice stop-playing/voice pause-playing

Bit 5 (PLAY) : voice-playing control
0/1 ➔ disable voice-playing/enable voice-playing

PLAY	S/P	function	Description
1 ➔ 0	0	Stop-playing	The playing address is reset to the beginning of the play. D/A data is reset.
	1	Pause-playing	The playing address is not reset.
0 ➔ 1	0	Playing from stop	The playing address is reset to the beginning of the play. D/A data is reset. Then it begins to play.
	1	Playing from pause	The playing address is not reset and it plays again.

Ps. While playing voice by setting (PLAY,S/P)=(1,0) or (1,1) comes to an end of the play (meet the stop code), the (PLAY,S/P) bits are automatically clear to (0,0).

Bit 6(GTONE) : Green tone for programming tone generator

0/1 ➔ disable/enable green tone function

When this function is enabled, either R3 bit5(P_TONE1) or R3 bit6(P_TONE2) is set then PLL is auto-on. At this time, TONE1 or TONE2 can be used no matter what MCU works on 32.768kHz or normal mode. When this function is disabled, TONE1 or TONE2 can only work on normal mode.

Bit 7 (EDGE) : Wake-up and interrupt trigging edge control of Energy Detector (DED) output

0/1 ➔ Falling edge trig. / Rising edge&Falling edge trig.

RC (CID RAM address)

7	6	5	4	3	2	1	0
CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0

Bit 0 ~ Bit 7 (CIDA0 ~ CIDA7) : Caller ID (CID) RAM address

User can select Caller ID RAM address from 0 to 255.

RD (CID RAM data buffer)

7	6	5	4	3	2	1	0
CIDD7	CIDD6	CIDD5	CIDD4	CIDD3	CIDD2	CIDD1	CIDD0

Bit 0 ~ Bit 7 (CIDD0 ~ CIDD7) : Caller ID RAM data register.

User can see IOCA register how to select CID RAM banks.

RE (Wake-up control, LCD control)

7	6	5	4	3	2	1	0
x	/WDTE	/WUP97	/WUP96	x	LCD_C2	LCD_C1	/WUEDD

Bit 0 (/WUEDD) : Wake-up control of Energy Detector (DED) output data

1/0 ➔ enable/disable

Bit 1 ~ Bit 2 (LCD_C1 ~ LCD_C2) : LCD display enable or blanking.

The display duty change must set the (LCD_C2,LCD_C1) to (0,0).

(LCD_C2,LCD_C1)	LCD Display Control	duty	bias
(0,0)	Disable(turn off LCD)	1/8 1/8	1/4 1/4
(0,1)	Blanking	:	
(1,1)	LCD display enable	:	

Bit 3 : unused

Bit 4 (/WUP96) : PORT9 bit6 wake-up control, 1/0 ➔ enable/disable

Bit 5 (/WUP97) : PORT9 bit7 wake-up control, 1/0 ➔ enable/disable

Bit 6 (/WDTE) : Watchdog timer enable control, 1/0 ➔ enable/disable

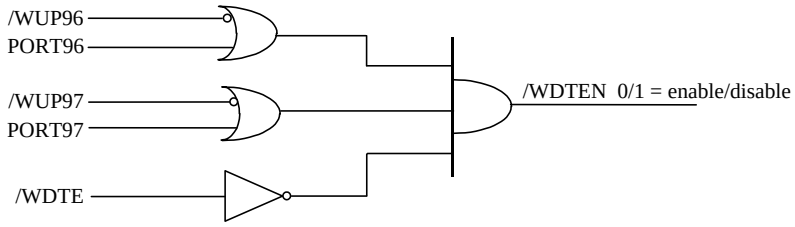


Fig.6 Wake up function and control signal

Bit 7 : unused

RF (Interrupt status register)

7	6	5	4	3	2	1	0
EDD	x	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF

Bit 0 (TCIF) : TCC timer overflow interrupt flag
It will be set when TCC timer is overflow.
Bit 1 (INT0) : External INT0 pin interrupt flag
It can be used when PORT70 is set to input port.
Bit 2 (INT1) : External INT1 pin interrupt flag
It can be used when PORT71 is set to input port.
Bit 3 (INT2/INT3) : external INT2 and INT3 pin interrupt flag
It can be used when PORT72 or PORT73 is set to input port.
Bit 4 (CNT1) : 8 bit Counter1 overflow interrupt flag.
It will be set when Counter1 is overflow.
Bit 5 (CNT2) : 8 bit Counter2 overflow interrupt flag.
It will be set when Counter2 is overflow.
Bit 6 : unused
Bit 7 (EDD) : Interrupt flag of Energy Detector (DED) output data

"1" means interrupt request and "0" means non-interrupt. INT0~INT3 interrupts are edge triggering (falling edge or rising edge) which can be set by CONT bit 7 (INT_EDGE). Interrupt edge control of DED output data is set by RB bit 7(EDGE). Also see corresponding interrupt mask in IOCF register. User can read and clear.

R10~R3F (General Purpose Register)

R10~R3F (Banks 0~3) are all general purpose registers.

VII.3 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
INT_EDGE	INT	TS	x	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 ➔ TCC/WDT

Bit 4 : unused

Bit 5(TS) : TCC signal source

0 ➔ Instruction clock

1 ➔ 16.384kHz

Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See Fig.16.

Bit 6 (INT) : INT enable flag

0 ➔ interrupt masked by DISI or hardware interrupt

1 ➔ interrupt enabled by ENI/RETI instructions

Bit 7(INT_EDGE) : interrupt edge type of P70

0 ➔ P70 's interruption source is a rising edge signal and falling edge signal.

1 ➔ P70 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

IOC5 (PORT5 I/O control, D/A clear, Voice synthesizer sampling rate and volume control)

PAGE0 (PORT5 I/O control)

7	6	5	4	3	2	1	0
IOC57	IOC56	IOC55	IOC54	x	x	x	x

Bit 0 ~ Bit 3 : unused

Bit 4 ~ 7 (IOC54 ~ IOC57) : PORT5(4~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (D/A clear, Voice synthesizer sampling rate and volume control)

7	6	5	4	3	2	1	0
CLDA	RATE1	RATE0`	RATE0	VOL3	VOL2	VOL1	VOL0

Bit 0 ~ Bit 3 (VOL0 ~ VOL3) : voice synthesizer volume control

VOL3 ~ VOL0	Max voice output current (mA)
0000	0
0001	5 x 2/16 mA = 0.625 mA
0010	5 x 3/16 mA = 0.9375 mA
0011	5 x 4/16 mA = 1.25 mA
0100	5 x 5/16 mA = 1.5625 mA
0101	5 x 6/16 mA = 1.875 mA
0110	5 x 7/16 mA = 2.1875 mA
0111	5 x 8/16 mA = 2.5 mA
1000	5 x 9/16 mA = 2.8125 mA
1001	5 x 10/16 mA = 3.125 mA
1010	5 x 11/16 mA = 3.4375 mA
1011	5 x 12/16 mA = 3.75 mA
1100	5 x 13/16 mA = 4.0625 mA
1101	5 x 14/16 mA = 4.375 mA
1110	5 x 15/16 mA = 4.6875 mA
1111	5 mA

Bit 4 ~ Bit 6 (RATE0 ~ RATE2) : voice synthesizer sampling rate control

RATE2 ~RATE0	Sampling rate
000	x
001	x
010	32.768kHz/2 = 16.384kHz
011	32.768kHz/3 = 10.9227kHz
100	32.768kHz/4 = 8.192kHz
101	32.768kHz/5 = 6.5536kHz
110	32.768kHz/6 = 5.4313kHz
111	32.768kHz/7 = 4.6811kHz

Bit 7 (CLDA) : Current D/A data clear enable control

0/1 ➔ disable/enable

When this bit is set(enabled), the internal Current D/A data will be clear and its output will go to ground level with VOICE pin connecting a resistor to ground. After setting this bit, remember to clear(disable) it again otherwise it will keep output to ground level no matter what voice ROM is playing or not

IOC6 (PORT6 I/O control)

PAGE0 (PORT6 I/O control)

7	6	5	4	3	2	1	0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60

Bit 0 ~ Bit 7 (IOC60 ~ IOC67) : PORT6(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1

Bit 0 ~ Bit 7 : unused

IOC7 (PORT7 I/O control, Voice ROM address(8 ~ 15))

PAGE0 (PORT7 I/O control register)

7	6	5	4	3	2	1	0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 0 ~ Bit 7 (IOC70 ~ IOC77) : PORT7(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (Voice ROM address(8~15))

7	6	5	4	3	2	1	0
VRA15	VRA14	VRA13	VRA12	VRA11	VRA10	VRA9	VRA8

Bit 0 ~ Bit 7 (VRA8 ~ VRA15) : voice ROM address register bit(8 ~ 15)

IOC8 (PORT8 I/O control, Voice ROM address(0 ~7))

PAGE0 (PORT8 I/O control register)

7	6	5	4	3	2	1	0
x	x	x	x	IOC83	IOC82	IOC81	IOC80

Bit 0 ~ Bit 3 (IOC80 ~ IOC83) : PORT8(0~3) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

Bit 4 ~ Bit 7 : unused

PAGE1 (Voice ROM address(0~7))

7	6	5	4	3	2	1	0
VRA7	VRA6	VRA5	VRA4	VRA3	VRA2	VRA1	VRA0

Bit 0 ~ Bit 7 (VRA0 ~ VRA7) : voice ROM address register bit(0 ~ 7)

IOC9 (PORT9 I/O control, Voice ROM data)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOC97	IOC96	x	x	x	x	x	x

Bit 0 ~ Bit 5 : unused

Bit 6 ~ Bit 7 (IOC96 ~ IOC97) : PORT9(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (Voice ROM data register)

7	6	5	4	3	2	1	0
x	x	x	VRD4	VRD3	VRD2	VRD1	VRD0

Bit 0 ~ Bit 4 (VRD0 ~ VRD4) : 8-bit voice ROM data register

Bit 5 ~ Bit 7 : unused

IOCA (PORT switch, LCD bias, key scan, D/A power control, DED control)

PAGE0 (PORT8,5 switch, LCD bias, key scan)

7	6	5	4	3	2	1	0
x	x	P8SL	P5S	BIAS3	BIAS2	BIAS1	SC

Bit 0 (SC) : key scan function control

0/1 ➔ disable/enable

Once you enable this bit, all of the LCD signal will have a low pulse during a common period. This pulse has 30us width. Please use the following procedure to implement the key scan function :

1. Set PORT7 as input port
2. Set IOCD PAGE1 to enable PORT7 pull high function
3. Enable key scan function
4. Once push a key . Set RA bit 6 to enable PLL(CPU will run in the normal mode)
5. LCD and disable key scan function

6. Set P5S =0 or/and P8SL=0. PORT5 or/and PORT8 sent probe signal to PORT7 and read PORT7. Get the key.
7. Note!! A probe signal should be delay a instruction at least to another probe signal.
8. Set P5S =1 or/and P8SL=1. PORT5 or/and PORT8 as LCD signal

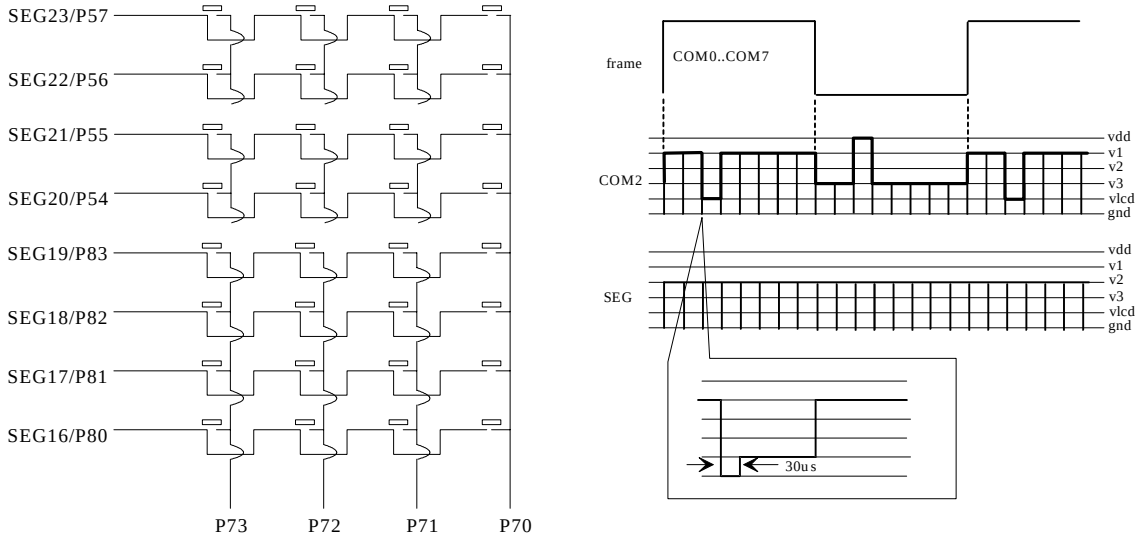


Fig.7. Key scan circuit

Bit 1 ~ 3 (BIAS1 ~ BIAS3) : LCD bias control used to choose LCD operation voltage.

(BIAS3,BIAS2,BIAS1)	Vop (VDD 3.3V)	VDD=3.3V
(0,0,0)	0.60VDD	1.98V
(0,0,1)	0.66VDD	2.18V
(0,1,0)	0.74VDD	2.44V
(0,1,1)	0.82VDD	2.71V
(1,0,0)	0.87VDD	2.87V
(1,0,1)	0.93VDD	3.07V
(1,1,0)	0.96VDD	3.17V
(1,1,1)	1.00VDD	3.30V

Bit 4 (P5S) : PORT5 nibble switch

0/1 ➔ normal I/O port/SEGMENT output

Bit 5 (P8SL) : port8 low nibble switch

0/1 ➔ normal I/O port P80~P83/SEGMENT output SEG16~SEG19

Bit 6 ~ Bit 7 : unused

PAGE1 (D/A power control, DED control)

7	6	5	4	3	2	1	0
/DASTOP	x	x	x	(RES)	EGCLK	DEDPWR	DEDTHD

Bit 0 (DEDTHD) : The minimum detection threshold of Dual Input Energy Detector (DED)

0/1 ➔ -45dBm/-30dBm

Bit 1 (DEDPWR) : Power control of Energy Detector (DED)

0/1 ➔ Power off/Power on

Bit 2 (EGCLK) : Operating clock for Energy Detector (DED)

0/1 ➔ 32.768kHz/3.5826MHz

This bit is used to select operating clock for Energy Detector (DED). When this bit is set to “1”, the PLL is also enabled regardless of RA bit 6 (ENPLL) value. At this time, the Energy detector works at high

frequency mode. When this bit is set to "0", the Energy Detector works at low frequency mode. The difference between high frequency mode and low frequency is as follows.

EGCLK	ENPLL	Energy Detector status	PLL status
0	0	32.768kHz operating clock	PLL is disabled
	1	Normal detection Small current consumption	PLL is enabled
1	x	3.5826MHz operating clock Accurate detection More current consumption	PLL is enabled

Ps. "x" means don't care

Bit 3 (RES) : reserved bit for factory test only. It has to be clear to zero or remain default value.
Bit 4 ~ Bit 6 : unused
Bit 7 (DASTOP) : D/A stop conversion and power down
0 ➔ Disable and power down D/A
1 ➔ Enable and power on D/A

IOCB (LCD RAM address, Counter 1 data)

PAGE0 (LCD RAM address)

Bit 0 ~ Bit 4 (LCDA0 ~ LCDA4) : LCD RAM address

The LCD display data is stored in the data RAM. The relation of data area and COM/SEG pin is as below :

COM7 ~ COM0	
00H (Bit7 ~ Bit0)	SEG0
01H	SEG1
:	:
:	:
17H	SEG23
18H	(empty)
	:
1FH	(empty)

Bit 6 ~ Bit 7 = 0 : unused

PAGE1 (Counter 1 preset)

8 bit up-counter (COUNTER1) preset and read out register. (write = preset) . After an interrupt, it will count from "00".

IOCC (LCD RAM data, Counter 2 data)

PAGE0 (LCD RAM data buffer)

Bit 0 ~ Bit 7 : LCD RAM data

PAGE1 (Counter 2 preset)

8 bit up-counter (COUNTER2) preset and read out register. (write = preset) After a interrupt, it will count from "00".

IOCD (TONE1 control, PORT7 pull high)

PAGE0 (TONE1 frequency control)

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10

Bit 0 ~ Bit 7 (T10 ~ T17) : TONE1 frequency control bits

Clock source = 111957Hz and Freq. = 111957Hz / N, where N = 0 ~ 255 is divider value for T17 ~ T10 Tone generator 1 ‘s frequency divider. Please run in normal mode.
T17~T10 = ‘11111111’ ➔ Tone generator 1 will has 439Hz SIN wave output
:
T17~T10 = ‘00000010’ ➔ Tone generator 1 will has 55978Hz SIN wave output
T17~T10 = ‘00000001’ ➔ Tone generator1 will has 111957Hz
T17~T10 = ‘00000000’ ➔ no used

PAGE1 (PORT7 pull high control)

7	6	5	4	3	2	1	0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0

Bit 0 ~ 7 (PH0 ~ PH7) : PORT7 pull high control bits
0/1 ➔ Disable internal pull-high/enable internal pull-high
These control bits are used to enable the pull-high of PORT7(0 ~ 7) pins.

IOCE (TONE2 control, Open-drain, Counter 1,2 clock source and prescaler)

PAGE0 (TONE2 frequency control)

7	6	5	4	3	2	1	0
T27	T26	T25	T24	T23	T22	T21	T20

Bit 0 ~ Bit 7 (T20 ~ T27) : TONE2 frequency control bits
Clock source = 111957Hz and Freq. = 111957Hz / N, where N = 0 ~ 255 is divider value for T27 ~ T20 Tone generator 2 ‘s frequency divider. Please run in normal mode.
Clock source = 111957Hz
T27~T20 = ‘11111111’ ➔ Tone generator 2 will has 439Hz SIN wave output.
:
T27~T20 = ‘00000010’ ➔ Tone generator 2 will has 55978Hz SIN wave output.
T27~T20 = ‘00000001’ ➔ Tone generator 2 will has 111957Hz SIN wave output.
T27~T20 = ‘00000000’ ➔ no used

		TONE2 (IOCE) High group freq.			
		1203.8 (0X5D)	1332.8(0X54)	1473.1(0X4C)	1646.4(0X44)
TONE1(IOCD, IOCA PAGE1) Low group freq.	699.7Hz(0x0A0)	1	2	3	A
	772.1Hz(0x091)	4	5	6	B
	854.6Hz(0x083)	7	8	9	C
	940.8Hz(0x077)	*	0	#	D

PAGE1 (Open-drain control, Counter 1,2 clock source and prescaler)

7	6	5	4	3	2	1	0
OP77	OP76	C2S	C1S	PSC2	PSC1	PSC0	x

Bit 0 : unused
Bit 1 ~ 2 (PSC1~PSC2) : Counter1 prescaler setting
reset = (0,0,0)

(PSC2,PSC1,PSC0)	Scaler ratio
(0,0,0)	1:1
(0,0,1)	1:2
(0,1,0)	1:4
(0,1,1)	1:8
(1,0,0)	1:16
(1,0,1)	1:32
(1,1,0)	1:64
(1,1,1)	1:128

Bit 4 (C1S) : Counter1 source
0/1 ➔ 32768Hz/MAIN clock if enable

Bit 5 (C2S) : Counter2 source
0/1 ➔ 32768Hz/MAIN clock if enable, scale=1:1
Bit 6 (OP76) : P76 open-drain control
0/1 ➔ disable/enable
Bit 7 (OP77) : P77 open-drain control
0/1 ➔ disable/enable

IOCF (Interrupt mask register)

7	6	5	4	3	2	1	0
EDD	x	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF

Bit 0 ~ 5,7 : interrupt enable bit
1/0 ➔ enable/disable interrupt
Bit 6 : unused
IOCF Register is readable and writable. They work with RF registers.

VII.3 TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8-bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.
- See the prescaler ratio in CONT register.
- Fig. 10 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

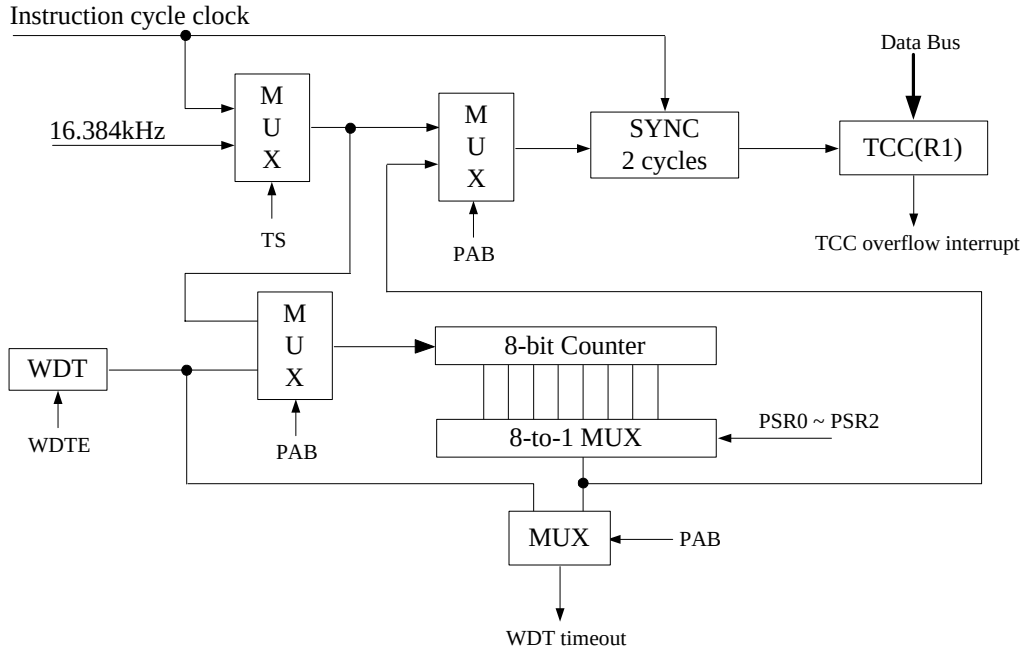


Fig.9 Block diagram of TCC WDT

VII.4 I/O Ports

The I/O registers, Port5 ~ Port 9, are bi-directional tri-state I/O ports. Port 7 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC6 ~ IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.11.

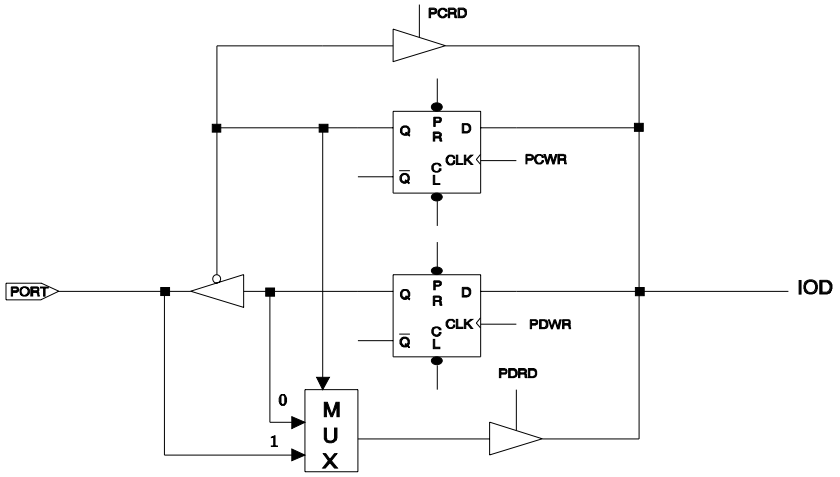


Fig.10 The circuit of I/O port and I/O control register

VII.5 RESET and Wake-up

The RESET can be caused by

(1) External /RESET pin

(2) Power on reset or Power on voltage detector reset(/POVD reset)

(3) WDT timeout. (if enabled and in GREEN or NORMAL mode)

Note that only Power on reset, or only Power on voltage detector reset in Case(2) is enabled in the system by CODE Option bit. If /POVDs disabled, Power on reset is selected in Case (2). Refer to Fig.11.

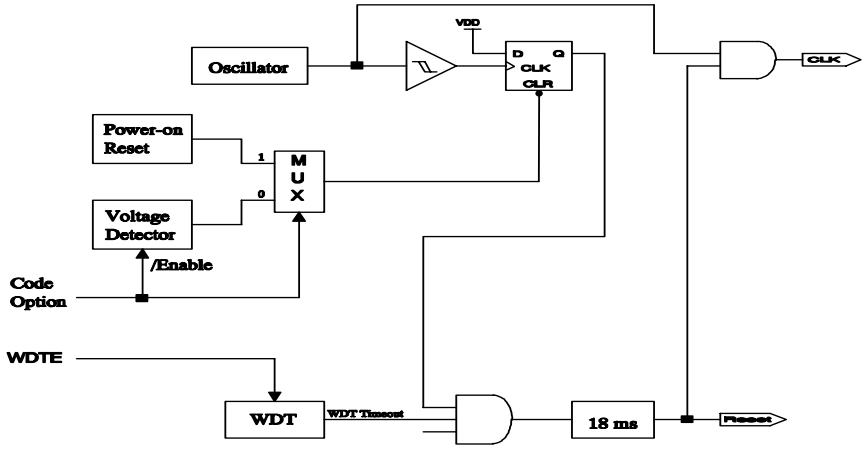


Fig.11 Block diagram of Reset of controller

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"

- The other register (bit7..bit0)

R5 = "xxxx0000"	IOC5 = "1111xxxx"	Page1 IOC5 = "01010000"
R6 = PORT	IOC6 = "11111111"	Page1 IOC6 = "00000000"
R7 = PORT	IOC7 = "11111111"	Page1 IOC7 = "00000000"
R8 = PORT	IOC8 = "11111111"	Page1 IOC8 = "00000000"
R9 = PORT	IOC9 = "11111111"	Page1 IOC9 = "000xxxxx"
RA = "00110000"	Page0 IOCA = "00000000"	Page1 IOCA = "00000000"
RB = "0000x000"	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000"	Page0 IOCC = "xxxxxxxx"	Page1 IOCC = "00000000"
RD = "xxxxxxxx"	Page0 IOCD = "00000000"	Page1 IOCD = "00000000"
RE = "x0000000"	Page0 IOCE = "00000000"	Page1 IOCE = "00000000"
RF = "00000000"	IOCF = "00000000"	

The controller can be awakened from SLEEP mode (execution of "SLEP" instruction, named as SLEEP mode) by (1) WDT time-out (if enabled) (2) external input at PORT9. After CPU is wake-up, user should control Watchdog in case of reset in GREEN mode or NORMAL mode. These two cases will set a RF flag.

VII.6 Interrupt

The CALLER ID IC has internal interrupts which are falling edge triggered, as follows : TCC timer overflow interrupt (internal) , two 8-bit counters overflow interrupt .

If these interrupt sources change signal from high to low , then RF register will generate '1' flag to corresponding register if you enable IOCF register.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are four external interrupt pins including INT0, INT1, INT2, INT3 . And four internal counters interrupt available.

External interrupt INT0, INT1, INT2, INT3 signals are from PORT7 bit0 to bit3 . If IOCF is enable then these signal will cause interrupt , or these signals will be treated as general input data .

After reset, the next instruction will be fetched from address 000H and the instruction interrupt is 001H and the hardware interrupt is 008H.

TCC will go to address 0x08 in GREEN mode or NORMAL mode after time out. These two cases will set a RF flag.

VII.7 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None

0	0000	0001	0000	0010	ENI	Enable Interrupt	None
0	0000	0001	0001	0011	DISI	Disable Interrupt	None
0	0000	0001	0010	0012	RET	[Top of Stack] → PC	None
0	0000	0001	0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0	0000	0001	0100	0014	CONTR	CONT → A	None
0	0000	0001	rrrr	001r	IOR R	IOCR → A	None
0	0000	0010	0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC
0	0000	01rr	rrrr	00rr	MOV R,A	A → R	None
0	0000	1000	0000	0080	CLRA	0 → A	Z
0	0000	11rr	rrrr	00rr	CLR R	0 → R	Z
0	0001	00rr	rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0	0001	01rr	rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0	0001	10rr	rrrr	01rr	DECA R	R-1 → A	Z
0	0001	11rr	rrrr	01rr	DEC R	R-1 → R	Z
0	0010	00rr	rrrr	02rr	OR A,R	A ∨ VR → A	Z
0	0010	01rr	rrrr	02rr	OR R,A	A ∨ VR → R	Z
0	0010	10rr	rrrr	02rr	AND A,R	A & R → A	Z
0	0010	11rr	rrrr	02rr	AND R,A	A & R → R	Z
0	0011	00rr	rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0	0011	01rr	rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0	0011	10rr	rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0	0011	11rr	rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0	0100	00rr	rrrr	04rr	MOV A,R	R → A	Z
0	0100	01rr	rrrr	04rr	MOV R,R	R → R	Z
0	0100	10rr	rrrr	04rr	COMA R	/R → A	Z
0	0100	11rr	rrrr	04rr	COM R	/R → R	Z
0	0101	00rr	rrrr	05rr	INCA R	R+1 → A	Z
0	0101	01rr	rrrr	05rr	INC R	R+1 → R	Z
0	0101	10rr	rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0	0101	11rr	rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0	0110	00rr	rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0	0110	01rr	rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0	0110	10rr	rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0	0110	11rr	rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None

1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1	1110	1000	kkkk	1E8k	PAGE k	K->R5	None
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

VII.8 CODE Option Register

The IC has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

12	11	10	9	8	7	6	5	4	3	2	1	0
												/POVD

Bit 0 (/POVD) : Power on voltage detector reset.

0 ➔ enable

1 ➔ disable

For VDD = 3.3V, the /POVD reset voltage

/POVD	1.8 V /POVD reset	1.6V power on reset	sleep mode current
1	No	yes	1uA
0	yes	no	6uA

Ps. When /POVD is disabled, the CPU reset is by power on reset circuit. When /POVD is enabled, the CPU reset is by /POVD reset circuit.

Bit 1 ~ Bit 12 : unused

VII.10 Energy Detector (DED)

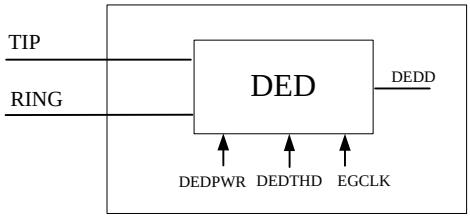


Fig.12 DED diagram

The Energy Detector is differential input and zero crossing detector namead as DED. It can detect any incoming AC signal above its threshold level and output corresponding zero-crossing frequency pulse. For very low power concern, there is no any signal filtering circuit in DED circuit so the user need to have his software algorithm to judge incoming signal by reading its output DEDD bit. For this energy detector, the user can set it's minimum detection threshold level at –30dBm or –45dBm by DEDTHD bit. All the minimum detection value can be achieved under input capacitor around 1000pF ~ 4700pF and input resistor around 22k ~ 100k ohms. The energy detector has power control by IOCA PAGE1 bit 1 (DEDPWR).

Register bits of Energy Detector :

Register bits	Descriptions
RB bit 3 (DEDD)	DEDD : Output data of DED
RB bit 7 (EDGE)	EDGE : edge control of DED output data 0/1 => Falling edge trig. / Rising edge trig.&Falling edge trig.
RE bit 0 (/WUEDD)	/WUEDD : Wake-up control of DED output data 1/0 => enable/disable
RF bit 7 (EDD)	EDD : Interrupt flag of DED output data
IOCF bit 7 (EDD)	EDD : Interrupt mask of DED output data 1/0 ➔ enable/disable interrupt of EDD output data
IOCA PAGE1 bit 0 (DEDTHD)	DEDTHD : Minimum detection threshold of DED 0/1 ➔ -45dBm/-30dBm
IOCA PAGE1 bit 1 (DEDPWR)	DEDPWR : Power control of DED 0/1 ➔ power off/power on
IOCA PAGE1 bit 2 (EGCLK)	Bit 2 (EGCLK) : Operating clock for DED 0/1 ➔ 32.768kHz/3.5826MHz

VII.12 LCD Driver

The CALLER ID IC can drive LCD directly and has 60 segments and 16 commons that can drive 60*16 dots totally. LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating power supply pins.

Duty , bias , the number of segment , the number of common and frame frequency are determined by LCD mode register. LCD control register.

The basic structure contains a timing control which uses the basic frequency 32.768KHz to generate the proper timing for different duty and display access. RE register is a command register for LCD driver, the LCD display(disable, enable, blanking) is controlled by LCD_C and the driving duty and bias is decided by LCD_M and the display data is stored in data RAM which address and data access controlled by registers RC and RD.

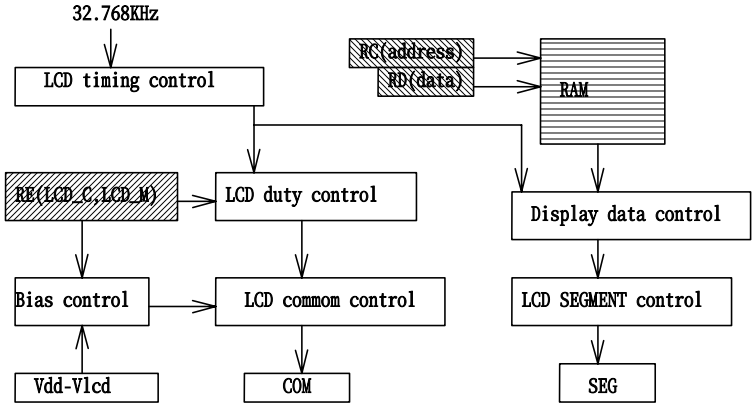


Fig.13 LCD driver control

VII.12.1 LCD Driver Control

RE(LCD Driver Control)(initial state "00000000")

7	6	5	4	3	2	1	0
					LCD_C2	LCD_C1	

Bit 1 ~ 2 (LCD_C1,LCD_C2) : LCD display enable or blanking

The display duty change must set the (LCD_C2,LCD_C1) to (0,0).

(LCD_C2,LCD_C1)	LCD Display Control	duty bias
(0,0)	Disable(turn off LCD)	1/8 1/4 1/8 1/4
(0,1)	Blanking	:
(1,1)	LCD display enable	:

VII.12.2 LCD display area

The LCD display data is stored in the data RAM. The relation of data area and COM/SEG pin is as below :

The relation of data area and COM/SEG pin is as below :

COM7 ~ COM0	
00H (Bit7 ~ Bit0)	SEG0
01H	SEG1
:	:
17H	SEG23
18H	(empty)
:	:
1FH	(empty)

IOCB(LCD Display RAM address)

7	6	5	4	3	2	1	0
-	-	-	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

* Bit 0 ~ Bit 5 : select LCD Display RAM addresses up to 23.
LCD RAM can be write whether in enable or disable mode and read only in disable mode.
IOCC (LCD Display data) : Bit 0 ~ Bit 7 are LCD data.

VII.12.3 LCD COM and SEG signal

COM signal : The number of COM pins varies according to the duty cycle used, as following: in 1/8 duty mode

	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
1/8	o	o	o	o	o	o	o	o

x : open, o : select,
SEG signal: The 24 segment signal pins are connected to the corresponding display RAM address 0 to 23. The high bit and the low bit (bit7 down to bit0) are correlated to COM7 to COM0 respectively.
When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0, a non-select signal is sent to the corresponding segment pin.
*COM, SEG and Select/Non-select signal is shown as following:

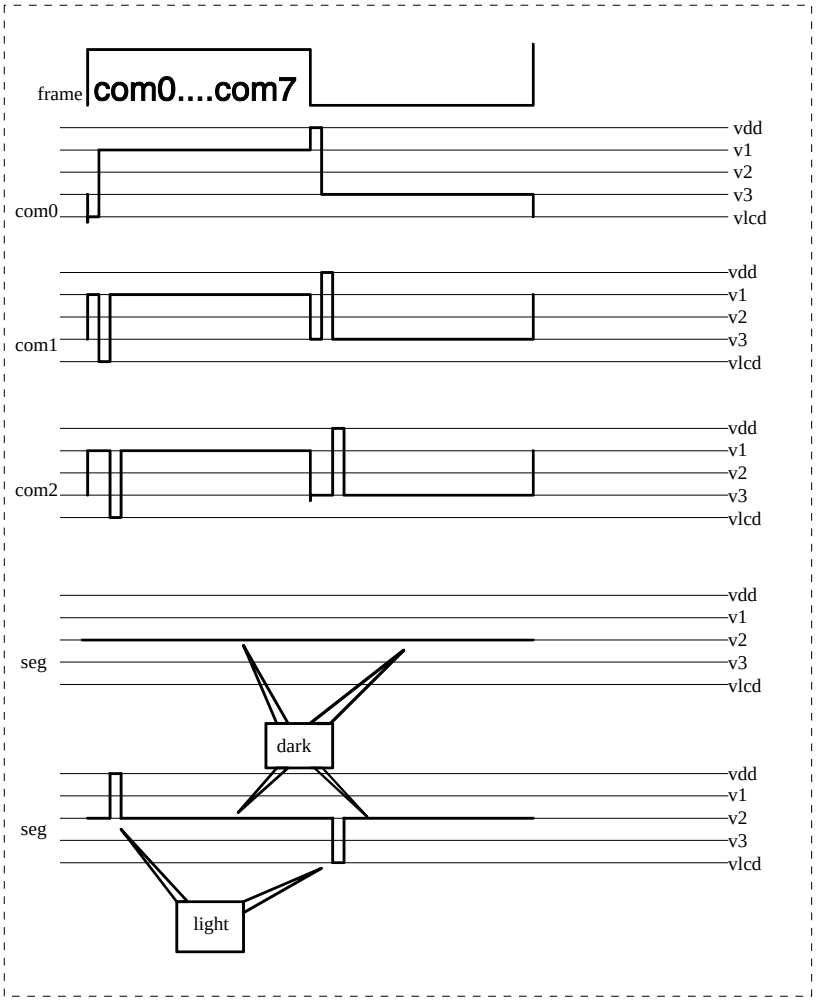


Fig.14 LCD wave 1/4 bias, 1/8 duty

VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	Vdd	-0.3 To 3.6	V
INPUT VOLTAGE	Vin	-0.3 TO Vdd +0.5	V
OPERATING TEMPERATURE RANGE	Ta	0 TO 70	℃

IX DC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=3.3V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL1	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
IIL2	Input Leakage Current for bi-directional pins	VIN = VDD, VSS			±1	μA
VIH	Input High Voltage		2.5			V
VIL	Input Low Voltage				0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC, RDET1	2.0			V
VILT	Input Low Threshold Voltage	/RESET, TCC,RDET1			0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5			V
VILX	Clock Input Low Voltage	OSCI			1.5	V
VOH1	Output High Voltage (port5,6,7,8)	IOH = -1.6mA	2.4			V
	(port9)	IOH = -6.0mA	2.4			V
VOL1	Output Low Voltage (port5,6,7,8)	IOL = 1.6mA			0.4	V
	(port9)	IOL = 6.0mA			0.4	V
Vcom	Com voltage drop	Io=+/- 50 uA	-	-	2.9	V
Vseg	Segment voltage drop	Io=+/- 50 uA	-	-	3.8	V
Vlcd	LCD drive reference voltage	Contrast adjustment				
IPH	Pull-high current	Pull-high active input pin at VSS		-10	-15	μA
ISB1	Power down current (SLEEP mode) POVD disable	All input and I/O pin at VDD, output pin floating, WDT disabled		1	4	μA
	Power down current (SLEEP mode) POVD enable			10	15	uA
ISB2	Low clock current (GREEN mode) POVD disable	CLK=32.768KHz,TONE block disable , All input and I/O pin at VDD, output pin floating, WDT disabled, LCD disable		35	50	μA
	Low clock current (GREEN mode) POVD enable			45	65	uA
ISB4	Low clock current (GREEN mode) POVD disable, DED enable	CLK=32.768KHz, All input and I/O pin at VDD, output pin floating, WDT disabled, LCD disable, other analog		55	75	μA

	Low clock current (GREEN mode) POVD enable, DED enable	Circuits disabled		65	90	uA
ICC1	Operating supply current (CPU enable)	/RESET=High, CLK=3.5826MHz, output pin floating, other analog circuits disabled		1	1.6	mA
ICC2	Operating supply current (CPU and DTMF receiver enable)	/RESET=High, DTMF receiver enable , CLK=3.5826MHz, output pin floating, other analog circuits disable		2.3	3	mA
ICC3	Operating supply current (CPU and FSK enable)	/RESET=High, FSK block enable , CLK=3.5826MHz, output pin floating, DTMF receiver and TONE block disable		2.3	3	mA
Vref2	Tone generator reference voltage		0.5		0.7	VDD
V1rms	Tone1 signal strength	Root mean square voltage	130	155	180	mV
V2rms	Tone2 signal strength	Root mean square voltage	1.259V1rms			mV

Ps. V1rms and V2rms has 2 dB difference. It means 20log(V2rms/V1rms) = 20log1.259 = 2 (dB)

Energy Detector (DED) (Ta=0°C ~ 70°C, VDD=3.3V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DED}	Operating current for Energy Detector	Not including MCU and other parts		15	20	uA

IX AC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=3.3V, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time	32.768KHz 3.5826MHz		60 550		us ns
Tdrh	Device delay hold time			18		ms
Ttcc	TCC input period	Note 1	(Tins+20)/N			ns
Twdt	Watchdog timer period	Ta = 25°C		18		ms

Note 1: N= selected prescaler ratio.

Tdiea	Delay from Phase 3 end to INSEND active	Cl=100pF			30	ns
Tdiei	Delay from Phase 4 end to INSEND inactive	Cl=100pF			30	ns
Tiew	INSEND pulse width		30			ns
Tdca	Delay from Phase 4 end to CA Bus valid	C1=100pF			30	ns
Tacc	ROM data access time		100			ns
Tcds	ROM data setup time		20			ns
Tcdh	ROM data hold time		20			ns
Tdca-1	Delay time of CA-1	C1=100pF			30	ns

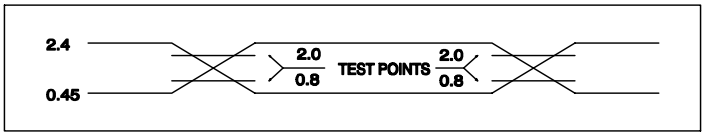
Note 1: N= selected prescaler ratio.

(DED AC Characteristic)(Vdd=+3.3V,Ta=+25℃)

CHARACTERISTIC	MIN	TYP	MAX	UNIT
Input sensitivity TIP and RING for DED, DEDTHD bit=0		-45	--	dBm
Input sensitivity TIP and RING for DED, DEDTHD bit=1		-30	--	dBm

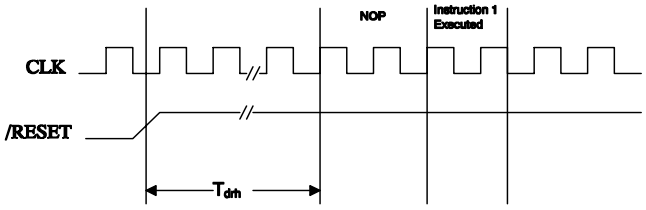
XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

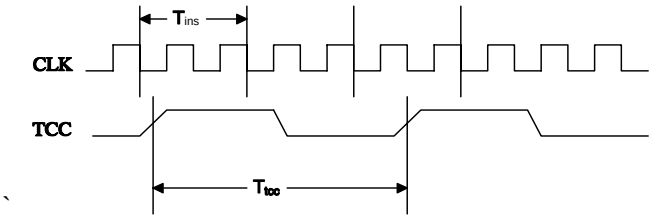


Fig.15 AC timing

XII. Application Circuit

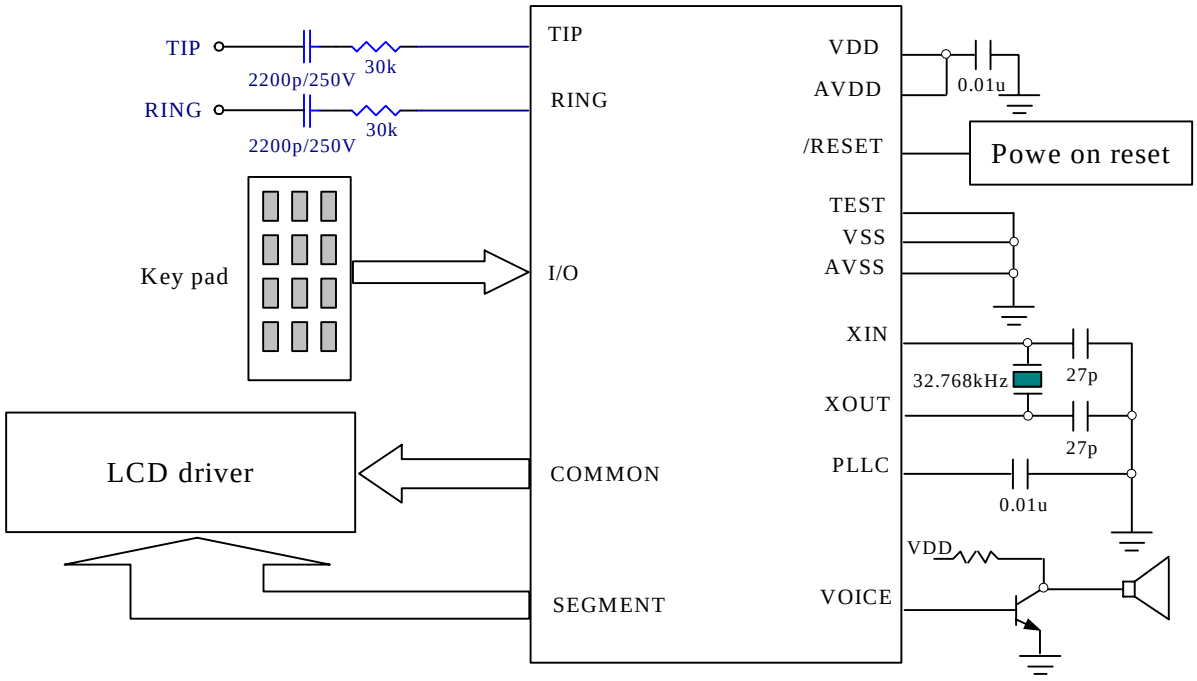


Fig.16 Application circuit

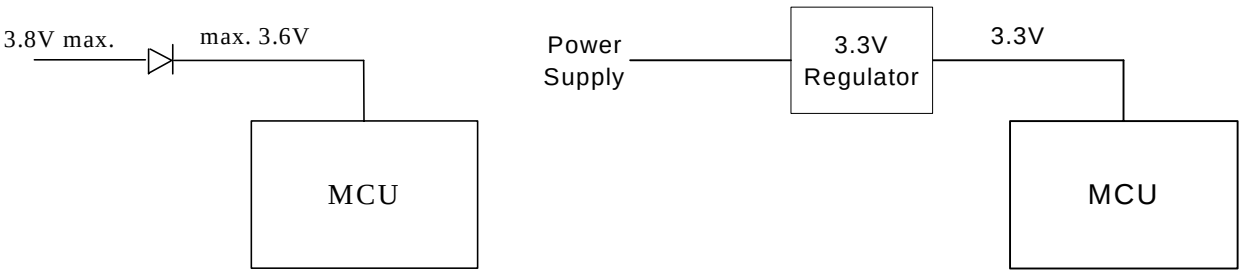


Fig.17 Power Concern in Application