Elan Microelectronics Crop.

CONFIDENTIAL

EM65567

66COM/ 96SEG 256 Color STN LCD Driver

January 9, 2003

Version 0.1 (Preliminary)

EM65567 Specification Revision History		
Version	**Content**	**Date**
0.1	Initial version	January 9, 2003

Caution: The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Contents

1. General description

EM65567 is one of the industry's most advanced wide-screen STN-LCD drivers for 256-color display. The industry's first sub-screen display function makes it possible to display different images and data in a sub-screen inside the main LCD screen. It also has a built-in display RAM, a power supply circuit for LCD drive, and an LCD controller circuit, therefore contributing to compact system design. Its partial display function realizes low power consumption.

*Partial display function: A function that utilizes only part of the screen, thus reducing power consumption.

2. Feature

- Display RAM capacity
  - Graphic: 96*64*(3+3+2)=49,152 bits
  - Icons: 96*2*(3+3+2)=1,536 bits
- Ratio of display duty cycle: 1/10, 1/18, 1/26, 1/34, 1/42, 1/50, 1/58, 1/66
- Outputs
  - Segment:96 RGB (288) outputs, Common: 66 outputs
  - Static driver: 2 outputs
- Built-in display RAM and power supply circuit
- Partial display functions
- Switchable display in black and white mode
- Bus connection with 80-family/ 68-family /Elan MCU
- Serial interface is available
- Logic power supply voltage: 1.8 to 3.3 V
- LCD driving voltage: 5.0 to 12.0 V
- Booster: 2 to 4 times
- Write system cycle: 140 ns
- Package (Ordering information):

Part Number	Package	Description	Package information
EM65567AGH	Gold bumped chip	NA	Page 5
EM65567AF	COF	64x96RGB (Version A)	Page 91

Note: The EM65567 series has the following sub-codes depending on their shapes.

H: Bare chip (Aluminum pad without bumped); **GH**: Gold bumped chip;

F: COF package; **T**: TAB (TCP) package

Example EM65567AF → EM65567: Elan number ; A: Package Version ; F: COF package

3. Applications

- Mobile phone
- DSC
- Small PDA

4. Pin configurations

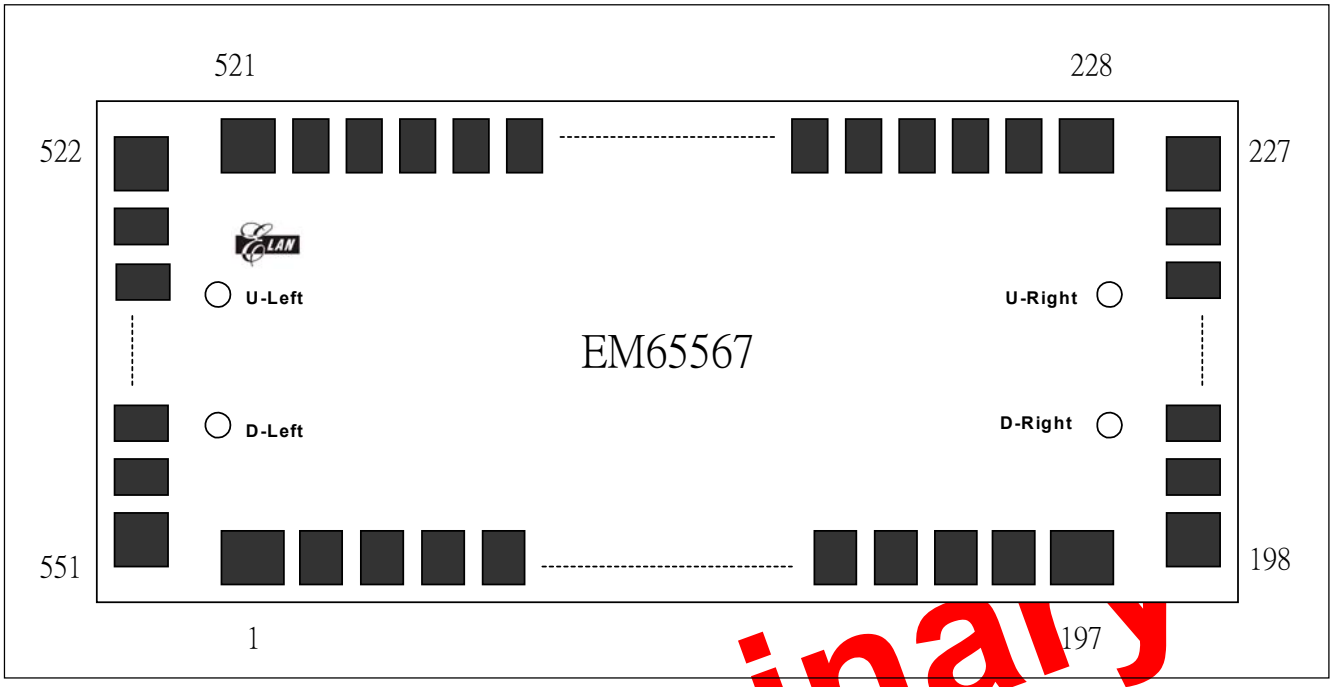


Figure 1. Pin configuration

Note: With the Elan logo in upper left the pin 1 is in the down left corner.

Mark	Coordinate (X,Y)	Mark	Coordinate (X,Y)
U-Left	-7241.1 ,141.6	U-Right	7247.9,141.6
D-Left	-7241.1 ,-208.4	D-Right	7247.9,-208.4

PIN DIMENSIONS

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	15450	1770	μm
Pad Pitch	1,197	82		
	2 ~ 196	70		
	198,227,228 521,522,551	56		
	199 ~ 226 229~ 520 523 ~ 550	50		
Bump Size	1, 197	70	63	
	2 ~ 196	46	63	
	198, 227, 522, 551	63	48	
	228, 521	48	63	
	199~226	63	36	
	229 ~ 520	36	63	
	523 ~ 550	63	36	
Die thickness (excluding bumps)	526 +/- 25			
Bump Height	All Pad 17 +/- 3 (within die)			
Minimum Bump Gap	14			
Coordinate Origin	Chip center			

PAD Coordinates Table

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
1	DUMMY	-7299.9 ,-765.0	51	CSB	-3575.6 ,-765.0
2	DUMMY	-7217.9 ,-765.0	52	CSB	-3505.6 ,-765.0
3	DUMMY	-7147.9 ,-765.0	53	RS	-3435.6 ,-765.0
4	DUMMY	-7077.9 ,-765.0	54	RS	-3365.6 ,-765.0
5	DUMMY	-7007.9 ,-765.0	55	VSS	-3295.6 ,-765.0
6	SSEG	-6937.9 ,-765.0	56	VSS	-3225.6 ,-765.0
7	V0	-6867.9 ,-765.0	57	VSS	-3155.6 ,-765.0
8	V0	-6797.9 ,-765.0	58	VSS	-3085.6 ,-765.0
9	V0	-6727.9 ,-765.0	59	M/S	-3015.6 ,-765.0
10	V0	-6657.9 ,-765.0	60	M/S	-2945.6 ,-765.0
11	V0	-6587.9 ,-765.0	61	VDD	-2875.6 ,-765.0
12	V1	-6517.9 ,-765.0	62	VDD	-2805.6 ,-765.0
13	V1	-6447.9 ,-765.0	63	VDD	-2735.6 ,-765.0
14	V1	-6377.9 ,-765.0	64	VDD	-2665.6 ,-765.0
15	V1	-6307.9 ,-765.0	65	P/S	-2595.6 ,-765.0
16	V1	-6237.9 ,-765.0	66	P/S	-2525.6 ,-765.0
17	V2	-6167.9 ,-765.0	67	M86	-2455.6 ,-765.0
18	V2	-6097.9 ,-765.0	68	M86	-2385.6 ,-765.0
19	V2	-6027.9 ,-765.0	69	VSS	-2315.6 ,-765.0
20	V2	-5957.9 ,-765.0	70	VSS	-2245.6 ,-765.0
21	V2	-5887.9 ,-765.0	71	VSS	-2175.6 ,-765.0
22	V3	-5817.9 ,-765.0	72	VSS	-2105.6 ,-765.0
23	V3	-5747.9 ,-765.0	73	VSS	-2035.6 ,-765.0
24	V3	-5677.9 ,-765.0	74	WRB	-1965.6 ,-765.0
25	V3	-5607.9 ,-765.0	75	WRB	-1895.6 ,-765.0
26	V3	-5537.9 ,-765.0	76	RDB	-1825.6 ,-765.0
27	V4	-5467.9 ,-765.0	77	RDB	-1755.6 ,-765.0
28	V4	-5397.9 ,-765.0	78	VDD	-1473.3 ,-765.0
29	V4	-5327.9 ,-765.0	79	VDD	-1403.3 ,-765.0
30	V4	-5257.9 ,-765.0	80	VDD	-1333.3 ,-765.0
31	V4	-5187.9 ,-765.0	81	VDD	-1263.3 ,-765.0
32	VSSH	-5117.9 ,-765.0	82	VDD	-1193.3 ,-765.0
33	VSSH	-5047.9 ,-765.0	83	D0	-1123.3 ,-765.0
34	VSSH	-4977.9 ,-765.0	84	D0	-1053.3 ,-765.0
35	VSSH	-4907.9 ,-765.0	85	D1	-983.3 ,-765.0
36	VSSH	-4837.9 ,-765.0	86	D1	-913.3 ,-765.0
37	DUMMY	-4767.9 ,-765.0	87	D2	-843.3 ,-765.0
38	DUMMY	-4485.6 ,-765.0	88	D2	-773.3 ,-765.0
39	DUMMY	-4415.6 ,-765.0	89	D3	-703.3 ,-765.0
40	DUMMY	-4345.6 ,-765.0	90	D3	-633.3 ,-765.0
41	DUMMY	-4275.6 ,-765.0	91	D4	-563.3 ,-765.0
42	VSSL	-4205.6 ,-765.0	92	D4	-493.3 ,-765.0
43	VSSL	-4135.6 ,-765.0	93	D5	-423.3 ,-765.0
44	VSSL	-4065.6 ,-765.0	94	D5	-353.3 ,-765.0
45	VSSL	-3995.6 ,-765.0	95	D6	-283.3 ,-765.0
46	VSSL	-3925.6 ,-765.0	96	D6	-213.3 ,-765.0
47	TEST	-3855.6 ,-765.0	97	D7	-143.3 ,-765.0
48	TEST	-3785.6 ,-765.0	98	D7	-73.3 ,-765.0
49	RESB	-3715.6 ,-765.0	99	D8	-3.3 ,-765.0
50	RESB	-3645.6 ,-765.0	100	D8	66.7 ,-765.0

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
101	D9	136.7 ,-765.0	151	VEE	3849.0 ,-765.0
102	D9	206.7 ,-765.0	152	VREG	3919.0 ,-765.0
103	D10	276.7 ,-765.0	153	VREG	3989.0 ,-765.0
104	D10	346.7 ,-765.0	154	VREG	4059.0 ,-765.0
105	D11	416.7 ,-765.0	155	VREG	4129.0 ,-765.0
106	D11	486.7 ,-765.0	156	VREG	4199.0 ,-765.0
107	D12	556.7 ,-765.0	157	VOUT	4481.3 ,-765.0
108	D12	626.7 ,-765.0	158	VOUT	4551.3 ,-765.0
109	D13	696.7 ,-765.0	159	VOUT	4621.3 ,-765.0
110	D13	766.7 ,-765.0	160	VOUT	4691.3 ,-765.0
111	D14	836.7 ,-765.0	161	VOUT	4761.3 ,-765.0
112	D14	906.7 ,-765.0	162	CAP1-	4831.3 ,-765.0
113	D15	976.7 ,-765.0	163	CAP1-	4901.3 ,-765.0
114	D15	1046.7 ,-765.0	164	CAP1-	4971.3 ,-765.0
115	LP	1116.7 ,-765.0	165	CAP1-	5041.3 ,-765.0
116	LP	1186.7 ,-765.0	166	CAP1-	5111.3 ,-765.0
117	FLM	1469.0 ,-765.0	167	CAP1+	5181.3 ,-765.0
118	FLM	1539.0 ,-765.0	168	CAP1+	5251.3 ,-765.0
119	M	1609.0 ,-765.0	169	CAP1+	5321.3 ,-765.0
120	M	1679.0 ,-765.0	170	CAP1+	5391.3 ,-765.0
121	CLK	1749.0 ,-765.0	171	CAP1+	5461.3 ,-765.0
122	CLK	1819.0 ,-765.0	172	CAP2-	5531.3 ,-765.0
123	VSS	1889.0 ,-765.0	173	CAP2-	5601.3 ,-765.0
124	VSS	1959.0 ,-765.0	174	CAP2-	5671.3 ,-765.0
125	VSS	2029.0 ,-765.0	175	CAP2-	5741.3 ,-765.0
126	VSS	2099.0 ,-765.0	176	CAP2-	5811.3 ,-765.0
127	VSS	2169.0 ,-765.0	177	CAP2+	5881.3 ,-765.0
128	CK	2239.0 ,-765.0	178	CAP2+	5951.3 ,-765.0
129	CK	2309.0 ,-765.0	179	CAP2+	6021.3 ,-765.0
130	CKS	2379.0 ,-765.0	180	CAP2+	6091.3 ,-765.0
131	CKS	2449.0 ,-765.0	181	CAP2+	6161.3 ,-765.0
132	VDD	2519.0 ,-765.0	182	CAP3-	6231.3 ,-765.0
133	VDD	2589.0 ,-765.0	183	CAP3-	6301.3 ,-765.0
134	VDD	2659.0 ,-765.0	184	CAP3-	6371.3 ,-765.0
135	VDD	2729.0 ,-765.0	185	CAP3-	6441.3 ,-765.0
136	VDD	2799.0 ,-765.0	186	CAP3-	6511.3 ,-765.0
137	DUMMY	2869.0 ,-765.0	187	CAP3+	6581.3 ,-765.0
138	DUMMY	2939.0 ,-765.0	188	CAP3+	6651.3 ,-765.0
139	DUMMY	3009.0 ,-765.0	189	CAP3+	6721.3 ,-765.0
140	DUMMY	3079.0 ,-765.0	190	CAP3+	6791.3 ,-765.0
141	DUMMY	3149.0 ,-765.0	191	CAP3+	6861.3 ,-765.0
142	VREF	3219.0 ,-765.0	192	SCOM	6931.3 ,-765.0
143	VREF	3289.0 ,-765.0	193	DUMMY	7001.3 ,-765.0
144	VREF	3359.0 ,-765.0	194	DUMMY	7071.3 ,-765.0
145	VREF	3429.0 ,-765.0	195	DUMMY	7141.3 ,-765.0
146	VREF	3499.0 ,-765.0	196	DUMMY	7211.3 ,-765.0
147	VEE	3569.0 ,-765.0	197	DUMMY	7293.3 ,-765.0
148	VEE	3639.0 ,-765.0	198	COM31	7605.0 ,-726.0
149	VEE	3709.0 ,-765.0	199	COM30	7605.0 ,-670.0
150	VEE	3779.0 ,-765.0	200	COM29	7605.0 ,-620.0

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
201	COM28	7605.0 ,-570.	251	SEGC6	6175.0 ,765.0
202	COM27	7605.0 ,-520.	252	SEGA7	6125.0 ,765.0
203	COM26	7605.0 ,-470.	253	SEGB7	6075.0 ,765.0
204	COM25	7605.0 ,-420.	254	SEGC7	6025.0 ,765.0
205	COM24	7605.0 ,-370.	255	SEGA8	5975.0 ,765.0
206	COM23	7605.0 ,-320.	256	SEGB8	5925.0 ,765.0
207	COM22	7605.0 ,-270.	257	SEGC8	5875.0 ,765.0
208	COM21	7605.0 ,-220.	258	SEGA9	5825.0 ,765.0
209	COM20	7605.0 ,-170.	259	SEGB9	5775.0 ,765.0
210	COM19	7605.0 ,-120.	260	SEGC9	5725.0 ,765.0
211	COM18	7605.0 ,-70.0	261	SEGA10	5675.0 ,765.0
212	COM17	7605.0 ,-20.0	262	SEGB10	5625.0 ,765.0
213	COM16	7605.0 ,30.0	263	SEGC10	5575.0 ,765.0
214	COM15	7605.0 ,80.0	264	SEGA11	5525.0 ,765.0
215	COM14	7605.0 ,130.0	265	SEGB11	5475.0 ,765.0
216	COM13	7605.0 ,180.0	266	SEGC11	5425.0 ,765.0
217	COM12	7605.0 ,230.0	267	SEGA12	5375.0 ,765.0
218	COM11	7605.0 ,280.0	268	SEGB12	5325.0 ,765.0
219	COM10	7605.0 ,330.0	269	SEGC12	5275.0 ,765.0
220	COM9	7605.0 ,380.0	270	SEGA13	5225.0 ,765.0
221	COM8	7605.0 ,430.0	271	SEGB13	5175.0 ,765.0
222	COM7	7605.0 ,480.0	272	SEGC13	5125.0 ,765.0
223	COM6	7605.0 ,530.0	273	SEGA14	5075.0 ,765.0
224	COM5	7605.0 ,580.0	274	SEGB14	5025.0 ,765.0
225	COM4	7605.0 ,630.0	275	SEGC14	4975.0 ,765.0
226	COM3	7605.0 ,680.0	276	SEGA15	4925.0 ,765.0
227	COM2	7605.0 ,736.0	277	SEGB15	4875.0 ,765.0
228	COM1	7331.0 ,765.0	278	SEGC15	4825.0 ,765.0
229	COM0	7275.0 ,765.0	279	SEGA16	4775.0 ,765.0
230	COMA	7225.0 ,765.0	280	SEGB16	4725.0 ,765.0
231	SEGA0	7175.0 ,765.0	281	SEGC16	4675.0 ,765.0
232	SEGB0	7125.0 ,765.0	282	SEGA17	4625.0 ,765.0
233	SEGC0	7075.0 ,765.0	283	SEGB17	4575.0 ,765.0
234	SEGA1	7025.0 ,765.0	284	SEGC17	4525.0 ,765.0
235	SEGB1	6975.0 ,765.0	285	SEGA18	4475.0 ,765.0
236	SEGC1	6925.0 ,765.0	286	SEGB18	4425.0 ,765.0
237	SEGA2	6875.0 ,765.0	287	SEGC18	4375.0 ,765.0
238	SEGB2	6825.0 ,765.0	288	SEGA19	4325.0 ,765.0
239	SEGC2	6775.0 ,765.0	289	SEGB19	4275.0 ,765.0
240	SEGA3	6725.0 ,765.0	290	SEGC19	4225.0 ,765.0
241	SEGB3	6675.0 ,765.0	291	SEGA20	4175.0 ,765.0
242	SEGC3	6625.0 ,765.0	292	SEGB20	4125.0 ,765.0
243	SEGA4	6575.0 ,765.0	293	SEGC20	4075.0 ,765.0
244	SEGB4	6525.0 ,765.0	294	SEGA21	4025.0 ,765.0
245	SEGC4	6475.0 ,765.0	295	SEGB21	3975.0 ,765.0
246	SEGA5	6425.0 ,765.0	296	SEGC21	3925.0 ,765.0
247	SEGB5	6375.0 ,765.0	297	SEGA22	3875.0 ,765.0
248	SEGC5	6325.0 ,765.0	298	SEGB22	3825.0 ,765.0
249	SEGA6	6275.0 ,765.0	299	SEGC22	3775.0 ,765.0
250	SEGB6	6225.0 ,765.0	300	SEGA23	3725.0 ,765.0

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
301	SEGB23	3675.0 ,765.0	351	SEGA40	1175.0 ,765.0
302	SEGC23	3625.0 ,765.0	352	SEGB40	1125.0 ,765.0
303	SEGA24	3575.0 ,765.0	353	SEGC40	1075.0 ,765.0
304	SEGB24	3525.0 ,765.0	354	SEGA41	1025.0 ,765.0
305	SEGC24	3475.0 ,765.0	355	SEGB41	975.0 ,765.0
306	SEGA25	3425.0 ,765.0	356	SEGC41	925.0 ,765.0
307	SEGB25	3375.0 ,765.0	357	SEGA42	875.0 ,765.0
308	SEGC25	3325.0 ,765.0	358	SEGB42	825.0 ,765.0
309	SEGA26	3275.0 ,765.0	359	SEGC42	775.0 ,765.0
310	SEGB26	3225.0 ,765.0	360	SEGA43	725.0 ,765.0
311	SEGC26	3175.0 ,765.0	361	SEGB43	675.0 ,765.0
312	SEGA27	3125.0 ,765.0	362	SEGC43	625.0 ,765.0
313	SEGB27	3075.0 ,765.0	363	SEGA44	575.0 ,765.0
314	SEGC27	3025.0 ,765.0	364	SEGB44	525.0 ,765.0
315	SEGA28	2975.0 ,765.0	365	SEGC44	475.0 ,765.0
316	SEGB28	2925.0 ,765.0	366	SEGA45	425.0 ,765.0
317	SEGC28	2875.0 ,765.0	367	SEGB45	375.0 ,765.0
318	SEGA29	2825.0 ,765.0	368	SEGC45	325.0 ,765.0
319	SEGB29	2775.0 ,765.0	369	SEGA46	275.0 ,765.0
320	SEGC29	2725.0 ,765.0	370	SEGB46	225.0 ,765.0
321	SEGA30	2675.0 ,765.0	371	SEGC46	175.0 ,765.0
322	SEGB30	2625.0 ,765.0	372	SEGA47	125.0 ,765.0
323	SEGC30	2575.0 ,765.0	373	SEGB47	75.0 ,765.0
324	SEGA31	2525.0 ,765.0	374	SEGC47	25.0 ,765.0
325	SEGB31	2475.0 ,765.0	375	SEGA48	-25.0 ,765.0
326	SEGC31	2425.0 ,765.0	376	SEGB48	-75.0 ,765.0
327	SEGA32	2375.0 ,765.0	377	SEGC48	-125.0 ,765.0
328	SEGB32	2325.0 ,765.0	378	SEGA49	-175.0 ,765.0
329	SEGC32	2275.0 ,765.0	379	SEGB49	-225.0 ,765.0
330	SEGA33	2225.0 ,765.0	380	SEGC49	-275.0 ,765.0
331	SEGB33	2175.0 ,765.0	381	SEGA50	-325.0 ,765.0
332	SEGC33	2125.0 ,765.0	382	SEGB50	-375.0 ,765.0
333	SEGA34	2075.0 ,765.0	383	SEGC50	-425.0 ,765.0
334	SEGB34	2025.0 ,765.0	384	SEGA51	-475.0 ,765.0
335	SEGC34	1975.0 ,765.0	385	SEGB51	-525.0 ,765.0
336	SEGA35	1925.0 ,765.0	386	SEGC51	-575.0 ,765.0
337	SEGB35	1875.0 ,765.0	387	SEGA52	-625.0 ,765.0
338	SEGC35	1825.0 ,765.0	388	SEGB52	-675.0 ,765.0
339	SEGA36	1775.0 ,765.0	389	SEGC52	-725.0 ,765.0
340	SEGB36	1725.0 ,765.0	390	SEGA53	-775.0 ,765.0
341	SEGC36	1675.0 ,765.0	391	SEGB53	-825.0 ,765.0
342	SEGA37	1625.0 ,765.0	392	SEGC53	-875.0 ,765.0
343	SEGB37	1575.0 ,765.0	393	SEGA54	-925.0 ,765.0
344	SEGC37	1525.0 ,765.0	394	SEGB54	-975.0 ,765.0
345	SEGA38	1475.0 ,765.0	395	SEGC54	-1025.0 ,765.0
346	SEGB38	1425.0 ,765.0	396	SEGA55	-1075.0 ,765.0
347	SEGC38	1375.0 ,765.0	397	SEGB55	-1125.0 ,765.0
348	SEGA39	1325.0 ,765.0	398	SEGC55	-1175.0 ,765.0
349	SEGB39	1275.0 ,765.0	399	SEGA56	-1225.0 ,765.0
350	SEGC39	1225.0 ,765.0	400	SEGB56	-1275.0 ,765.0

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
401	SEGC56	-1325.0 ,765.0	451	SEGB73	-3825.0 ,765.0
402	SEGA57	-1375.0 ,765.0	452	SEGC73	-3875.0 ,765.0
403	SEGB57	-1425.0 ,765.0	453	SEGA74	-3925.0 ,765.0
404	SEGC57	-1475.0 ,765.0	454	SEGB74	-3975.0 ,765.0
405	SEGA58	-1525.0 ,765.0	455	SEGC74	-4025.0 ,765.0
406	SEGB58	-1575.0 ,765.0	456	SEGA75	-4075.0 ,765.0
407	SEGC58	-1625.0 ,765.0	457	SEGB75	-4125.0 ,765.0
408	SEGA59	-1675.0 ,765.0	458	SEGC75	-4175.0 ,765.0
409	SEGB59	-1725.0 ,765.0	459	SEGA76	-4225.0 ,765.0
410	SEGB59	-1775.0 ,765.0	460	SEGB76	-4275.0 ,765.0
411	SEGA60	-1825.0 ,765.0	461	SEGC76	-4325.0 ,765.0
412	SEGB60	-1875.0 ,765.0	462	SEGA77	-4375.0 ,765.0
413	SEGC60	-1925.0 ,765.0	463	SEGB77	-4425.0 ,765.0
414	SEGA61	-1975.0 ,765.0	464	SEGC77	-4475.0 ,765.0
415	SEGB61	-2025.0 ,765.0	465	SEGA78	-4525.0 ,765.0
416	SEGC61	-2075.0 ,765.0	466	SEGB78	-4575.0 ,765.0
417	SEGA62	-2125.0 ,765.0	467	SEGC78	-4625.0 ,765.0
418	SEGB62	-2175.0 ,765.0	468	SEGA79	-4675.0 ,765.0
419	SEGC62	-2225.0 ,765.0	469	SEGB79	-4725.0 ,765.0
420	SEGA63	-2275.0 ,765.0	470	SEGC79	-4775.0 ,765.0
421	SEGB63	-2325.0 ,765.0	471	SEGA80	-4825.0 ,765.0
422	SEGC63	-2375.0 ,765.0	472	SEGB80	-4875.0 ,765.0
423	SEGA64	-2425.0 ,765.0	473	SEGC80	-4925.0 ,765.0
424	SEGB64	-2475.0 ,765.0	474	SEGA81	-4975.0 ,765.0
425	SEGC64	-2525.0 ,765.0	475	SEGB81	-5025.0 ,765.0
426	SEGA65	-2575.0 ,765.0	476	SEGC81	-5075.0 ,765.0
427	SEGB65	-2625.0 ,765.0	477	SEGA82	-5125.0 ,765.0
428	SEGC65	-2675.0 ,765.0	478	SEGB82	-5175.0 ,765.0
429	SEGA66	-2725.0 ,765.0	479	SEGC82	-5225.0 ,765.0
430	SEGB66	-2775.0 ,765.0	480	SEGA83	-5275.0 ,765.0
431	SEGC66	-2825.0 ,765.0	481	SEGB83	-5325.0 ,765.0
432	SEGA67	-2875.0 ,765.0	482	SEGC83	-5375.0 ,765.0
433	SEGB67	-2925.0 ,765.0	483	SEGA84	-5425.0 ,765.0
434	SEGC67	-2975.0 ,765.0	484	SEGB84	-5475.0 ,765.0
435	SEGA68	-3025.0 ,765.0	485	SEGC84	-5525.0 ,765.0
436	SEGB68	-3075.0 ,765.0	486	SEGA85	-5575.0 ,765.0
437	SEGC68	-3125.0 ,765.0	487	SEGB85	-5625.0 ,765.0
438	SEGA69	-3175.0 ,765.0	488	SEGC85	-5675.0 ,765.0
439	SEGB69	-3225.0 ,765.0	489	SEGA86	-5725.0 ,765.0
440	SEGC69	-3275.0 ,765.0	490	SEGB86	-5775.0 ,765.0
441	SEGA70	-3325.0 ,765.0	491	SEGC86	-5825.0 ,765.0
442	SEGB70	-3375.0 ,765.0	492	SEGA87	-5875.0 ,765.0
443	SEGC70	-3425.0 ,765.0	493	SEGB87	-5925.0 ,765.0
444	SEGA71	-3475.0 ,765.0	494	SEGC87	-5975.0 ,765.0
445	SEGB71	-3525.0 ,765.0	495	SEGA88	-6025.0 ,765.0
446	SEGC71	-3575.0 ,765.0	496	SEGB88	-6075.0 ,765.0
447	SEGA72	-3625.0 ,765.0	497	SEGC88	-6125.0 ,765.0
448	SEGB72	-3675.0 ,765.0	498	SEGA89	-6175.0 ,765.0
449	SEGC72	-3725.0 ,765.0	499	SEGB89	-6225.0 ,765.0
450	SEGA73	-3775.0 ,765.0	500	SEGC89	-6275.0 ,765.0

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
501	SEGA90	-6325.0 ,765.0	551	COMB	-7605.0 ,-726.0
502	SEGB90	-6375.0 ,765.0			
503	SEGC90	-6425.0 ,765.0			
504	SEGA91	-6475.0 ,765.0			
505	SEGB91	-6525.0 ,765.0			
506	SEGC91	-6575.0 ,765.0			
507	SEGA92	-6625.0 ,765.0			
508	SEGB92	-6675.0 ,765.0			
509	SEGC92	-6725.0 ,765.0			
510	SEGA93	-6775.0 ,765.0			
511	SEGB93	-6825.0 ,765.0			
512	SEGC93	-6875.0 ,765.0			
513	SEGA94	-6925.0 ,765.0			
514	SEGB94	-6975.0 ,765.0			
515	SEGC94	-7025.0 ,765.0			
516	SEGA95	-7075.0 ,765.0			
517	SEGB95	-7125.0 ,765.0			
518	SEGC95	-7175.0 ,765.0			
519	COM32	-7225.0 ,765.0			
520	COM33	-7275.0 ,765.0			
521	COM34	-7331.0 ,765.0			
522	COM35	-7605.0 ,736.0			
523	COM36	-7605.0 ,680.0			
524	COM37	-7605.0 ,630.0			
525	COM38	-7605.0 ,580.0			
526	COM39	-7605.0 ,530.0			
527	COM40	-7605.0 ,480.0			
528	COM41	-7605.0 ,430.0			
529	COM42	-7605.0 ,380.0			
530	COM43	-7605.0 ,330.0			
531	COM44	-7605.0 ,280.0			
532	COM45	-7605.0 ,230.0			
533	COM46	-7605.0 ,180.0			
534	COM47	-7605.0 ,130.0			
535	COM48	-7605.0 ,80.0			
536	COM49	-7605.0 ,30.0			
537	COM50	-7605.0 ,-20.0			
538	COM51	-7605.0 ,-70.0			
539	COM52	-7605.0 ,-120.0			
540	COM53	-7605.0 ,-170.0			
541	COM54	-7605.0 ,-220.0			
542	COM55	-7605.0 ,-270.0			
543	COM56	-7605.0 ,-320.0			
544	COM57	-7605.0 ,-370.0			
545	COM58	-7605.0 ,-420.0			
546	COM59	-7605.0 ,-470.0			
547	COM60	-7605.0 ,-520.0			
548	COM61	-7605.0 ,-570.0			
549	COM62	-7605.0 ,-620.0			
550	COM63	-7605.0 ,-670.0			

5. Functional block diagram

5.1 System Block Diagram

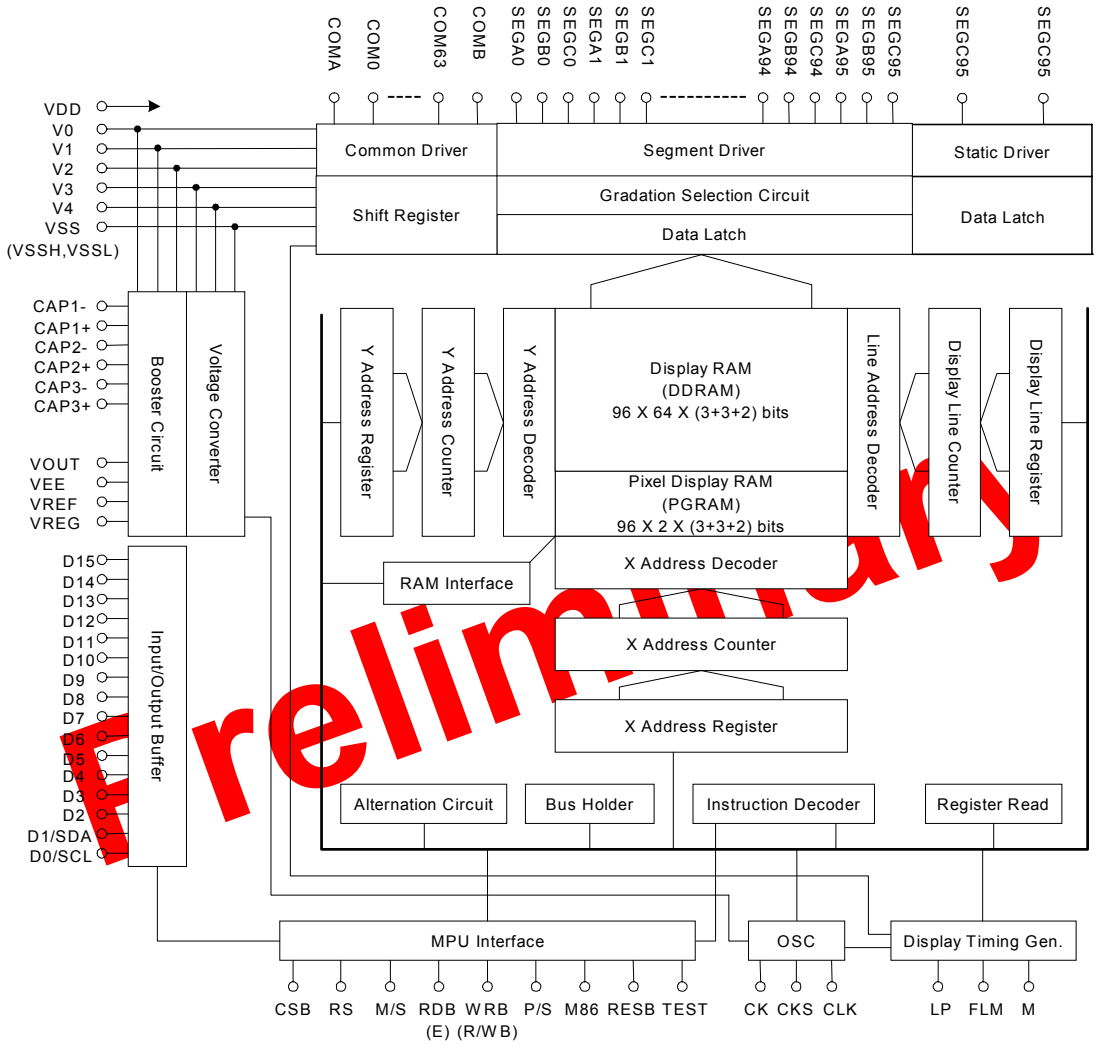


Figure 2. System Block Diagram

5.2 Power Circuit Block Diagram

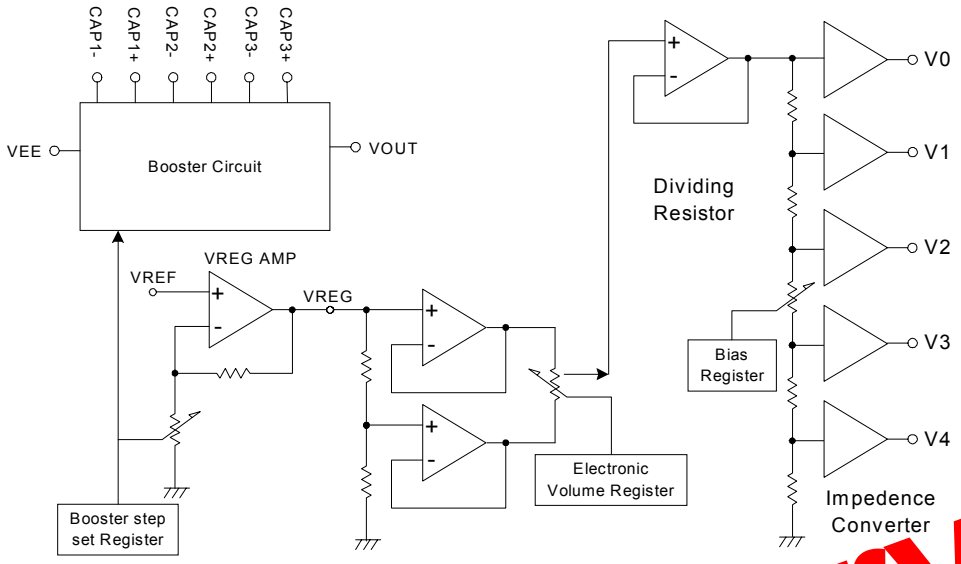


Figure 3. Power Circuit Block Diagram

6. Pin Description

6.1 Power Supply Pins

Symbol	I/O	Description
VDD	Power Supply	Power supply pin for logic circuit to +1.8 to 3.3V
VSSL	Power Supply	Ground pin for logic circuit, connect to 0V
VSSH	Power Supply	Ground pin for high voltage circuit, connected to 0V
V0 V1 V2 V3 V4	Power Supply	Bias power supply pin for LCD drive voltage When using an external power supply, convert impedance by using resistance-division of LCD drive power supply or operation amplifier before adding voltage to the pins. These voltages should have following relationship: VSS<V4<V3<V2<V1<V0 When the internal power supply circuit is active, these voltages are generated by the built-in booster and voltage converter. Then, must connect capacitor each to VSS.

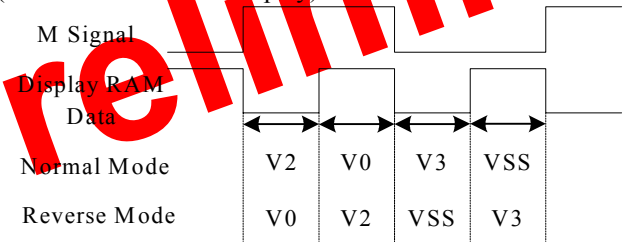
6.2 LCD Power Supply Circuit Pins

Symbol	I/O	Description
CAP1+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP1- and CAP1+.
CAP1-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP1- and CAP1+.
CAP2+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP2- and CAP2+.
CAP2	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP2- and CAP2+.
CAP3+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP3- and CAP3+.
CAP3-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP3- and CAP3+.
VREF	I	Voltage input pin for generating reference power source
VEE	Power Supply	Voltage supply pin for booster circuit. Usually the same voltage level as VDD.
VOUT	O	Output pin of boosted voltage in the built-in booster. The capacitor must be connected between this pin and VSS.
VREG	O	Output pin for regulated voltage of VREG AMP. The capacitor must be connected between this pin and VSS.

6.3 System Bus Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin.
When RESB is “L”, initialization is executed.</td></tr>
<tr><td>D0/SCL
D1/SDA
D2-D7</td><td>I/O</td><td>Data bus / Signal interface related pins.
When parallel interface is selected (P/S = “H”), The D7-D0 are 8-bits bi-directional data bus, connect to MPU data bus.
When serial interface is selected (P/S = “L”), D0 and D1 (SCL, SDA) are used as serial interface pins.
SCL: Input pin for data transfer clock
SDA: Serial data input pin
SDA data is latched at the rising edge of SCL.
Internal serial/parallel conversion into 8-bit data occurs at the rising edge of 8th clock of SCL
After completing data transferring, or when making no access, be sure to set SCL to “L”.</td></tr>
<tr><td>D8-D15</td><td>I/O</td><td>8-bit bi-directional bus. Connected to MPU data bus.
Used as data bus for upper 8-pins in the 16-bits data RAM transfer mode.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip Select input pin.
CSB = “L”: accepts access from MPU
CSB = “H”: denies access from MPU</td></tr>
<tr><td>RS</td><td>I</td><td>RAM/Register select input pin.
RS = “0”: D7-D0 are display RAM data
RS = “1”: D7-D0 are control register data</td></tr>
<tr><td>RDB
(E)</td><td>I</td><td>Read/Write control pin
Select 80-family MPU type (M86 = “L”)
The RDB is a data read signal. When RDB is “L”, D7-D0 are in an output status.
Select 68-family MPU type (M86 = “H”)
R/WB = “H”: When E is “H”, D7-D0 are in an output status.
R/WB = “L”: The data on D7-D0 are latched at falling edge of the E signal.</td></tr>
<tr><td>WRB
(R/WB)</td><td>I</td><td>Read/Write control pin
Select 80-family MPU type (M86 = “L”)
The WRB is a data write signal. The data on D7-D0 are latched at rising edge of the WRB signal.
Select 68-family MPU type (M86 = “H”)
Read/Write control input pin.
R/W = “H”: Read
R/W = “L”: Write</td></tr>
<tr><td>M86</td><td>I</td><td>MPU interface type selecting input pin.
M86 = “H”: 68-family interface
M86 = “L”: 80-family interface
Fixed at either “H” or “L”</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel/Serial interface select pin.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data identification</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>CSB</td><td>RS</td><td>D0-D7</td><td>RDB, WRB</td><td>-</td></tr>
<tr><td>L</td><td>CSB</td><td>RS</td><td>SDA</td><td>Write only</td><td>SCL</td></tr>
</table>
P/S = “H”: For parallel interface.
P/S = “L”: For serial interface. Fix D15-D5 pins are Hi-Z, RDB and WRB pins to either “H” or “L”.</td></tr>
<tr><td>TEST</td><td>I</td><td>For testing. Fix to “L”.</td></tr>
</table>

6.4 LCD Drive Circuit Signals

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>LP</td><td>I/O</td><td>The LP is latch clock I/O pin.
At the rising edge, count the display line counter. At the falling edge output the LCD drive signal. This pin use in master/slave multi-chip system
M/S = “H”: LP is output
M/S = “L”: LP is input</td></tr>
<tr><td>FLM</td><td>I/O</td><td>I/O pin for LCD display synchronous signals (first line maker).
When FLM pin is set to “H”, the display start-line address is preset. This pin use in master/slave multi-chip system. In the display line counter
M/S = “H”: FLM is output
M/S = “L”: FLM is input</td></tr>
<tr><td>M</td><td>I/O</td><td>I/O pin for alternated signals of LCD drive output.
M/S = “H”: M is output
M/S = “L”: M is input
This pin use in master/slave multi-chip system.</td></tr>
<tr><td>M/S</td><td>I</td><td>Maser/Slave mode select input pin
<table>
<tr><th>M/S</th><th>State</th><th>OSC</th><th>Power Supply Circuit</th><th>LP</th><th>FLM</th><th>M</th><th>CLK</th></tr>
<tr><td>H</td><td>Master</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Slave</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table>
Fix to “H” or “L” at this terminal.</td></tr>
<tr><td>SEGA0-A95
SEGB0-B95
SEGC0-C95</td><td>O</td><td>Segment output pins for LCD drives.
According to the data of the Display RAM data, non-lighted at “0”, lighted at “1” (Normal Mode). non-lighted at “1”, lighted at “0” (Reverse Mode) and, by a combination of M signal and display data, one signal level among V0,V2,V3 and VSS signal levels are selected.
(When Monochrome Display)
 
</td></tr>
<tr><td>COM0-
COM63</td><td>O</td><td>Common output pins for LCD drivers. By a combination of the scanning data and M signal, one signal level among V0, V1, V4 and VSS signal level is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>COMA</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
<tr><td>COMB</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
<tr><td>SCOM
SSEG</td><td>O</td><td>LCD driver output pin for static driver</td></tr>
</table>

6.5 Oscillating Circuit Pin

Symbol	I/O	Description
CKS	I	Display timing clock source select input pin. CKS = "H": Use external clock from CK pin. CKS = "L": Use internal oscillated clock. In the slave mode, fix this pin at "L". In the case of TCP, draw it as a separate terminal.
CK	I	External clock input pin for display timing. In the slave mode, fix the CK pin at "L".
CLK	I/O	I/O pin for display timing clock. To use this pin in the master/slave system. M/S = "H": Output in the master mode. M/S = "L": Input display timing clock from the master. In the monochrome mode, this signal is not output signal.

7. Functional Description

7.1 MPU Interface

7.1.1 Selection of Interface Type

The EM65567 transfers data through 8-bit parallel I/O (D7-D0), 16-bit parallel I/O (D15-D0) or serial data input (SDA, SCL). The parallel interface or serial interface can select by state of P/S pin. When select serial interface, data reading cannot be performed, only data writing can operate.

P/S	I/F Type	CSB	RS	RDB	WRB	M86	SDA	SCL	Data
H	Parallel	CSB	RS	RDB	WRB	M86	-	-	D7~D0 (D15~D0)
L	Serial	CSB	RS	-	-	-	SDA	SCL	-

7.1.2 Parallel Input

When parallel interface is selected with the P/S pin, the EM65567 allows data to be transferred in parallel to an 8-bit/16-bit MPU through the data bus. For the 8-bit/16-bit MPU, either the 80-family MPU interface or the 68-family MPU interface can be selected with the m86 pin.

M86	MPU Type	CSB	RS	RDB	WRB	Data
H	68-family MPU	CSB	RS	E	R/WB	D7~D0 (D15~D0)
L	80-family MPU	CSB	RS	RDB	WRB	D0~D7 (D15~D0)

7.1.3 Read/Write functions of Register and display RAM

The EM65567 have four read/write functions at parallel interface mode. Each read/write function select by combinations of RS, RDB and WRB signals.

RS	68-family	80-family		Function
	R/WB	RDB	WRB	
1	1	0	1	Read internal Register
1	0	1	0	Write internal Register
0	1	0	1	Read display data
0	0	1	0	Write display data

7.1.4 Serial Interface

The serial interface of EM65567 can accept inputs of SDA and SCL in the state of chip select (CSB="L"). When not in the state of chip select. The internal shift register and counter are reset in the initial condition. Serial data SDA are input sequentially in order of D7 to D0 at the rising of serial clock (SCL) and are converted into 8-bit parallel data (by serial to parallel conversion) at the rising edge of the 8th serial clock, being processed in accordance with the data. The identification whether are serial data inputs (SDA) are display data or control register data is judged by input to RS pin.

RS = "L": display RAM data

RS = "H": control register data

After completing 8-bit data transferring, or when making no access, be sure to set serial clock input (SCL) to "L". Cares of SDA and SCL signals against external noise should be taken in board wiring. To prevent transfer error due to external noise, release chip select (CSB = "H") every completion of 8-bit data transferring.

When serial interface is used, access is only made for 8-bit data transfer.

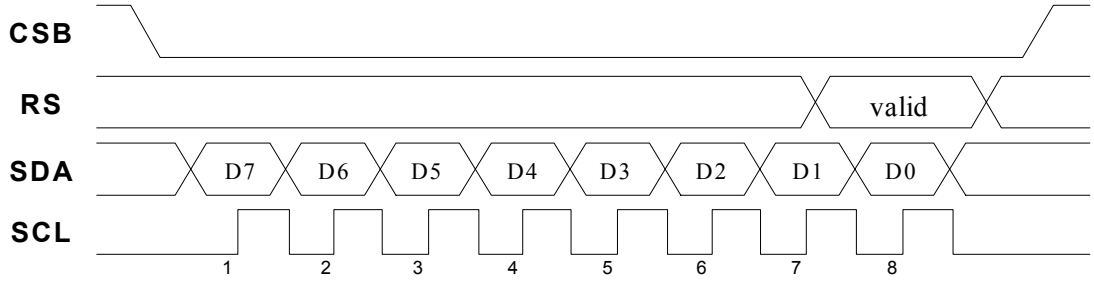


Figure 4. Serial Interface

7.2 Data write to Display RAM and Control Register

The data write to display RAM and Control Register use almost same procedure, only different setting of RS that select access object.

RS = "L": Display RAM data

RS = "H": Control register data

In the case of the 80-family MPU, the data is written at the rising edge of WRB. In the case of the 68-family MPU, the datais written at the falling edge of signal E.

Data write operation

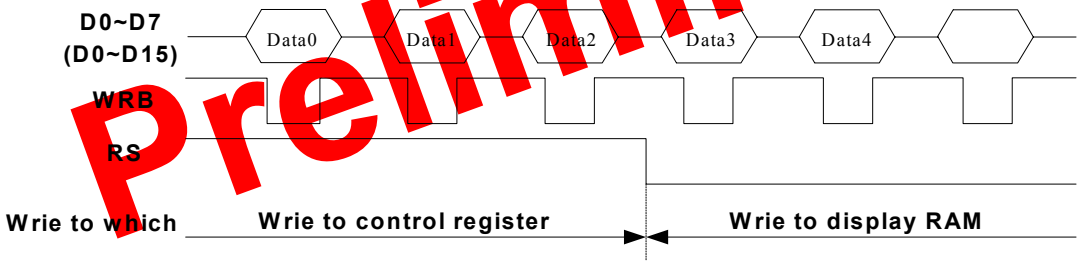


Figure 6. Data write operation

7.3 Internal Register Read

In the case of display RAM read operation, need dummy read one time. The designated address data are not output to read operation immediately after the address set to AX or AY register, but are output when the second data read. Dummy read is always required one time after address set and write cycle.

Read display RAM operation

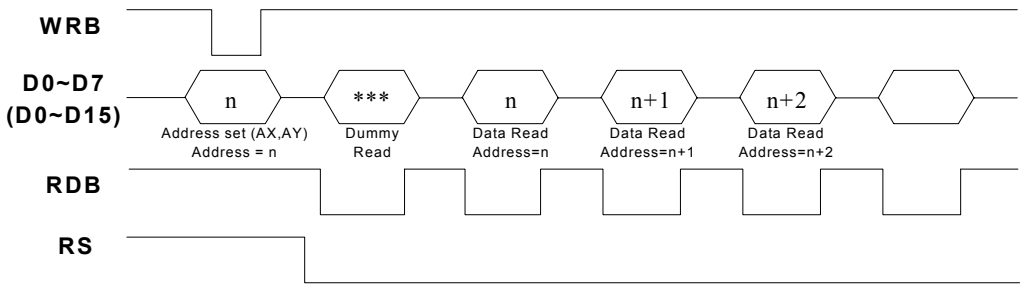


Figure 7. Read display RAM operation

The EM65567 can be read the control registers, in case of control register read operation, data bus upper nibble (D3-D0) use for register address (0 to FH). In maximum, 16 registers can access directly. But number of register is more than 16 registers. Therefore, EM65567 has register bank control. The RE register is set bank number to access. And the RE address is 0FH, in any bank can access RE register. It is need 4-steps to read the specific register in maximum case.

(1) Write 04H to RE register for access to RA register.
(2) Writes specific register address to RA register.
(3) Write specific register bank to RE register.
(4) Read specific register contents.

Register read operation

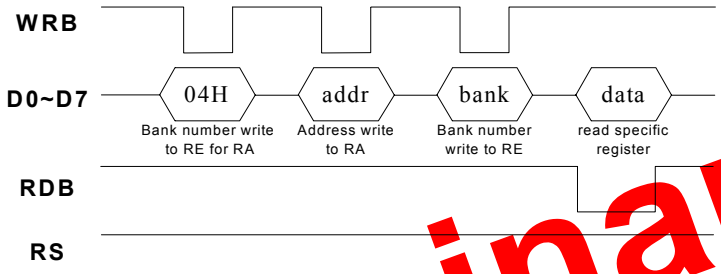


Figure 8. Register read operation

7.4 16-bit Data Access to Display RAM

The EM65567 correspond to 8-bits and 16-bits bus size access.

The data bus size can select by WLS register.

WLS = "0": 8-bits bus size

WLS = "1": 16-bits bus size

In the 16-bits access mode, access for control register use low-byte data bus (D7~D0). Then high byte data bus (D15~D8) are not used in internal circuit. When read control register using 16-bits bus. Register values output to D3-D0 and D15-D4 output "H". 16-bit access is only effective for access to the display RAM.

7.5 Display Start Address Register

This register determines the Y-address of the display RAM corresponding to the display start line. The display RAM data that addressed Display Start Address register output to common driver start line. The actual common start line of LCD panel depend on Display Start Common register and SHIFT bit of Display Control register. The register are preset every timing of FLM signal variation in the display line counter. The line counter counts up being synchronized with LP input and generates line addresses which read out sequentially 288 bits data from display RAM to LCD drive circuit.

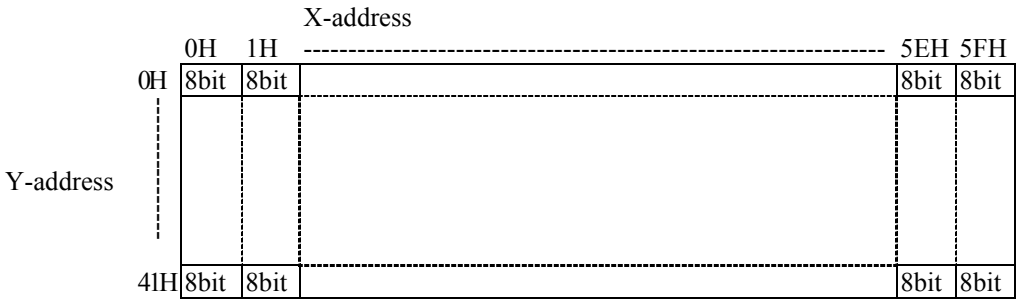
7.6 Addressing of Display RAM

The EM65567 has built-in bit mapped display RAM. The display RAM consists of 768 bits (8 bits*96) in the X-direction and 66 bits in the Y-direction. In the gradation display mode, the EM65567 provides segment driver output for 8-gradation display using 3 bits and that for 4-gradation display using 2 bits. The three outputs of the segment driver can be used for one pixel of RGB. When connected to an STN color LCD panel, the EM65567 can display 96*66 pixels with 256 colors (8

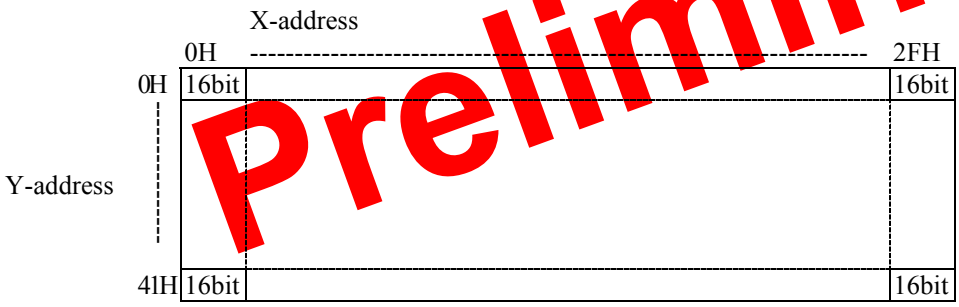
gradation * 8 gradation * 4 gradation). The address area in the X-direction depends on the access bus size. When use 8-bits bus size, can access 00H to 5FH address. When use 16-bits bus size, can access 00H to 2FH address. In the X-direction, X Address register use to access; and in the Y-direction, Y Address register use to access. Do not specify any address outside the effective address area in each access mode because it is not permitted.

In Gradation Display Mode (MON="0")

8-bits bus size access



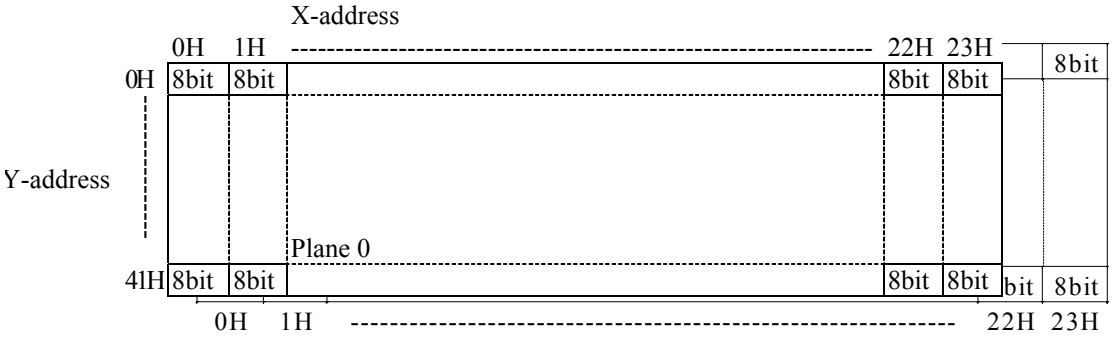
16-bits bus size access



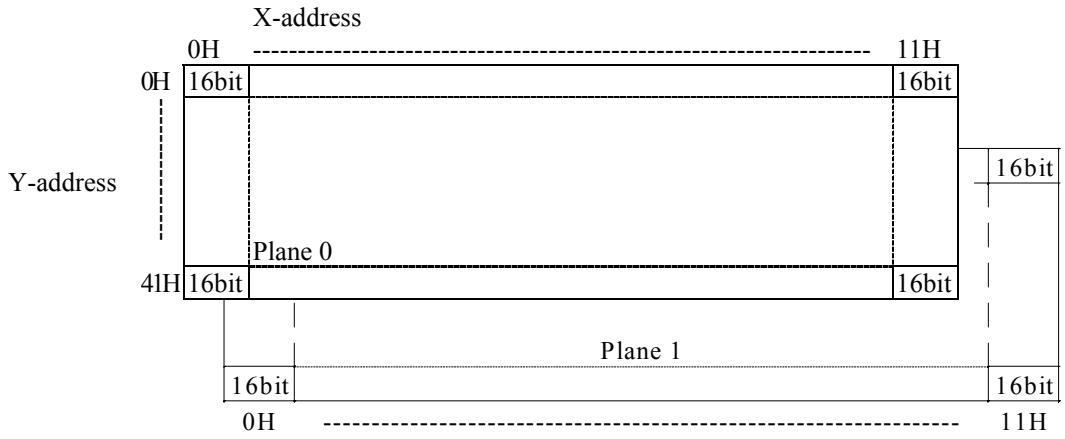
In the monochrome display mode, can access 288*66dots size two screens (plane 0/plane 1). The selection of either plane 0 or 1 to access is made by the plane selection register (PSEL). The address area in the X-direction depends on the access bus size. When use 8-bits bus size, can access 00H to 23H address. When use 16-bits bus size, can access 00H to 11H address.

In Monochrome Display Mode (MON="1")

8-bits bus size access



16-bits bus size access



The addresses, X Address and Y Address are possible to be set up so that they can increment automatically with the address control register. The increment is made every time display RAM is read or written from MPU. In the Y-direction, 288 bits of data are read out to the display data latch circuit by internal operation when the LP rises in a one-line cycle. They are output from the display data latch circuit when the LP fails. When FLM signals being output in one frame cycle are at "H", the values in the display starting line register are preset in the line counter and the line counter counts up at the falling of LP signals. The display line address counter is synchronized with each timing signal of the LCD system to operate and is independent of address counters X and Y.

7.7 Display RAM Data and LCD (only monochrome mode)

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are set up as follows.

Normal display (REV=0): RAM data = "0" not lighted
RAM data = "1" lighted

Reverse display (REV=1): RAM data = "0" lighted
RAM data = "1" not lighted

7.8 Segment Display Output Order/Reverse Set up

The order of display output, SEGA0, SEGB0, SEGC0 to SEGA95, SEGB95, and SEGC95 can be reversed. If REF control bit set to "1", display by reversing access to display RAM from MPU by using REF register, lessen the limitation in placing IC when assembling an LCD panel module.

7.9 Relationship between Display RAM and Address

The Display RAM block diagram shows in the figure below:

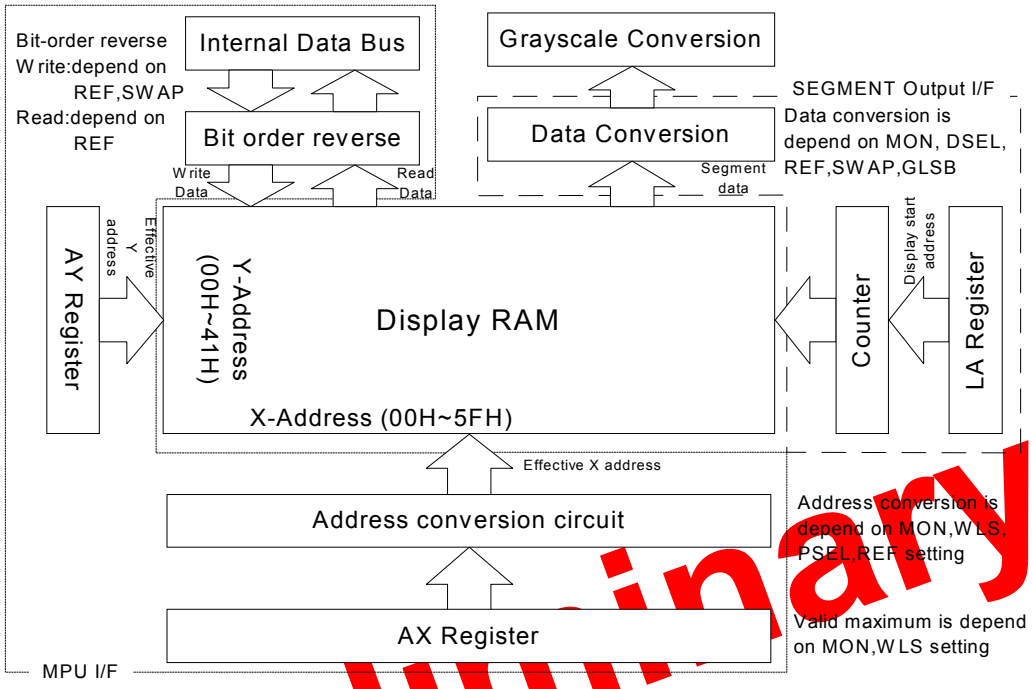
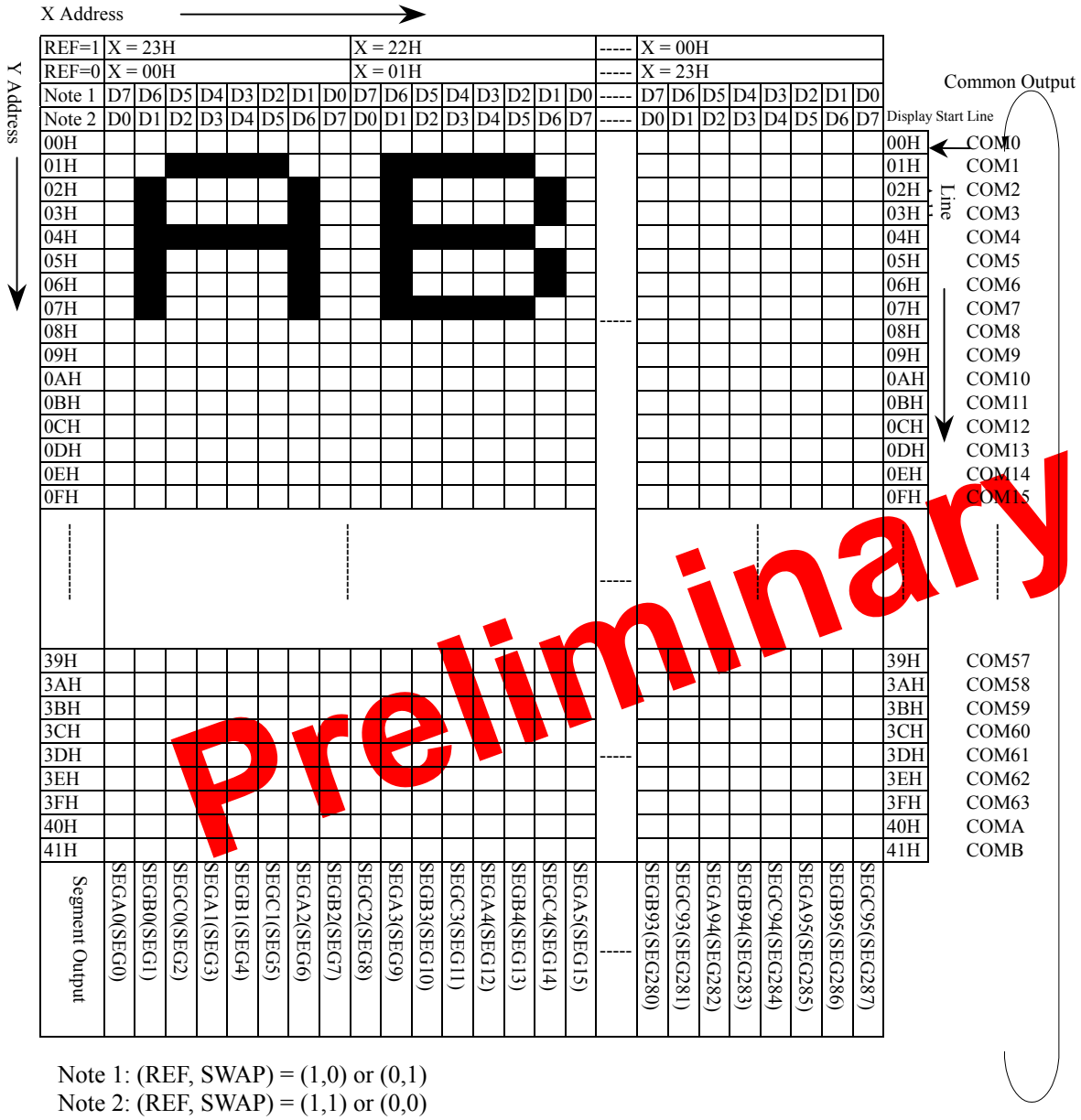


Figure 10. The Display RAM block diagram

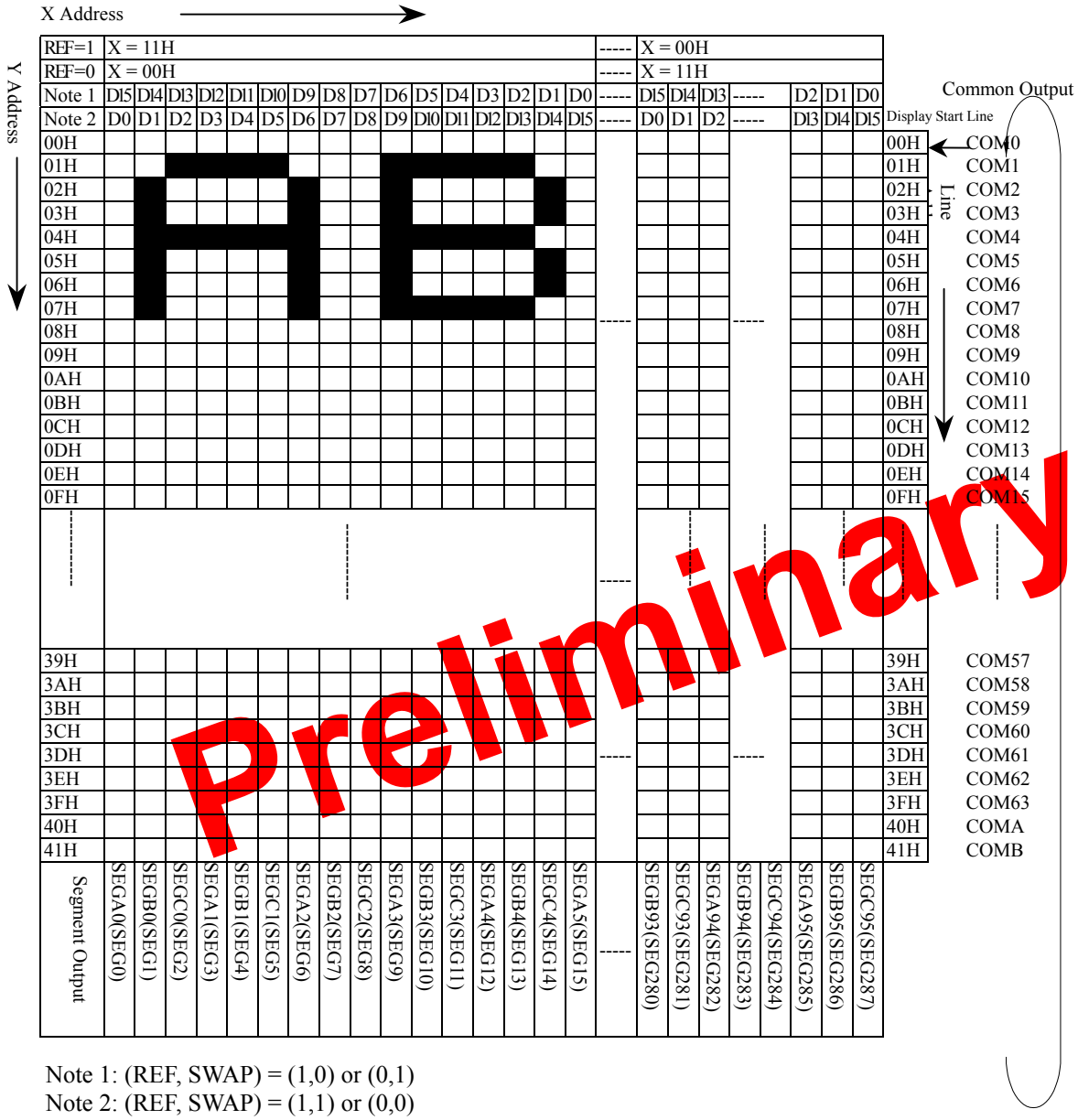
The EM65567 execute address conversion that depends on control register setting. In case of auto increment mode, usually AX register is added one. For instance when REF and AXI are both “1”, AX register is added one, but effective X address seems decrement because of address conversion. The effective Y address use AY register values as it is.

(1) Monochrome mode, 8-bits Access mode, Display Start Address = "00H" and Plane0 or Plane1 displayed.



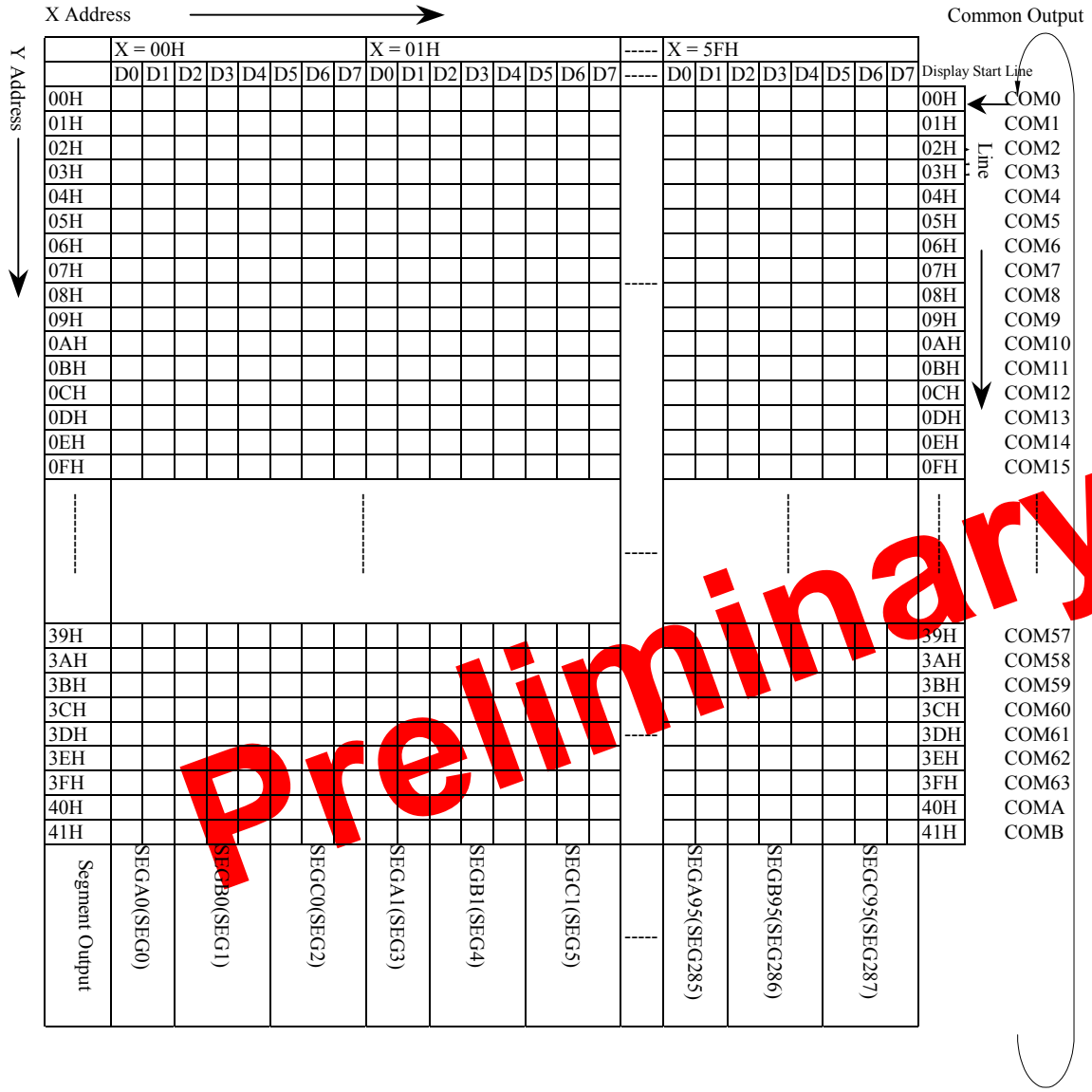
Note 1: (REF, SWAP) = (1,0) or (0,1)
Note 2: (REF, SWAP) = (1,1) or (0,0)

(2) Monochrome mode, 16-bits Access mode, Display Start Address = “00H” and Plane0 or Plane1 displayed.

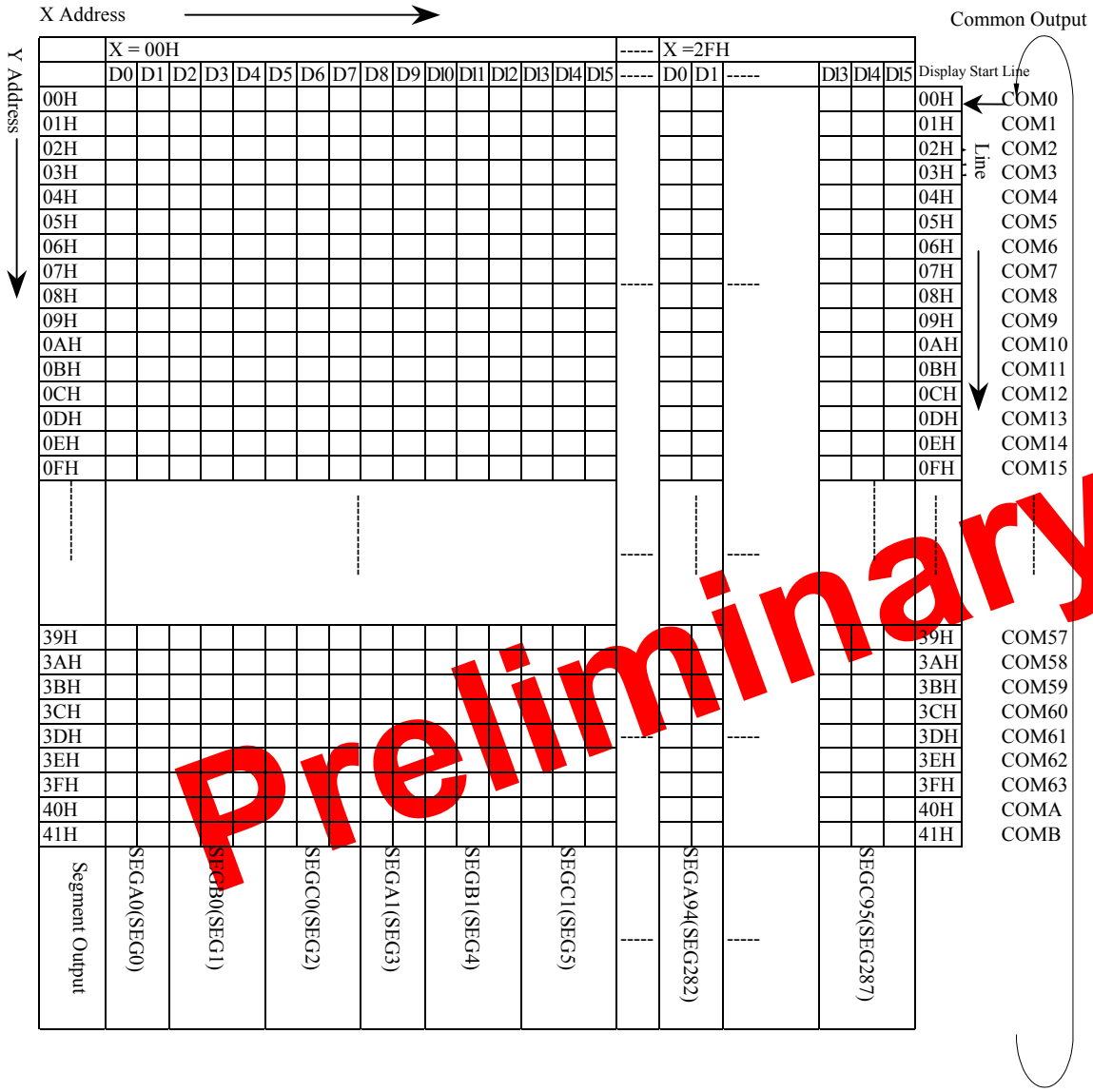


Note 1: (REF, SWAP) = (1,0) or (0,1)
Note 2: (REF, SWAP) = (1,1) or (0,0)

(3) Gradation mode, 8 bits access mode, (REF, SWAP) = (0,0)

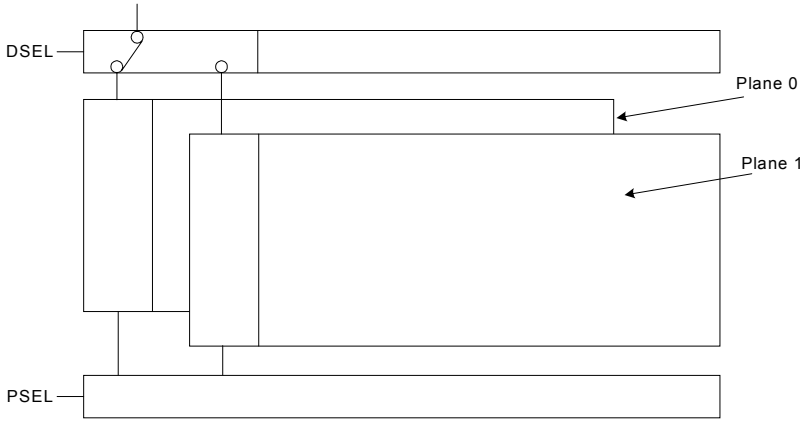


(4) Gradation mode, 16 bits access mode, (REF, SWAP) = (0,0)



7.10 Monochrome Two-Plane Display

When the gradation display is not necessary, the monochrome display may be selected. In this case, display RAM for gradation are can be used to select either of two planes for display. When data is written to the memory, the plane 0 or 1 is selected with the PSEL bit. The DSEL control bit select plane for display, data can be written to the other plane, and when the write has been completed, the displayed plane can be changed. In the monochrome mode (MON="1"), 00H, 01H, …23H are assigned to X-addresses on the plane 0/1. Access to each plane is changed with the PSEL bit.



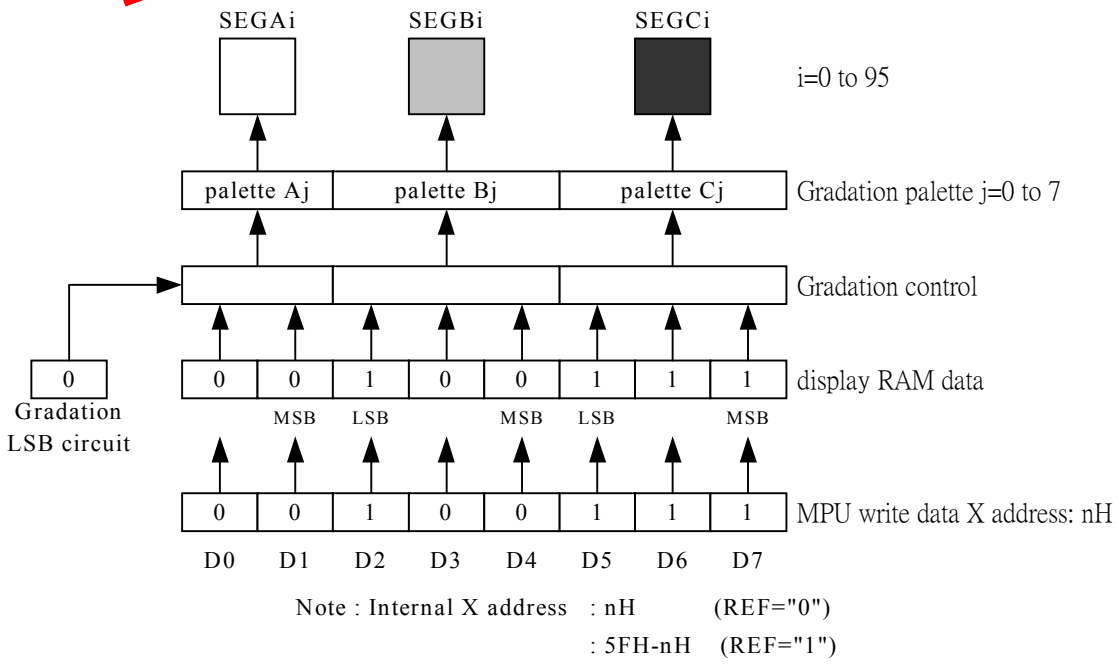
7.11 Display Data Structure and Gradation Control

For the purpose of gradation control, one pixel requires multiple bits of display RAM. The EM65567 has 3-bit or 2-bit data per output to achieve the gradation display.

The three outputs of the segment driver are used for one pixel of RGB, and the EM65567 is connected to an STN color LCD panel. It can display 96*66 pixels with 256 colors (3 bits * 3 bits * 2 bits). In this case, since the gradation display data is processed by a single access to the memory, the data can be rewritten fast and naturally.

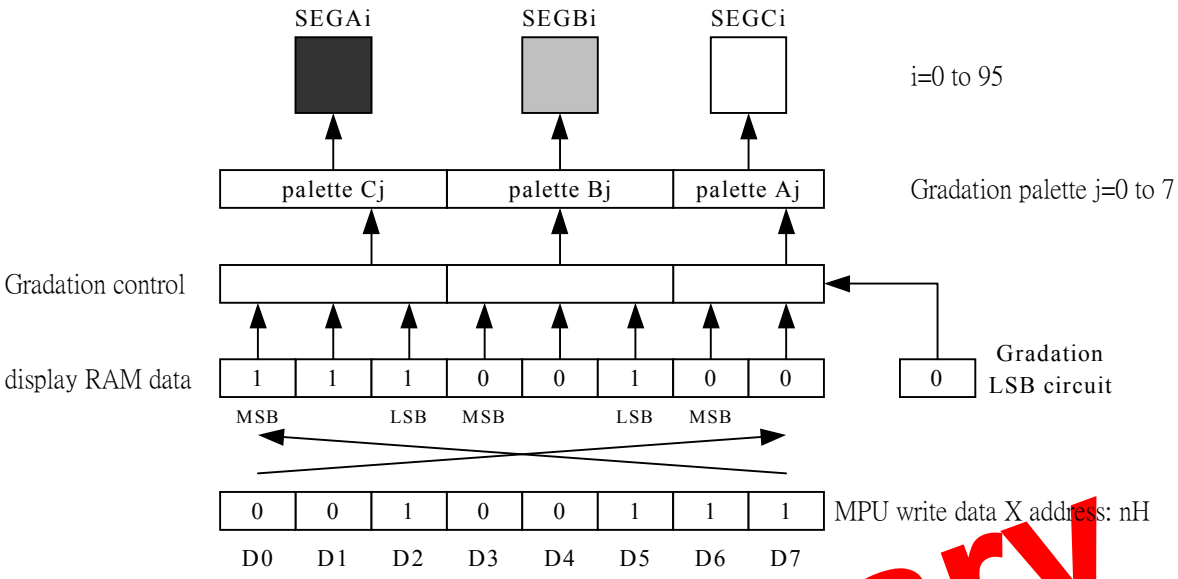
The weighting for each data bit is dependent on the status of the SWAP bit and the REF bit that is selected when data is written to the display RAM.

- (REF, SWAP)=(0,0) or (1,1)



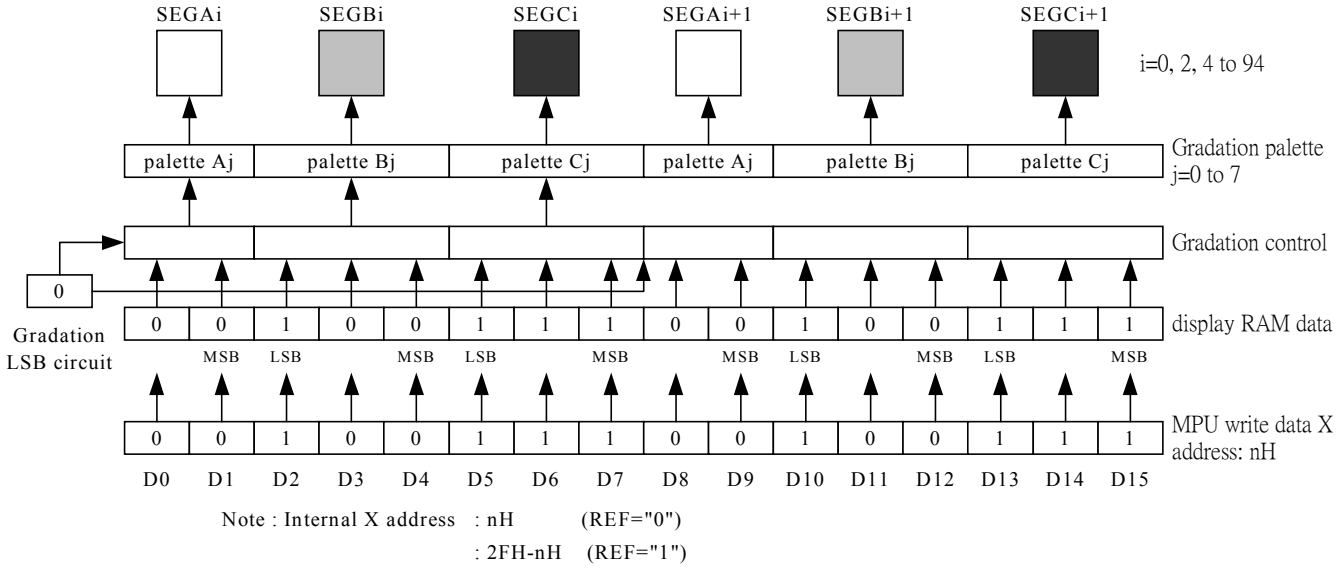
Note : Internal X address : nH (REF="0")
: 5FH-nH (REF="1")

(REF, SWAP)=(0,1) or (1,0)

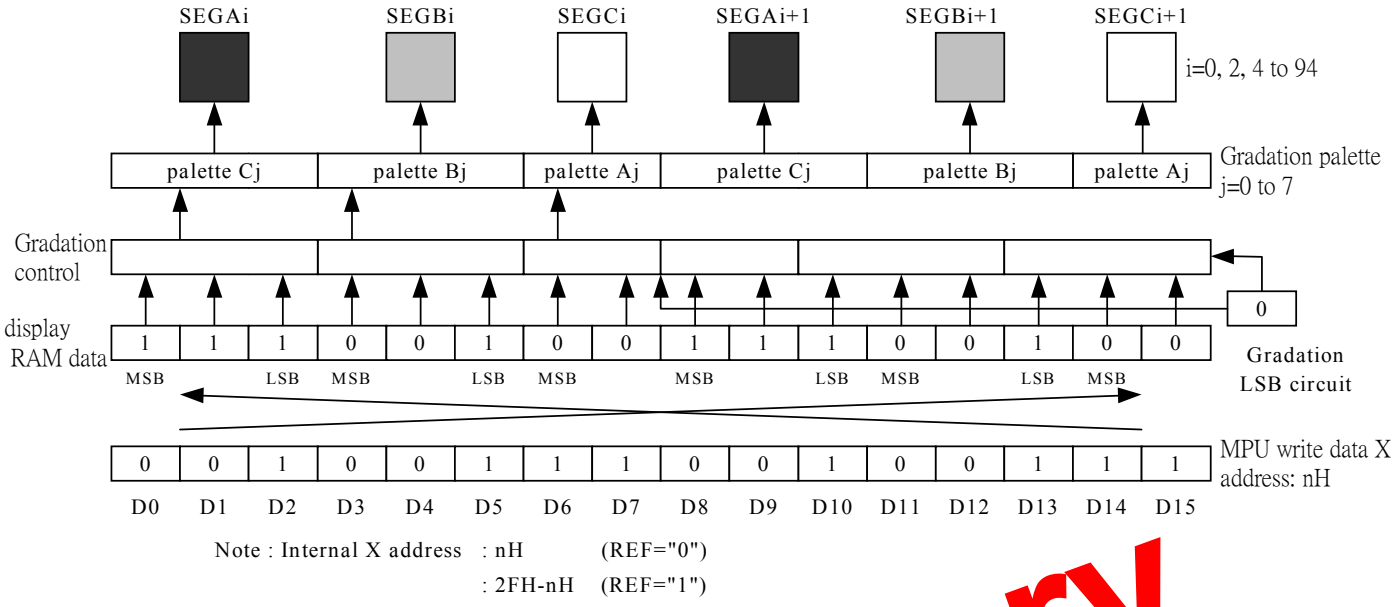


In 16-bits access, the weighting for each data bit is dependent on the status of the SWAP bit and the REF bit that is selected when data is written to the display RAM, as in the case with 8-bits access.

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)



7.12 Gradation LSB Control

In the gradation display mode, the EM65567 provides segment driver output for 8 gradation display using 3-bits and that for 4 gradation display using 2-bits. The segment driver output for the 4-gradation display uses 2-bits written to the corresponding RAM area and 1-bit supplemented by the gradation LSB circuit, and then selects 4-gradation form 8-gradation.

In the gradation display mode, the segment driver output for the 4-gradation display result in a gradation level of 0 regardless of the gradation LSB, when 2-bits of data on the display RAM are “00”. When 2-bits of data on the display RAM is “11”, a gradation level of 7/7 is selected regardless of the bit information of the gradation LS8.The other gradation levels are selected depending on 2-bits of data on the display RAM and the gradation LSB bits.

One bit of data is supplemented by setting the gradation LSB register (GLSB).

The Gradation LSB control bit applied to all 4-gradation segment drivers.

Gradation LSB = “0”: Selects 0 as the LSB information on the RAM for 4-gradation segment drivers.

Gradation LSB = “1”: Selects 1 as the LSB information on the RAM for 4-gradation segment drivers.

7.13Gradation Palette

The EM65567 has two gradation display modes, the gradation fixed display mode and the gradation variable display mode. Select either of the two modes using the gradation display mode register.

PWM = “0”: Selects the variable display mode using 8 gradation selected from 32 gradation.

PWM = “1”: Selects the fixed display mode using specific 8 gradation.

To select the best gradation level suited to the LCD panel, use the gradation palette register among the 32-level gradation palettes in the gradation variable display mode. The segment driver output is set up by the selected 8-levels of gradation palettes.

The gradation palette register provides three registers for the SEGAi (0-95) group, SEGBi (0-95) group, and SEGCi (0-95)

group of segment driver outputs [palettes Aj, Bj, and Cj (j = 0-7)]. Each register consists of a 5-bit register, selecting 8-gradations from the pattern for 32-gradations.

Initial values on gradation palette register

[Three groups of palettes Aj, Bj, and Cj (j = 0-7) are available]

(MSB)RAM data(LSB)			Register Name	Initial value
0	0	0	Gradation Palette 0	0 0 0 0 0
0	0	1	Gradation Palette 1	0 0 1 0 1
0	1	0	Gradation Palette 2	0 1 0 1 0
0	1	1	Gradation Palette 3	0 1 1 1 0
1	0	0	Gradation Palette 4	1 0 0 0 1
1	0	1	Gradation Palette 5	1 0 1 0 1
1	1	0	Gradation Palette 6	1 1 0 1 0
1	1	1	Gradation Palette 7	1 1 1 1 1

Gradation level table (PWM = "0", variable mode)

[Three groups of palettes Aj, Bj, and Cj (j = 0-7) are available

Palette	Gradation level	Remarks	Palette	Gradaton level	Remarks
0 0 0 0	0	gradation palette0 initial valu	1 0 0 0 0	16/31	
0 0 0 0	1/31		1 0 0 0 1	17/31	gradation palette4 initial valu
0 0 0 1	2/31		1 0 0 1 0	18/31	
0 0 0 1	3/31		1 0 0 1 1	19/31	
0 0 1 0	4/31		1 0 1 0 0	20/31	
0 0 1 0	5/31	gradation palette1 initial valu	1 0 1 0 1	21/31	gradation palette5 initial valu
0 0 1 1	6/31		1 0 1 1 0	22/31	
0 0 1 1	7//31		1 0 1 1 1	23/31	
0 1 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0	9/31		1 1 0 0 1	25/31	
0 1 0 1	10/31	gradation palette2 initial valu	1 1 0 1 0	26/31	gradation palette6 initial valu
0 1 0 1	11/31		1 1 0 1 1	27/31	
0 1 1 0	12/31		1 1 1 0 0	28/31	
0 1 1 0	13/31		1 1 1 0 1	29/31	
0 1 1 1	14/31	gradation palette3 initial valu	1 1 1 1 0	30/31	
0 1 1 1	15/31		1 1 1 1 1	31/31	gradation palette7 initial valu

Gradation level table (PWM = "1", fixed mode)

(MSB)RAM data(LSB)			Gradation level
0	0	0	0
0	0	1	1/7
0	1	0	2/7
0	1	1	3/7
1	0	0	4/7
1	0	1	5/7
1	1	0	6/7
1	1	1	7/7

RAM Data		GLSB	Gradation level
0	0	※	0
0	1	0	2/7
0	1	1	3/7
1	0	0	4/7
1	0	1	5/7
1	1	※	7/7

※ : Don't Care

7.14 Display Timing Circuit

The display timing circuit generates internal signals and timing pulses (LP, FLM, M and CLK) by clock. It can select external input (CK) or internal oscillation.

By setting up Master/Slave mode (M/S), the state of timing pulse pins and the timing generator changes.

M/S Pin	Mode	LP Pin	M Pin	FLM Pin	CLK Pin	State of timing generator
L	Slave	Input	Input	Input	Input	LP,FLM,M generation stop
H	Master	Output	Output	Output	Output	Operation state

Display timing pulse pins and Generator State

7.15 Signal Generation to Display Line Counter, and Display Data Latching Circuit

Both the clock to the line counter and clock to display data latching circuit from the display clock (LP) are generated. Synchronized with the display clock (LP), the line addresses of Display RAM are generated and 288-bits display data are latched to display data latching circuit to output to the LCD drive circuit (Segment outputs). Read-out of the display data to the LCD drive circuit is completely independent of MPU. Therefore, MPU that has no relationship the read-out operation of the display data can access.

7.16 Generation of the Alternated Signal (M) and the Synchronous Signal (FLM)

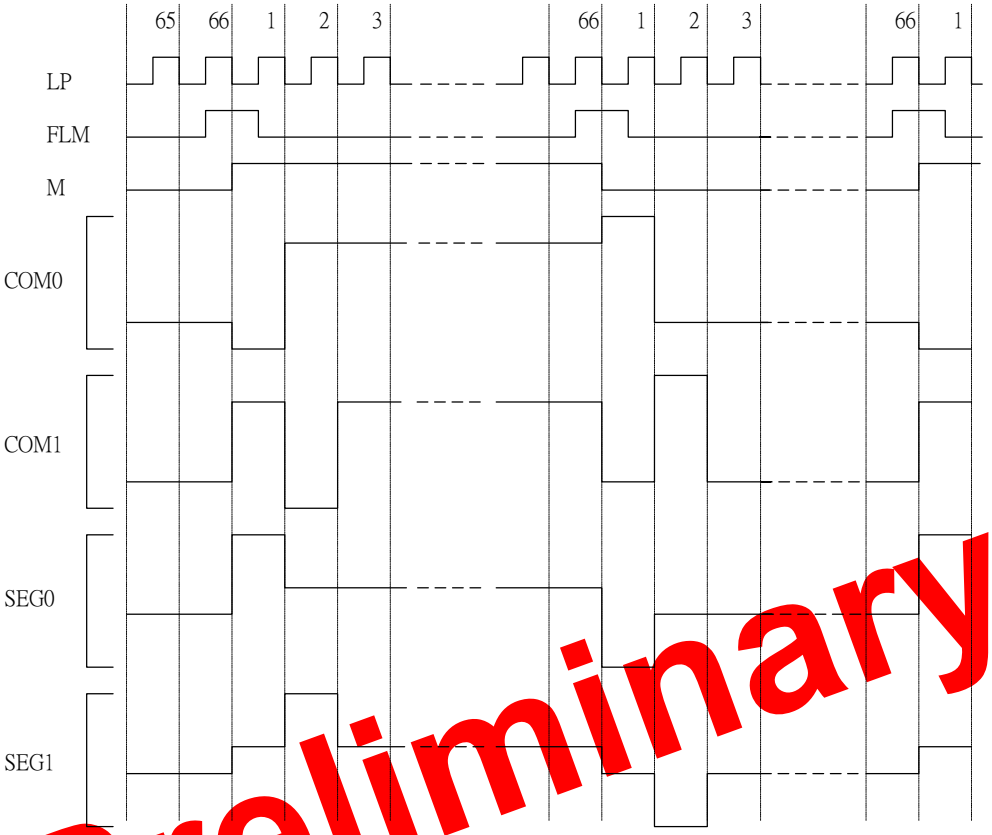
LCD alternated signal (M) and synchronous signal (FLM) are generated by the display clock (LP). The FLM generates alternated drive waveform to the LCD drive circuit. Normally, the FLM generates alternated drive waveform every frame (M-signal level is reversed every one frame). However, by setting up data (n-1) in an n-line reverse register and n-line alternated control bit (NLIN) at "1", n-line reverse waveform is generated. When the EM65567 is used in multi chip system, master chip must provide LP, FLM, and M signals for the slave chip.

7.17 Display Data Latching Circuit

Display data latching Circuit temporally latches display data that is output display data to LCD driver circuit from display RAM every one common period. Normal display/reverse display, display ON/OFF, and display all on functions are operated by controlling data in display data latch. Therefore, no data within display RAM changes.

7.18 Output Timing of LCD Driver

Display timing at Normal mode (not reverse mode), 1/66 DUTY, and on monochrome mode.



7.19 LCD Drive Circuit

This drive circuit generates four levels LCD drive voltage. The circuit has 288 segment outputs and 66 common outputs and outputs combined display data and M signal. Two of common outputs, COMA and COMB, are special outputs. The COMA and COMB outputs be not influenced by partial setting. Mainly use for display. The common drive circuit that has shift register sequentially outputs common scan signals.

7.20 Oscillating Circuit

The EM65567 has the CR oscillator. The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster.

This can use only in the master operation mode.

When in the master operation mode and external clock is used, feed the clock to CK pin.

The duty cycle of the external clock must be 50%.

The resistance ratio of CR oscillator is programmable. If change this ratio, also change frame frequency for display.

7.21 Power Supply Circuit

This circuit supplies voltages necessary to drive a LCD. The circuit consists of booster and voltage converter.

Boosted voltage from the booster is fed to the voltage converter that converts this input voltage into V0, V1, V2, V3 and V4 that are used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many

pixels. Otherwise, display quality will degrade considerably. Instead, use an external power supply. When using the external power supply, turn off the internal power supply (AMPON, DCON="00"), disconnect pins CAP1+, CAP2+, CAP2-, CAP3+, CAP3-, VOUT, VEE, VREF and VREG. Then, feed external LCD drive voltages to pins V0, V1, V2, V3 and V4. The power circuit can be control by power circuit related register. So partial function of built-in power circuit can use with external power supply.

DCON	AMPON	Booster circuit	Voltage conversion circuit	Extemal voltage input	Note
0	0	DISABLE	DISABLE	V0,V1,V2,V3 and V4 are supplied	※1
0	1	DISABLE	ENABLE	VOUT is supplied	※2
1	1	ENABLE	ENABLE	-	-

※ 1 Because the booster and voltage converter not operating, disconnect pins
CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3-, VOUT, VEE, VREG and VREF.
Apply external LCD drive voltages to corresponding pin.

※ 2 Because the booster is not operating, disconnect pins
CAP1+, CAP1-, CAP2+, CPA2-, CAP3+, CAP3-
Derive the voltage source to be supplied to the voltage converter from VOUT pin and then
Input the reference voltage at VREF pin.

7.22 Booster Circuit

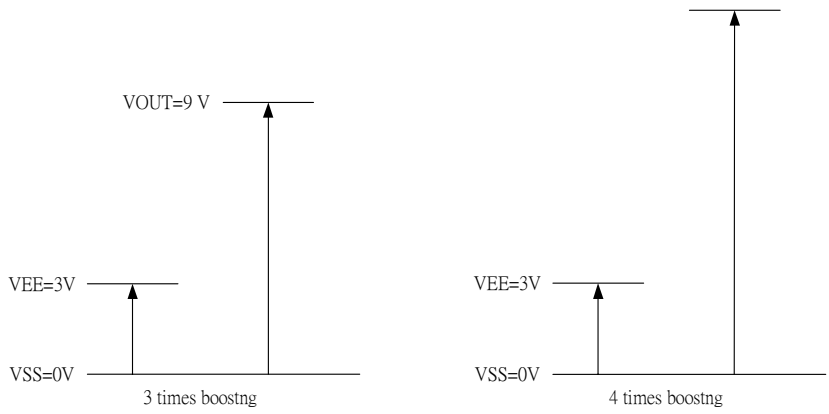
Placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3- and across VOUT and VSS boosts the voltage coming from VEE and VSS n-times and outputs the boosted voltage to VOUT pin. The twice, third, or fourth boosted voltage output to the VOUT pin by the boost step register set. The boost step registers set by the command.

(1) In case of using only twice boosted voltage, placing C1 only across CAP1+ and CAP1- and opening CAP2+, CAP2-, CAP3+, CAP3

(2) In case of using only third boosted voltage, placing C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2- and opening CAP3+, CAP3-

(3) In case of using only fourth boosted voltage, placing C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3-

When use built-in booster circuit, output voltage (VOUT) must less than recommended operating voltage (15.0 Volt). If output voltage (VOUT) over recommended operating voltage, correct work of chip can not guarantee.



7.23 Electronic volume

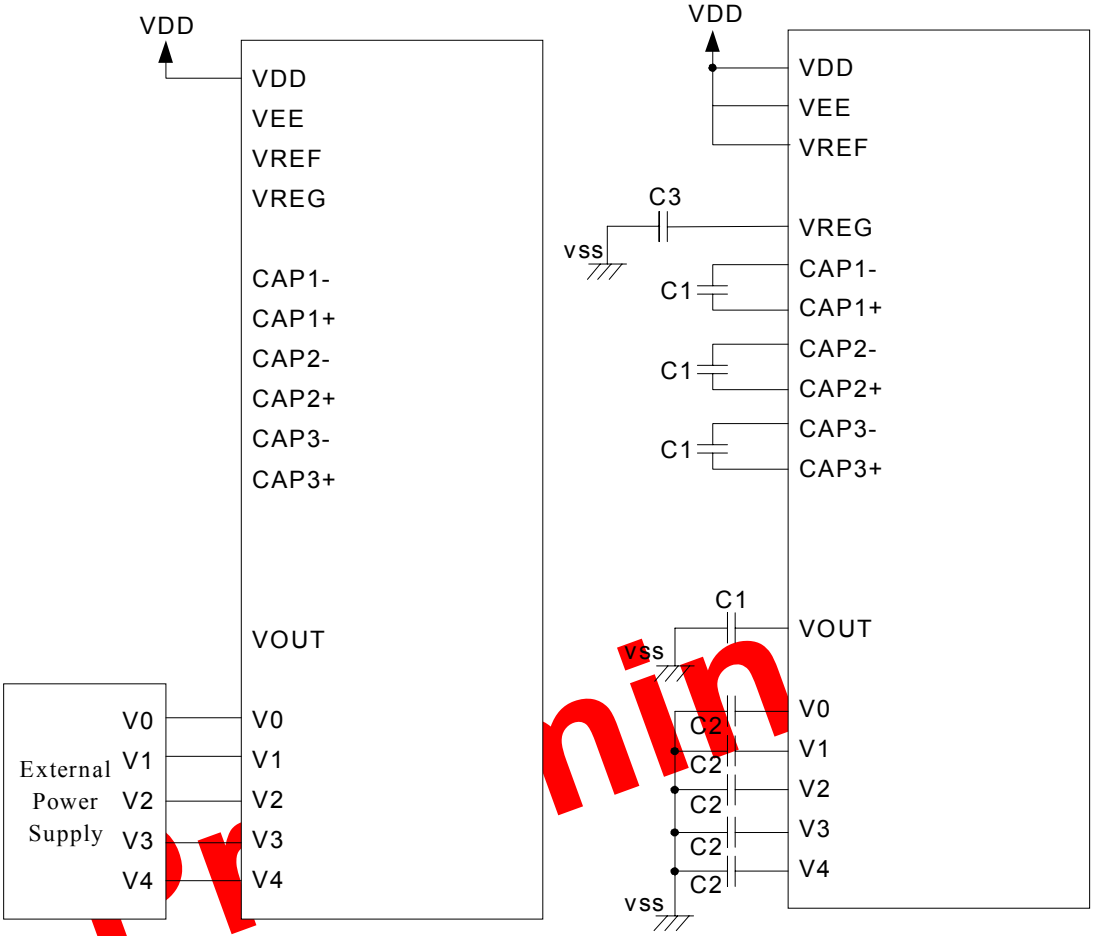
The voltage conversion circuit has built-in an electronic volume, which allows the LCD drive voltage level V0 to be controlled with DV register setting and allows the tone of LCD to be controlled. The DV registers are 7-bits, so can select 128 voltage values for the LCD drive voltage V0.

7.24 Voltage Regulator

The EM65567 has built-in reference voltage regulator, which generate the voltage amplified by input voltage from VREF pin. The generated voltage is output at the VREG pin. Even if the boosted voltage level fluctuates, VREG remains stable so far as VOUT is higher than VREG Stable power supply can be obtained using this constant voltage, even if the load fluctuates. The EM65567 uses the generated VREG level for the reference level of the electronic volume to generate LCD drive voltage. In order to stabilize the output voltage at the VREG pin, connect the capacitor C3 as appropriate by choosing its value.

7.25 LCD Drive Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V0, that is, V1, V2, V3 and V4 are obtained by dividing V0 through a resistor network. The LCD drive voltage from EM65567 is biased at 1/5, 1/6, 1/7, 1/8 or 1/9. When using the internal power supply, connect a stabilizing capacitor C2 to each of pins V0 to V4. The capacitance of C2 should be determined while observing the LCD panel to be used. When using the external power supply, apply external LCD drive voltages to V0, V1, V2, V3, V4, disconnect pins CAP1+, CAP-, CAP2+, CAP2-, CAP3+, CAP3-, VOUT, VEE, VREF and VREG. When using only the voltage conversion circuit, turn off the internal booster circuit, disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3- and VEE. Derive the voltage source to be supplied to the voltage converter from VOUT pin and then input the reference voltage to VREF pin.



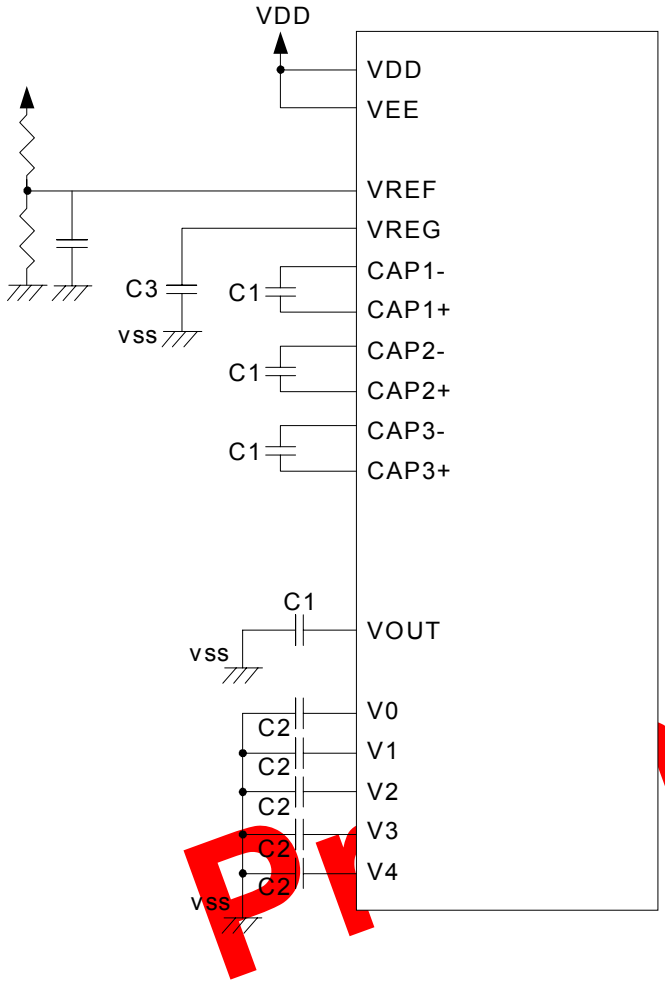
When using external power supply.

When using internal power circuit. (4 times boosting)

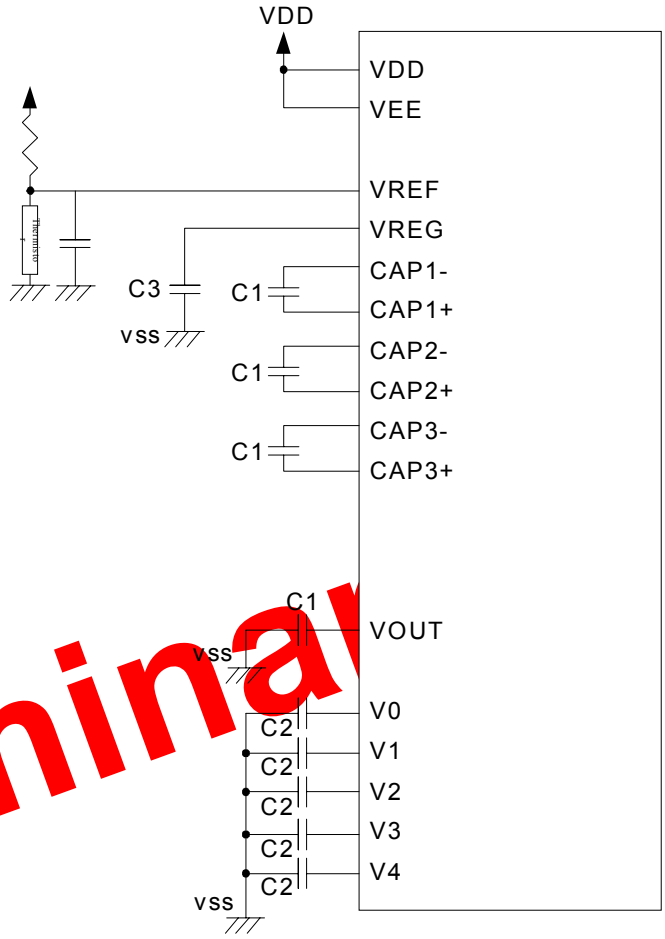
Recommended value.

C1	1.0 to 4.7 μF
C2	1.0 to 2.2 μF
C3	0.1 μF

Note: External Capacitance must be use B characteristic.



When using internal power circuit with external reference voltage input.
(4 times boosting)

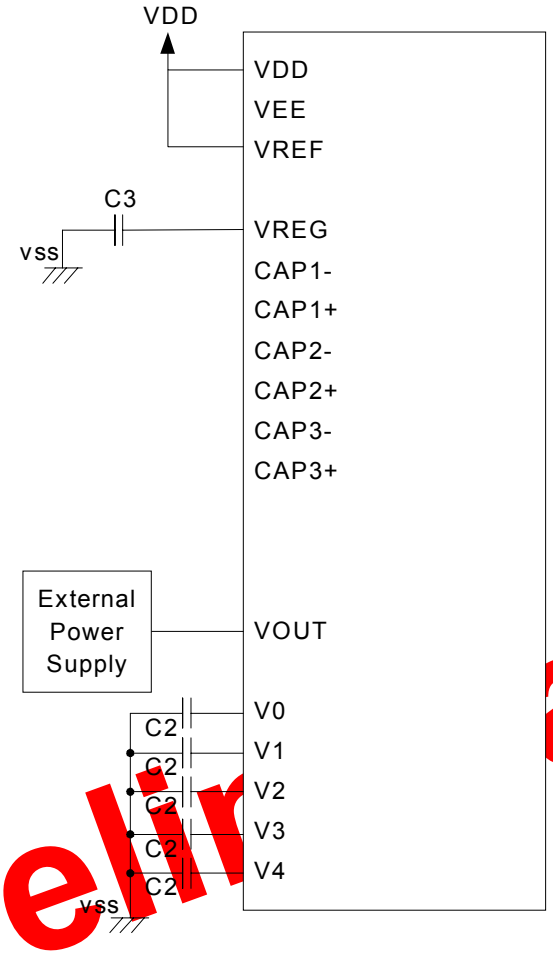


When using internal power circuit with thermistor for temperature independt.
(4 times boosting)

Recommended value.

C1	1.0 to 4.7 μF
C2	1.0 to 2.2 μF
C3	0.1 μF

Note: External Capacitance must be use B characteristic.



When using internal power circuit.

(VOUT supplied from external, no use boosting circuit)

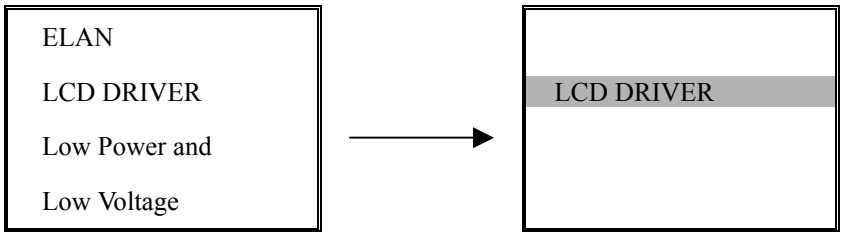
Recommended value.

C2	1.0 to 2.2 μF
C3	0.1 μf

Note: External Capacitance must be use B characteristic.

7.26 Partial Display Function

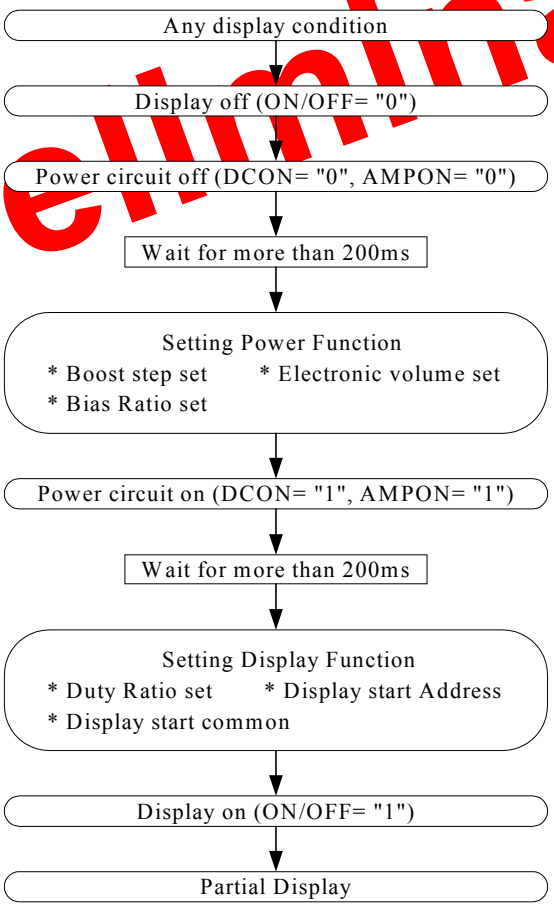
The EM65567 has the partial display function, which can display a part of graphic display area. This function is used be set lower bias ratio, lower boost step, and lower LCD drive voltage. Since setting partial display function, EM65567 provides low power consumption. Partial display function is the most suitable for clock indication or calendar indication when a portable equipment stand-by.



Normal Display Partial Display

Image of partial Display

When using the partial display function, it is necessary to keep following sequence.



Select a display duty ratio for the partial display from 1/10, 1/18, 1/26, 1/34, 1/42, 1/50 and 1/58 using the DS(LCD duty ratio) register. Set the most suitable values for LCD drive bias ratio, LCD drive voltage, electronic volume, the number of boosting steps, and others according to the actually used LCD panel and the selected duty ratio.

7.27 Discharge circuit

The EM65567 has built-in the discharge circuit, which discharges electricity from capacitors for a stability of power sources(V0~V4).

The discharge circuit is valid, while the DIS register is set to "1" or the RESB pin is set "L". When the built-in power supply is used, should be set DIS="1" after the power source is turned off (DCON, AMPON)=(0, 0). And don't turn on both the built-in power source and the external power source (V0~V4, VOUT) while DIS="1".

7.28 Initialization

The EM65567 is initialized by setting RESB pin to "L". Normally, RESB pin is initialized together with MPU by connecting to the reset pin of MPU. When power ON, be sure to make RESB="L".

Display RAM	Not fixed
X Address	00H set
Y Address	00H set
Display starting line	Set at the first line(0H)
Display ON/OFF	Display OFF
Display Normal/Reverse	Normal
Display duty	1/66
n-line alternated	every frame unit
Common shift direction	COM0→COM63, COMA, COMB
Increment mode	Increment OFF
REF mode	Normal
Data SWAP Mode	OFF
Register in electronic volume	(0,0,0,0,0,0,0)
Power Supply	OFF
Display mode	Gradation display mode
Bias ratio	1/9 bias
Gradation palette 0	(0, 0, 0, 0, 0)
Gradation palette 1	(0, 0, 1, 0, 1)
Gradation palette 2	(0, 1, 0, 1, 0)
Gradation palette 3	(0, 1, 1, 1, 0)
Gradation palette 4	(1, 0, 0, 0, 1)
Gradation palette 5	(1, 0, 1, 0, 1)
Gradation palette 6	(1, 1, 0, 1, 0)
Gradation palette 7	(1, 1, 1, 1, 1)
Gradation display mode	Variable mode
Gradation LSB	"0"
RAM access data length	8-bits mode
Discharge Register	"0"
Booster frequency	(0,0)
Static Pictograh	OFF

7.29 Precaution when Power ON and Power OFF

This LSI may be permanently damaged by high current that may flow if a voltage is supplied to the LCD driver power supply while the system power supply is floating. The detail is as follows.

(i)When using as external power supply

・ Procedure for Power ON

(1) Logic system (VDD) power ON, make reset operation.

(2) Supply external LCD drive voltage to corresponding pins (V0, V1, V2, V3 and V4)

・ Procedure for Power OFF

(1) Set HALT register to "1" or make reset operation.

(2) Cut off external LCD drive voltage.

(3) Logic system(VDD) power OFF.

Note: connect the serial resistor (50 to 100Ω) or fuse to the LCD drive power V0 or VOUT(when only use internal voltage conversion circuit) of the system as a current limiter. Moreover, set up the suitable value of the resistor in consideration of LCD display grade.

(ii)When using the built-in power supply

・ Procedure for Power ON

(1) Logic system (VDD) power ON

(2) Booster circuit system (VEE) power ON

(3) Make reset operation, booster and voltage conversion circuit enable.

If VDD and VEE voltages aren't same potential, power on logic system (VDD) first.

・ Procedure for Power OFF

(1) Set HALT register to "1" or make reset operation.

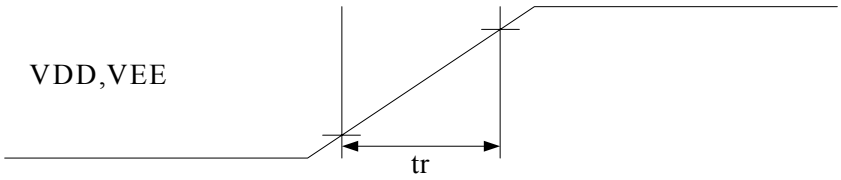
(2) Booster circuit system (VEE) power ON

(3) Logic system (VDD) power OFF.

If VDD and VEE are not same potential, cut off VEE first. After VEE, VOUT, V0, V1, V2, V3 and V4 voltages are below LCD ON voltage (threshold voltage for Liquid crystal turn on), power off logic system (VDD).

(iii)Power supply rising time

Though especially there is no constraint on the rising time of the power supply, the tr (rising time) of the following is recommended in the practical use.

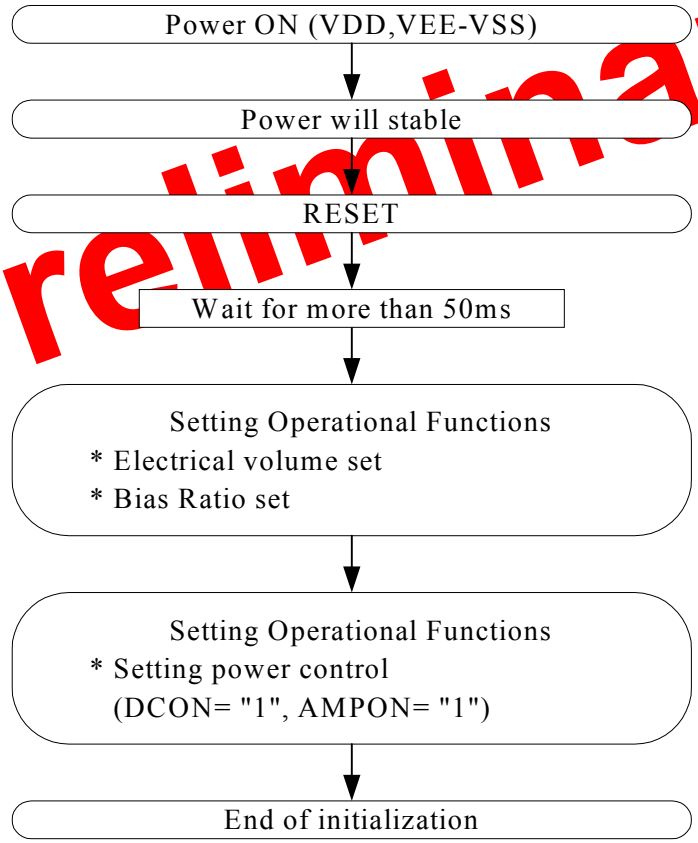


Item	Recommended rising time	Applicable Power
tr	30us ~ 10ms	VDD, VEE

Note: The rising time is the time from 10% of VDD, VEE to 90%.

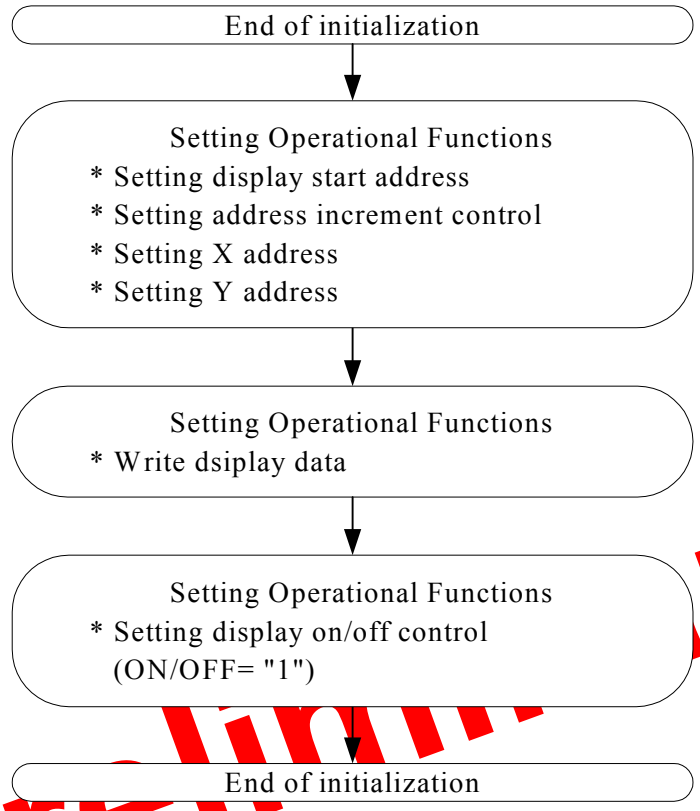
7.30 Example of Setting Registers

(1) Initialization

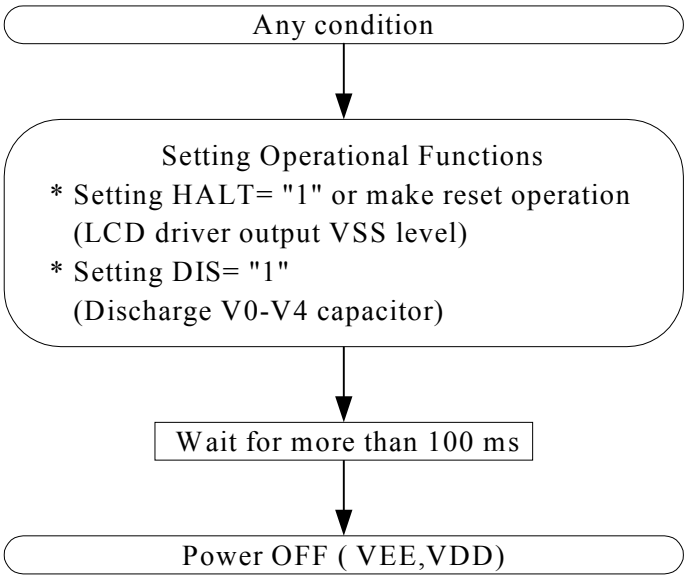


If VDD and VEE voltage are not same, connect the logic system power supply (VDD) first.

(2) Display data



(3) Power OFF



When turning off the power, set HALT command or make reset operation.

If VDD and VEE voltage are not same, disconnect the booster circuit power supply (VEE) first.

PROGRAM EXAMPLES Use Elan Risc II MCU assembly

```
;*************************************************************************
;       INITIALIZATION SETTING EXAMPLE OF EM65567
;*************************************************************************
WRITEOR macro   REGSEL,INSDAT       ; Write macro
        MOV      A,INSDAT           ; Write data
        OR       A,REGSEL           ; Write register address
        CALL     WRITE_LCD_1BYTE    ;Write A to LCD
        endm
EM65567_INI:
    WRITEOR #REREGISTERSET,#0b00000000          ;SET RE FLAG 000--> INSTRUCTION bank 0
    WRITEOR #POWERCONTROL,#0b00000001           ;ACL(B0) =1 initialization ON
    MOV      A,#50                              ;WAIT 50ms FOR EM65567 INITIAL SETTING
    CALL     WAIT_A_MS
    WRITEOR #BOOSTERSET,#0b00000011     ;BOOSTER x 4 (B1 ,B0 = 1 1)
    WRITEOR #POWERCONTROL,#0b00001010           ;BOOSTER CIRCUIT(B1) ON; OPAMP(B3) ON
    WRITEOR #BIASRATIOCONTROL,#0b00000000   ;BIAS =1/9 (B2,B1,B0=000)
    WRITEOR #LCDDUTYSET,#0b00000111             ;LCD Duty Set 1/66 DUTY (B2,B1,B0=111)
    WRITEOR #INCREMENTCONTROL,#0b00000011 ; X (B0) INCREMENT ; Y(B1) INCREMENT
    WRITEOR #DISPLAYSTARTLINELOWER,#0b00000000  ;SET Display Start LOWER Line=0
    WRITEOR #DISPLAYSTARTLINEUPPER,#0b00000000  ;SET Display Start UPPER Line=0
    WRITEOR #XADDRESSLOWER,#0b00000000          ;SET X Add=0
    WRITEOR #XADDRESSUPPER,#0b00000000
    WRITEOR #YADDRESSLOWER,#0b00000000          ;SET Y Add=0
    WRITEOR #YADDRESSUPPER,#0b00000000
    WRITEOR #DISPLAYCONTROL1,#0b00001000    ;DISPLAY(B0) OFF ; SHIFT(B3) = '1'
    WRITEOR #DISPLAYCONTROL2,#0b00000010    ;SWAP(B1) = '1'
    WRITEOR #REREGISTERSET,#0b00000100 ;SET RE FLAG 100--> INSTRUCTION bank 4
    WRITEOR #ELECTRONICVOLUMEUPPER,#0b00000111      ;SET ELECTRONIC UPPER TO MAX 0111
    WRITEOR #ELECTRONICVOLUMELOWER,#0b00001111      ;SET ELECTRONIC LOWER TO MAX 1111
    WRITEOR #COMMONSTARTLINESET,#0b00000100         ;SET COMMON START FROM COM 32 B2='1'
    WRITEOR #STATICPICTGRAPHCONTROL,#0b00000000 ;Static Pictograph Control =000
    WRITEOR #DISPLAYSELECTCONTROL,#0b00001000   ;PWM (B3)=1 8-gradation fixed display
    WRITEOR #RAMDATALENGTHSET,#0b00000000       ;WLS=0(B0) 8-BIT WIDTH MODE
    WRITEOR #DISCHARGECONTROL,#0b00000010       ;Discharge(B0) off; High power mode(B1) off
    WRITEOR #REREGISTERSET,#0b00000000          ;SET RE FLAG 000--> INSTRUCTION bank 0
    RET
```

```
;*************************************************************************
;       WRITE DISPLAY_PICTURE DATA INTO DISPLAY DATA RAM OF EM65567
;*************************************************************************
DATA_WRITE_65567:
      BS        REG_PORTB,F_LCD_A0          ; LCD RS = 1 INSTRUCTION OUTPUT
      WRITEOR #XADDRESSLOWER,#0b00000000                ;SET X Add=0
      WRITEOR #XADDRESSUPPER,#0b00000000
      WRITEOR #YADDRESSLOWER,#0b00000000                ;SET Y Add=0
      WRITEOR #YADDRESSUPPER,#0b00000000
      MOV       A,#LINE_Y_MAX                   ;COMMON = 3FH (63)
      MOV       DRAMY,A
DATA_W1:
      MOV       A,#LINE_X_MAX             ;SEGMENT = 5fh (95)
      MOV       DRAMX,A
      BC        REG_PORTB,F_LCD_A0          ;SET LCD RS=0 DATA READ/WRITE
DATA_W2:
      TBRD      01,REG_ACC                ;WRITE LCD SCREEN FROM DATA INDEX
      CALL      WRITE_LCD_1BYTE
      DEC       DRAMX
      JBS       REG_STATUS,F_C,DATA_W2
      DEC       DRAMY
      JBS       REG_STATUS,F_C,DATA_W1
      BS        REG_PORTB,F_LCD_A0        ;LCD RS = 1 INSTRUCTION OUTPUT
      RET
;*************************************************************************
;       WRITE ONE BYTE DATA INTO DDRAM (PARALLEL MODE 80 SERIES)
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION WRITE
WRITE_LCD_1BYTE:
        JBS       REG_DCRG,F_LAHEN,WRITE_LCD_1BYTE_1      ;CHECK REG_DCRG LAHEN BIT=1 OR NOT
        BC        REG_PORTC,F_LCD_WR                      ;SET /WR=0 ENABLE WRITE
        MOV       REG_DATA,A                              ;MOVE A==> PORT_G
        NOP                                               ;Write low pulse( Wait 2 instruction cycles)
        NOP
        BS        REG_PORTC,F_LCD_WR                      ;SET /WR=1 DISABLE WRITE
        NOP
        NOP
```

```
        NOP
        NOP
        RET
WRITE_LCD_1BYTE_1:
        MOV     REG_DATA,A                      ;MOVE A==> PORT_G
        RET

;*************************************************************************
;
;       READ ONE BYTE DATA INTO DDRAM (PARALLEL MODE 80 SERIES)
;
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION READ
READ_LCD_1BYTE:
        BC      REG_PORTB,F_LCD_RD              ;SET /RD=0 ENABLE READ
        NOP
        NOP
        MOV     A,REG_DATA                      ;MOVE PORT_G ==> A
        NOP
        BS      REG_PORTB,F_LCD_RD              ;SET /RD=1 DISABLE READ
        NOP
        RET
```

8. Control Register

8.1 control register

Control Register Table (Bank 0)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data write	0	0	0	1	0/1	0/1	0/1	Write Data								Write to Display RAM
Display Data read	0	0	1	0	0/1	0/1	0/1	Read Data								Read from Display RAM
Internal Register read	0	1	1	0	0/1	0/1	0/1	*	*	*	*	Read Data				Read out Internal Register
X Address (Lower nibble) [0H]	0	1	0	1	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
X Address (Upper nibble) [1H]	0	1	0	1	0	0	0	0	0	0	1	*	AX6	AX5	AX4	Set of X direction Address in display RAM
Y Address (Lower nibble) [2H]	0	1	0	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Set of X direction Address in display RAM
Y Address (Upper nibble) [3H]	0	1	0	1	0	0	0	0	0	1	1	*	AY6	AY5	AY4	Set of X direction Address in display RAM
Display start address (Lower nibble) [4H]	0	1	0	1	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Set address of display RAM making common starting line display
Display start address (Upper nibble) [5H]	0	1	0	1	0	0	0	0	1	0	1	*	*	LA5	LA4	Set address of display RAM making common starting line display
n-line altemation (Lower nibble) [6H]	0	1	0	1	0	0	0	0	1	1	0	N3	N2	N1	N0	Set the number of altemated reverse line
n-line altemation (Upper nibble) [7H]	0	1	0	1	0	0	0	0	1	1	1	*	*	N5	N4	Set the number of altemated reverse line
Display control (1) [8H]	0	1	0	1	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF	SHIFT: Select common shift direction MON: Select Monochrome/gradation ALLON: All display ON ON/OFF: Display ON/OFF control
Display control (2) [9H]	0	1	0	1	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Display normal/reverse NLIN: n line reverse control SWAP: Display data swapping REF: Segment normal/reverse
Increment control [AH]	0	1	0	1	0	0	0	1	0	1	0	*	AIM	AYI	AXI	AIM: Select increment mode AYI: Y increment, AXI: X increment
Power control [BH]	0	1	0	1	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: Intemal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting
LCD Duty Ratio [CH]	0	1	0	1	0	0	0	1	1	0	0	*	DS2	DS1	DS0	Set LCD drive duty ratio
Booster [DH]	0	1	0	1	0	0	0	1	1	0	1	*	*	VU1	VU0	Set number of boosting step for booster circuit
Bias ratio control [EH]	0	1	0	1	0	0	0	1	1	1	0	*	B2	B1	B0	Set bias ratio for LCD driving voltage
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 1)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette A0 (Lower nibble) [0H]	0	1	0	1	0	0	1	0	0	0	0	PA03	PA02	PA01	PA00	Set the umber of Gradation Palette A0
Gradation palette A0 (Upper nibble) [1H]	0	1	0	1	0	0	1	0	0	0	1	*	*	*	PA04	Set the umber of Gradation Palette A0
Gradation palette A1 (Lower nibble) [2H]	0	1	0	1	0	0	1	0	0	1	0	PA13	PA12	PA11	PA10	Set the umber of Gradation Palette A1
Gradation palette A1 (Upper nibble) [3H]	0	1	0	1	0	0	1	0	0	1	1	*	*	*	PA14	Set the umber of Gradation Palette A1
Gradation palette A2 (Lower nibble) [4H]	0	1	0	1	0	0	1	0	1	0	0	PA23	PA22	PA21	PA20	Set the umber of Gradation Palette A2
Gradation palette A2 (Upper nibble) [5H]	0	1	0	1	0	0	1	0	1	0	1	*	*	*	PA24	Set the umber of Gradation Palette A2
Gradation palette A3 (Lower nibble) [6H]	0	1	0	1	0	0	1	0	1	1	0	PA33	PA32	PA31	PA30	Set the umber of Gradation Palette A3
Gradation palette A3 (Upper nibble) [7H]	0	1	0	1	0	0	1	0	1	1	1	*	*	*	PA34	Set the umber of Gradation Palette A3
Gradation palette A4 (Lower nibble) [8H]	0	1	0	1	0	0	1	1	0	0	0	PA43	PA42	PA41	PA40	Set the umber of Gradation Palette A4
Gradation palette A4 (Upper nibble) [9H]	0	1	0	1	0	0	1	1	0	0	1	*	*	*	PA44	Set the umber of Gradation Palette A4
Gradation palette A5 (Lower nibble) [AH]	0	1	0	1	0	0	1	1	0	1	0	PA53	PA52	PA51	PA50	Set the umber of Gradation Palette A5
Gradation palette A5 (Upper nibble) [BH]	0	1	0	1	0	0	1	1	0	1	1	*	*	*	PA54	Set the umber of Gradation Palette A5
Gradation palette A6 (Lower nibble) [CH]	0	1	0	1	0	0	1	1	1	0	0	PA63	PA62	PA61	PA60	Set the umber of Gradation Palette A6
Gradation palette A6 (Upper nibble) [DH]	0	1	0	1	0	0	1	1	1	0	1	*	*	*	PA64	Set the umber of Gradation Palette A6
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 2)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette A7 (Lower nibble) [0H]	0	1	0	1	0	1	0	0	0	0	0	PA73	PA72	PA71	PA70	Set the umber of Gradation Palette A7
Gradation palette A7 (Upper nibble) [1H]	0	1	0	1	0	1	0	0	0	0	1	*	*	*	PA74	Set the umber of Gradation Palette A7
Gradation palette B0 (Lower nibble) [2H]	0	1	0	1	0	1	0	0	0	1	0	PB03	PB02	PB01	PB00	Set the umber of Gradation Palette B0
Gradation palette B0 (Upper nibble) [3H]	0	1	0	1	0	1	0	0	0	1	1	*	*	*	PB04	Set the umber of Gradation Palette B0
Gradation palette B1 (Lower nibble) [4H]	0	1	0	1	0	1	0	0	1	0	0	PB13	PB12	PB11	PB10	Set the umber of Gradation Palette B1
Gradation palette B1 (Upper nibble) [5H]	0	1	0	1	0	1	0	0	1	0	1	*	*	*	PB14	Set the umber of Gradation Palette B1
Gradation palette B2 (Lower nibble) [6H]	0	1	0	1	0	1	0	0	1	1	0	PB23	PB22	PB21	PB20	Set the umber of Gradation Palette B2
Gradation palette B2 (Upper nibble) [7H]	0	1	0	1	0	1	0	0	1	1	1	*	*	*	PB24	Set the umber of Gradation Palette B2
Gradation palette B3 (Lower nibble) [8H]	0	1	0	1	0	1	0	1	0	0	0	PB33	PB32	PB31	PB30	Set the umber of Gradation Palette B3
Gradation palette B3 (Upper nibble) [9H]	0	1	0	1	0	1	0	1	0	0	1	*	*	*	PB34	Set the umber of Gradation Palette B3
Gradation palette B4 (Lower nibble) [AH]	0	1	0	1	0	1	0	1	0	1	0	PB43	PB42	PB41	PB40	Set the umber of Gradation Palette B4
Gradation palette B4 (Upper nibble) [BH]	0	1	0	1	0	1	0	1	0	1	1	*	*	*	PB44	Set the umber of Gradation Palette B4
Gradation palette B5 (Lower nibble) [CH]	0	1	0	1	0	1	0	1	1	0	0	PB53	PB52	PB51	PB50	Set the umber of Gradation Palette B5
Gradation palette B5 (Upper nibble) [DH]	0	1	0	1	0	1	0	1	1	0	1	*	*	*	PB54	Set the umber of Gradation Palette B5
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 3)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette B6 (Lower nibble) [0H]	0	1	0	1	0	1	1	0	0	0	0	PB63	PB62	PB61	PB60	Set the umber of Gradation Palette B6
Gradation palette B6 (Upper nibble) [1H]	0	1	0	1	0	1	1	0	0	0	1	*	*	*	PB64	Set the umber of Gradation Palette B6
Gradation palette B7 (Lower nibble) [2H]	0	1	0	1	0	1	1	0	0	1	0	PB73	PB72	PB71	PB70	Set the umber of Gradation Palette B7
Gradation palette B7 (Upper nibble) [3H]	0	1	0	1	0	1	1	0	0	1	1	*	*	*	PB74	Set the umber of Gradation Palette B7
Gradation palette C0 (Lower nibble) [4H]	0	1	0	1	0	1	1	0	1	0	0	PC03	PC02	PC01	PC00	Set the umber of Gradation Palette C0
Gradation palette C0 (Upper nibble) [5H]	0	1	0	1	0	1	1	0	1	0	1	*	*	*	PC04	Set the umber of Gradation Palette C0
Gradation palette C1 (Lower nibble) [6H]	0	1	0	1	0	1	1	0	1	1	0	PC13	PC12	PC11	PC10	Set the umber of Gradation Palette C1
Gradation palette C1 (Upper nibble) [7H]	0	1	0	1	0	1	1	0	1	1	1	*	*	*	PC14	Set the umber of Gradation Palette C1
Gradation palette C2 (Lower nibble) [8H]	0	1	0	1	0	1	1	1	0	0	0	PC23	PC22	PC21	PC20	Set the umber of Gradation Palette C2
Gradation palette C2 (Upper nibble) [9H]	0	1	0	1	0	1	1	1	0	0	1	*	*	*	PC24	Set the umber of Gradation Palette C2
Gradation palette C3 (Lower nibble) [AH]	0	1	0	1	0	1	1	1	0	1	0	PC33	PC32	PC31	PC30	Set the umber of Gradation Palette C3
Gradation palette C3 (Upper nibble) [BH]	0	1	0	1	0	1	1	1	0	1	1	*	*	*	PC34	Set the umber of Gradation Palette C3
Gradation palette C4 (Lower nibble) [CH]	0	1	0	1	0	1	1	1	1	0	0	PC43	PC42	PC41	PC40	Set the umber of Gradation Palette C4
Gradation palette C4 (Upper nibble) [DH]	0	1	0	1	0	1	1	1	1	0	1	*	*	*	PC44	Set the umber of Gradation Palette C4
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 4)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette C5 (Lower nibble) [0H]	0	1	0	1	1	0	0	0	0	0	0	PC53	PC52	PC51	PC50	Set the umber of Gradation Palette C5
Gradation palette C5 (Upper nibble) [1H]	0	1	0	1	1	0	0	0	0	0	1	*	*	*	PC54	Set the umber of Gradation Palette C5
Gradation palette C6 (Lower nibble) [2H]	0	1	0	1	1	0	0	0	0	1	0	PC63	PC62	PC61	PC60	Set the umber of Gradation Palette C6
Gradation palette C6 (Upper nibble) [3H]	0	1	0	1	1	0	0	0	0	1	1	*	*	*	PC64	Set the umber of Gradation Palette C6
Gradation palette C7 (Lower nibble) [4H]	0	1	0	1	1	0	0	0	1	0	0	PC73	PC72	PC71	PC70	Set the umber of Gradation Palette C7
Gradation palette C7 (Upper nibble) [5H]	0	1	0	1	1	0	0	0	1	0	1	*	*	*	PC74	Set the umber of Gradation Palette C7
Display start common [6H]	0	1	0	1	1	0	0	0	1	1	0	*	SC2	SC1	SC0	Set Common Driver Start Line
Static Pictgraph Control [7H]	0	1	0	1	1	0	0	0	1	1	1	*	*	SPC1	SPC0	Set Static Pictgraph Drive Mode
Display Select Control [8H]	0	1	0	1	1	0	0	1	0	0	0	PWM	GLSB	PSEL	DSEL	Select Plane(access/display) Set GLSB Bit. Select PWM Mode
RAM Data length Set [9H]	0	1	0	1	1	0	0	1	0	0	1	*	*	*	WLS	Set Data length on RAM Access 8-bit access or 16-bit access
Electronic Volume (Lower nibble) [AH]	0	1	0	1	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Set Electronic Vollume Register (lower code)
Electronic Volume (Upper nibble) [BH]	0	1	0	1	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Set Electronic Vollume Register (upper code)
Register read Control [CH]	0	1	0	1	1	0	0	1	1	0	0	RA3	RA2	RA1	RA0	Set Register Address for read
Select Rf [DH]	0	1	0	1	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Select Rf ratio of OSC circuit
Extended power control [EH]	0	1	0	1	1	0	0	1	1	1	0	BF1	BF0	HPM	DIS	DIS:Discharge capacitance of V0,V1,V2,V3,V4 Pins HPM : high power mode set BF: Set Booster frequency
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

8.2 Functions of Control Registers

The EM65567 has many control registers. In case of control register access, upper nibble of data bus (D7~D4) represent register address, lower nibble of data bus (D3~D0) represent data. The access example is shown in the following. The Pins (CSB, RS, RDB, WRB) setting are for 80-family MPU interface. Only the setting of terminal (RDB,WRB) is different, when it is accessed by the 68-fanily MPU.

(Example) X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

Register address | Data

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Pins setting | Register Bank

In the writing to the control register, it is used directly as addressing D7~D4 of the data bus. In case of register read, first set RA register for specific register address, next can read specific register. Therefore, it is need 2-step for register read. Then, specific register output to D3~D0 of data bus. Except D3~D0 of data bus are all "H". Prohibit access to undefined register address area. When RS is "L", all read/write operations are accessed to display RAM. Then data bus doesn't include register address. In case of write, D3~D0 data is written to the register designated at D7~D4 in rising edge of the WRB signal. In case of read, register can output to data bus is RDB active period. Control register and display RAM are the equal access timing.

8.2.1 Data Write to Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
Display RAM write data							

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

The Display RAM data of 8-bit are written in the designated X and Y address.

8.2.2 Data Read from Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
Display RAM read data							

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

The 8-bit contents of Display RAM designated in X. and Y address and read out.

Immediately after data are set in X and Y address, dummy read is necessary one time.

8.2.3 Internal Register Data Read

D7	D6	D5	D4	D3	D2	D1	D0
※	※	※	※	Internal Register read data			

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

※ Mark shows "Don't care"

This command is used to read data from an internal register. Before executing the command. You need to set the address and RE flag for reading data from the internal register.

8.2.4 X Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX3, AX2, AX1, AX0}= 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	※	AX6	AX5	AX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX6, AX5, AX4}= 0H, read address: 1H)

※ Mark shows "Don't care"

The AX register set to X-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 3-bit respectively. Be sure to do setting from the lower bit.

8.2.5 Y Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	AY3	AY2	AY1	AY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {AY3, AY2, AY1, AY0}=0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	※	AY6	AY5	AY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AY6, AY5, AY4}=0H, read address: 3H)

※ Mark shows "Don't care"

The AY register set to Y-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 3-bit respectively. 00H to 41H are applicable to the values for AY6 to AY0, and 42H to FFH are not permitted. The address for (AY6 to AY0) = 40H, 41H are in the display RAM area for icon display.

8.2.6 Display Start Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LA3	LA2	LA1	LA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {LA3, LA2, LA1, LA0}=0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	LA5	LA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {LA5, LA4}=0H, read address: 5H)

※ Mark shows "Don't care"

This display line address is require to designate, and the designated address becomes the display line of COM0. The display of LCD panel is indicated in the increment direction of the designated display starting address to the line address.

LA5	LA4	LA3	LA2	LA1	LA0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:						
1	1	1	1	1	1	63

8.2.7 n Line Alternated Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	N3	N2	N1	N0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {N3, N2, N1, N0}=0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	N5	N4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: { N5, N4}=0H, read address: 7H)

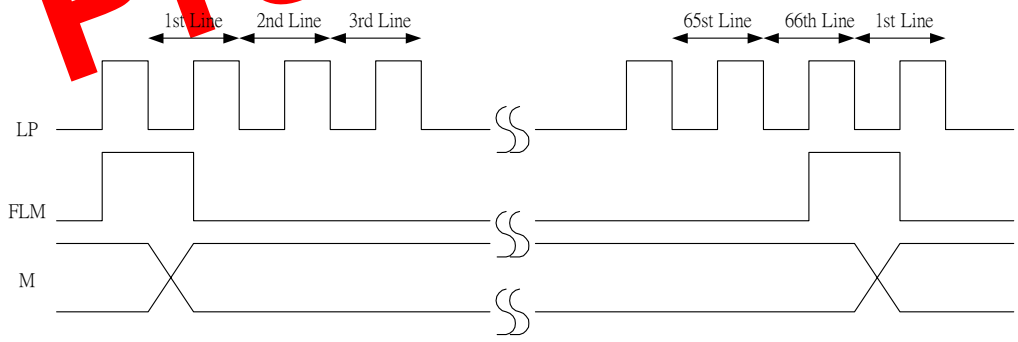
※ Mark shows "Don't care"

The reverse line number of LCD alternated drive is required to set in the register. The line number has a limit, must keeps between from 2 to 64 lines. The values set up by the alternated register become enable when NLIN control bit is "1". When NLIN control bit is "0", alternated drive waveform reverses by each frame is generated.

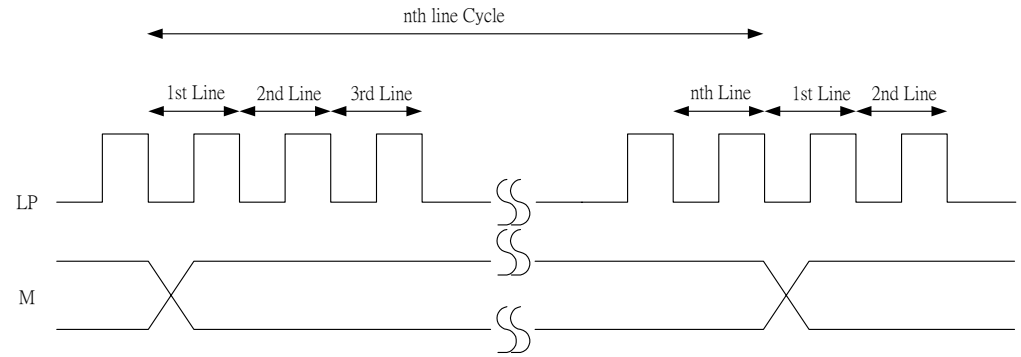
N5	N4	N3	N2	N1	N0	Line Address
0	0	0	0	0	0	-
0	0	0	0	0	1	2
		:				
1	1	1	1	1	1	64

Alternated Timing

(i) NLIN="0" (in case of 1/66 DUTY Display)



(ii) NLIN="1"



8.2.8 Display Control (1) Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {SHIFT, MON, ALLON, ON/OFF}=0H, read address: 8H)

Various control of display is set up.

ON/OFF

To control ON/OFF of display

ON/OFF = “0”: Display OFF

ON/OFF = “1”: Display ON

ALLON

Regardless of the data for display, all is on.

This control has priority over display normal/reverse commands.

ALLON = “0”: Normal display

ALLON = “1”: All display lighted

MON

Select Monochrome or Gradation display

MON = “0”: Gradation display mode

MON = “1”: Monochrome display mode

SHIFT

The shift direction of display scanning data in the common driver output is selected.

SHIFT = “0”: COM0→COM63 shift-scan

SHIFT = “1”: COM63→COM0 shift-scan

8.2.9 Display Control (2) Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	REV	NLIN	SWA	REF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {REV, NLIN, SWAP, REF}=0H, read address: 9H)

Various control of display is set up.

REF

When MPU accesses to display RAM, the X address and data can reverse. The REF function shows in the table below: The order of segment driver output can be reversed by register by register setting, lessening the limitation in placing IC when assembling a LCD module.

REF	*Access from MPU*		*Internal Access*		*Corresponding Segment Output*
	X Address	*D7-D0*	*X Address*	*D7-D0*	
0	NH	D0(LSB) : D7(MSB)	NH	(LSB) : (MSB)	SEG(8*NH)Output : SEG(8*NH+7)Output
1	NH	D0(LSB) : D7(MSB)	maxH-NH	(MSB) : (LSB)	SEG(8*(maxH-NH)+7)Output : SEG(8*(maxH-NH))Output

Note: maxH: The maximum X-address in each access mode.

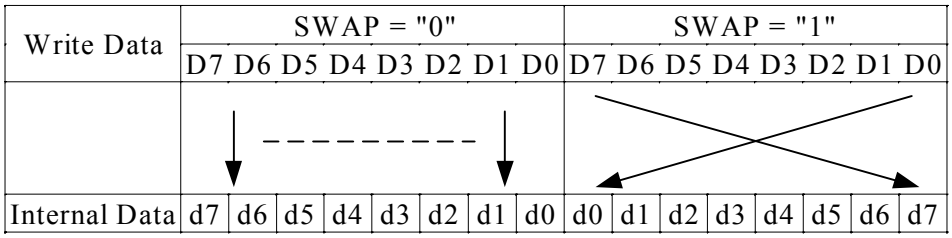
SWAP

When data to display RAM are written, the write data exchange bit order.

SWAP = “0”: Normal mode. In data writing, the data either of D7 to D0 or D15 to D0can be written to the display RAM.

SWAP = “1”: SWAP mode ON. In data writing the swapped data either of D7 to D0 or of D15 to D0 can be written to display RAM.

Example of exchange bit order



CAUTION: REF and SWAP both set to “1”

When data write to display RAM, the write data is normal bit order.

When data read from display RAM, the read data is exchanged bit order.

NLIN

The NLIN control n-line alternated drive.

NLIN = “0”: n-line alternated drive OFF. In each frame, the alternated signals (M) are reversed.

NLIN =”1”: n-line alternated drive ON. According to data set up in n-line alternated register, the alternation is made.

REV

Corresponding to the data of display RAM, the lighting or not-lighting of the display is set up.

REV =”0”: When RAM data at “H”, LCD at ON voltage (normal)

REV =”1”: When RAM data at “L”, LCD at ON voltage (reverse)

8.2.10 Increment Control Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	※	AIM	AYI	AXI

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

※ Mark shows “Don’t care”

(At the tine of reset: {AIM, AYI, AXI}=0H, read address: AH)

The increment mode is set up when accessing to display RAM. By AIM, AYI, AXI register, the setting up of increment operation/non-operation for the X address counter and the Y address counter every write access or every read access to display RAM is possible. In setting to this control register, the increment operation of address can be made without setting successive address for writing data or for reading data to display RAM from MPU.

After the increment control register has been set. be sure to assign address to the X and Y address registers starting from the lowest bit. Because it is not assuring the data of X and Y address register after setting increment control register. The increment control of X and Y address by AIM, AYI, AXI registers is as follows.

AIM	Address Increment Timing
0	When writing to Display RAM or reading from Display RAM This is effective when access to successive address area
1	Only when writing to Display RAM This is effective the case of “Read Modify Write

AYI	AXI	Select Address Increment Operation	Remark
0	0	Address is not increment	(1)
0	1	X-Address is increment	(2)
1	0	Y-Address is increment	(3)
1	1	X and Y both are increment	(4)

(1) Regardless of AIM, no increment for AX and AY register.

(2) According to the setting-up of AIM, automatically change X address.

In accordance with the REF register, AX register and X address becomes as follows.

REF	Transition of AX Register	Transition of X Address
0	00H→ 01H→.....→ max	Same as AX register
1		max→ maxH→..... →00H

Note: maxH: The internal maximum X-address in each access mode.

(3) According to the setting-up of AIM, automatically change Y address. Regardless of REF, increment by loop of

Transition of AY Register	Transition of Y Address
00H→01H→.....→41H	Same as AY register

(4) According to the setting-up of AIM, cooperative change X and Y address. When the X address exceed maxH, Y address increment occurs.

REF	Transition of AX and AY Register	Transition of X and Y Address
0	AX: 00H → 00H→ – – → max AY: When each AX exceed maxH, increment AY 00H → 00H→ – – → 41H	Same as AX and AY register
1		AX: max→ maxH→ – – →00H AY: Same as AY register

Note: maxH: The internal maximum X-address in each access mode.

In each operation mode, the following increment operation is performed:

(i) When gradation display mode and 8-bit access are selected: Address are incremented as described above.

(ii) When gradation display mode and 16-bit access are selected: Two bytes are accessed by accessing the RAM once. The X-addresses increment in the order of 00H,01H,…2EH,and 2FH.

(iii) When monochrome display mode and 8-bit access are selected:

In the monochrome display mode, 0H to 23H are available for X-addresses in the access area.

PSEL = "0": The plane 0 area is selected, and the X-address change in increments in the order of 00H,01H,…22H, and 23H.

PSEL = "1": The plane 1 area is selected, and the X-address change in increments in the order of 00H,01H,…22H, and 23H.

(iv) When monochrome display mode and 16-biit access are selected:

Two bytes are accessed by accessing the RAM once.

PSEL = "0": The plane 0 area is selected, and the X-address change in increments in the order of 00H,01H,…10H,and 11H.

PSEL = "1": The plane 1 area is selected, and the X-address change in increments in the order of 00H,01H,…10H,and 11H.

8.2.11 Power Control Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	AMPON	HALT	DCON	ACL

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {AMPON, HALT, DCON, ACL}=0H, read address: BH)

ACL

The internal circuit can be initialized. This register is effective only at Master operation mode.

ACL = "0": Normal operation

ACL = "1": Initialization ON

When the reset operation begins internally after ACL register sets to "1", the ACL register is automatically cleared to "0". The internal reset signal has been generated with a clock (built-in oscillation circuit or CK input) for the display. Therefore, install the WAIT period for the display clock two cycles at least. After WAIT period, next operation can handle. Since built-in oscillation circuit and external CK input can not be used in the slave mode, the setting of the ACL register becomes the invalidity. Certainly use the RESB terminal, when the reset is applied on the slave chip.

DCON

The internal booster circuit is set ON/OFF

DCON = "0": Booster circuit OFF

DCON="1": Booster circuit ON

HALT

The conditions of power saving are set ON/OFF by this command.

HALT = "0": Normal operation

HALT="1": Power-saving operation

When setting in the power-saving state, the consumed current can be reduced to a value near to the standby current.

The internal condition at power saving are as follows.

(a) The oscillating circuit and power supply circuit are stopped.

(b) The LCD drive is stopped, and output of the segment driver and common driver are VSS level.

(c) The clock input from CK pin is inhibited.

(d) The contents of Display RAM data are maintained.

(e) The operational mode maintains the state of command execution before executing power saving command.

AMPON Command

The internal OP-AMP circuit block (voltage regulator, electronic volume, and voltage conversion circuit) is set ON/OFF by this command.

AMPON = "0": The internal OP-AMP circuit OFF

AMPON = "1": The internal OP-AMP circuit ON

8.2.12 LCD Duty Set

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	※	DS2	DS1	DS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {DS2, DS1, DS0}=0H, read address: CH)

※ **Mark shows "Don't care"**

The DS register set to LCD display duty.

DS2	*DS1*	*DS0*	*Display width and Duty*
0	0	0	8-dot width display in Y-direction, 1/10 duty
0	0	1	16-dot width display in Y-direction, 1/18 duty
0	1	0	24-dot width display in Y-direction, 1/26 duty
0	1	1	32-dot width display in Y-direction, 1/34 duty
1	0	0	40-dot width display in Y-direction, 1/42 duty
1	0	1	48-dot width display in Y-direction, 1/50 duty
1	1	0	56-dot width display in Y-direction, 1/58 duty
1	1	1	64-dot width display in Y-direction, 1/66 duty

Partial display can be made possible by setting an arbitrary duty ratio.

8.2.13 Booster Set

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	※	※	VU1	VU0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {VU2, VU1, VU0}=0H, read address: DH)

※ Mark shows "Don't care"

The booster steps set to VU register

VU1	*VU0*	*Booster Operation*
0	0	Booster disable (No operation)
0	1	2 times voltage output
1	0	3 times voltage output
1	1	4 times voltage output

8.2.14 Bias Setting Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	※	B2	B1	B0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {B2, B1, B0}=0H, read address: EH)

※ Mark shows "Don't care"

This register is used to set a bias ratio. A bias ratio can be selected from 1/9, 1/8, 1/7, 1/6, and 1/5 by setting B2, B1, and B0.

B2	*B1*	*B0*	*Bias*
0	0	0	1/9 Bias
0	0	1	1/8 Bias
0	1	0	1/7 Bias
0	1	1	1/6 Bias
1	0	0	1/5 Bias
1	0	1	Prohibit code
1	1	0	Prohibit code
1	1	1	Prohibit code

8.2.15 Register Access Control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	TST0	RE2	RE1	RE0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

(At the time of reset: {TST0, RE2, RE1, RE0}=0H, read address: FH)

※ Mark shows "Don't care"

The RE register set to number of register bank. Access to each control register, set RE register at first.

The TST0 register use for test of LSI, Therefore this register must be set to "0"

8.2.16 Gradation Palette Register (PA0~PA7, PB0~PB7, PC0~PC7)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PA03	PA02	PA01	PA00

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	※	※	※	PA04

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 1H)

(At the time of reset: PA04~PA00 = "00000")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PA13	PA12	PA11	PA10

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	※	※	※	PA14

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 3H)

(At the time of reset: PA14~PA10 = "00101")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PA23	PA22	PA21	PA20

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PA24

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 5H)

(At the time of reset: PA24~PA20 = "01010")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PA33	PA32	PA31	PA30

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	※	PA34

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 7H)

(At the time of reset: PA34~PA30 = "01110")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PA43	PA42	PA41	PA40

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 8H)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	※	※	※	PA44

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 9H)

(At the time of reset: PA44~PA40 = "10001")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PA53	PA52	PA51	PA50

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: AH)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	※	※	※	PA54

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: BH)

(At the time of reset: PA54~PA50 = "10101")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PA63	PA62	PA61	PA60

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: CH)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	※	※	※	PA64

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: DH)

(At the time of reset: PA64~PA60 = "11010")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PA73	PA72	PA71	PA70

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	※	※	※	PA74

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 1H)

(At the time of reset: PA74~PA70 = “11111”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PB03	PB02	PB01	PB00

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	※	※	※	PB04

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 3H)

(At the time of reset: PB04~PB00 = “00000”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PB13	PB12	PB11	PB10

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PB14

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 5H)

(At the time of reset: PB14~PB10 = “00101”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PB23	PB22	PB21	PB20

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	※	PB24

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 7H)

(At the time of reset: PB24~PB20 = “01010”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PB33	PB32	PB31	PB30

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 8H)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	※	※	※	PB34

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 9H)

(At the time of reset: PB34~PB30 = “01110”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PB43	PB42	PB41	PB40

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: AH)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	※	※	※	PB44

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: BH)

(At the time of reset: PB44~PB40 = “10001”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PB53	PB52	PB51	PB50

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: CH)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	※	※	※	PB54

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: DH)

(At the time of reset: PB54~PB50 = “00101”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PB63	PB62	PB61	PB60

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	※	※	※	PB64

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 1H)

(At the time of reset: PB64~PB60 = “11010”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PB73	PB72	PB71	PB70

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PB74

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 3H)

(At the time of reset: PB74~PB70 = “11111”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PC03	PC02	PC01	PC00

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PC04

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 5H)

(At the time of reset: PC04~PC00 = “00000”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PC13	PC12	PC11	PC10

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	※	PC14

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 7H)

(At the time of reset: PC14~PC10 = “00101”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PC23	PC22	PC21	PC20

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 8H)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	※	※	※	PC24

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 9H)

(At the time of reset: PC24~PC20 = “01010”)

※ Mark shows “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PC33	PC32	PC31	PC30

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: AH)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	※	※	※	PC34

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: BH)

(At the time of reset: PC34~PC30 = "01110")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PC43	PC42	PC41	PC40

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: CH)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	※	※	※	PC44

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: DH)

(At the time of reset: PC44~PC40 = "10001")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PC53	PC52	PC51	PC50

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	※	※	※	PC54

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: 1H)

(At the time of reset: PC54~PC50 = "10101")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PC63	PC62	PC61	PC60

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	※	※	※	PC64

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: 3H)

(At the time of reset: PC64~PC60 = "11010")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PC73	PC72	PC71	PC70

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PC74

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: 5H)

(At the time of reset: PC74~PC70 = "11111")

※ Mark shows "Don't care"

These gradation palette register set up gradation level. The EM65567 has 32 gradation levels. Gradation level table [Three groups of palettes Aj,Bj, and Cj (j=0-7) are available]

Palette	Gradation level	Remarks	Palette	Gradation level	Remarks
0 0 0 0 0	0	gradation palette 0 initial value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	gradation palette 4 initial value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	gradation palette 1 initial value	1 0 1 0 1	21/31	gradation palette 5 initial value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	gradation palette 2 initial value	1 1 0 1 0	26/31	gradation palette 6 initial value
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	gradation palette 3 initial value	1 1 1 1 0	30/31	
0 1 1 1 1	15/31		1 1 1 1 1	31/31	gradation palette 7 initial value

8.2.17 Display Start Common Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	※	SC2	SC1	SC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset:{ SC2,SC1,SC0}=0H, read address: 6H)

※ Mark shows "Don't care"

The SC register set up the scanning start output of the common driver.

SC2	*SC1*	*SC0*	*Display starting common when SHIFT=0*	*Display starting common when SHIFT=1*
0	0	0	COM0~	COM63~
0	0	1	COM8~	COM55~
0	1	0	COM16~	COM47~
0	1	1	COM24~	COM39~
1	0	0	COM32~	COM31~
1	0	1	COM40~	COM23~
1	1	0	COM48	COM15~
1	1	1	COM56	COM7~

SHIFT="0": COM0→ COM63 shift-scan

SHIFT="1": COM63→ COM0 shift-scan

8.2.18 Static Pictograph Control

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	SPC1	SPC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

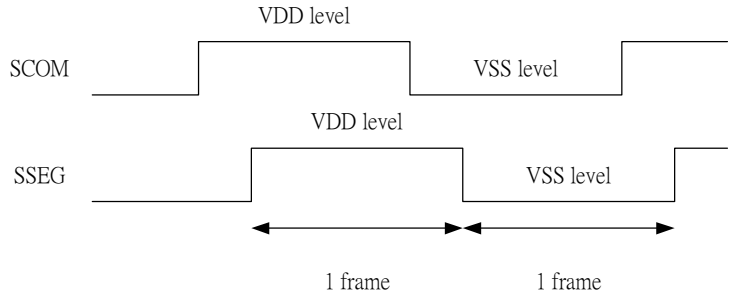
(At the time of reset:{ SPC1,SPC0}=0H, read address: 7H)

Mark shows "Don't care"

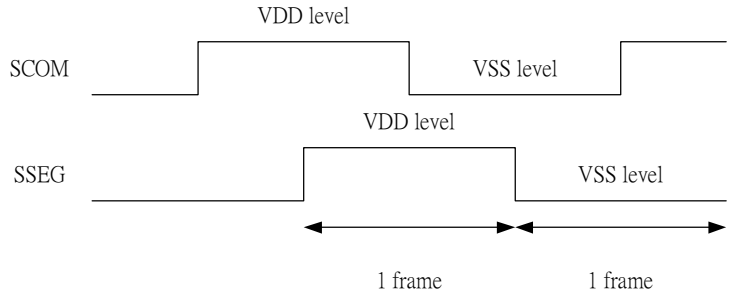
This command is used to select a signal to drive static pictograph.

SPC1	*SPC0*	*Signal for static pictograph*
0	0	VSS level is always output at SCOM and SSEG
0	1	Phase deviates by 45 degrees at SCOM and SSEG
1	0	Phase deviates by 90 degrees at SCOM and SSEG
1	1	Phase deviates by 135 degrees at SCOM and SSEG

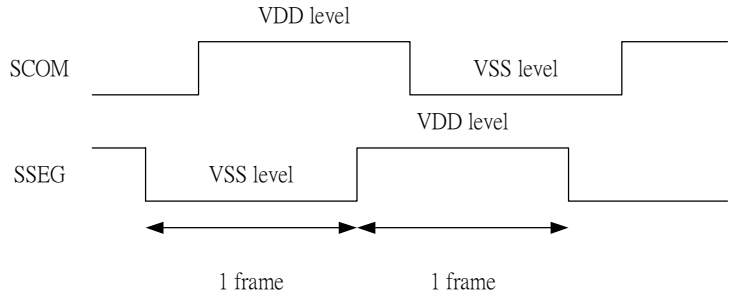
Drive waveform when (SPC1, SPC0) =(0, 1)



Drive waveform when (SPC1, SPC0) =(1, 0)



Drive waveform when (SPC1, SPC0) =(1, 1)



8.2.19 Display Select Control

D7	D6	D5	D4	D3	D2	D1	D0	CSB	RS	RDB	WRB	RE2	RE1	RE0
1	0	0	0	PWM	GLS	PSEL	DSEL	0	1	1	0	1	0	0

(At the time of reset: {PWM, GLSA, PSEL, DSEL} = 0H, read address: 8H)

PSEL

The PSEL register select assessable plane from MPU in the monochrome display mode (MON="1").

PSEL = "0": The plane 0 can access

PSEL = "1": The plane 1 can access

DSEL command

The DSEL register select active plane for display in the monochrome display mode(MON="1").

DSEL = "0": The plane 0 is active for display.

DSEL = "1": The plane 1 is active for display.

GLSB

For the segment driver of 4-gradation display, select 4 gradations from 8 gradations using the 2 bits written to the corresponding RAM area and the 1 bit supplemented by the gradation LSB circuit. Supplement the 1 bit of data by setting the gradation LSB register (GLSB).

Gradation LSB = "0": Selects 0 as the LSB information on the RAM for 4-gradation segment driver.

Gradation LSB = "1": Selects 1 as the LSB information on the RAM for 4-gradation segment driver.

PWM

The PWM register selection the gradation display mode.

PWM = “0”: Variable display mode using 8 gradations selected from 32 gradations

PWM = “1”: 8-gradation fixed display mode

8.2.20 RAM Data Length Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	※	※	※	WLS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {WLS} = 0H, read address: 9H)

※ Mark shows “Don’t care”

The WLS register select data bus size for access from MPU

WLS = “0”: The data bus size is 8-bits width

WLS = “1”: The data bus size is 16-bits width

When MPU access to control register using 16-bits bus size, high byte data is ignored.

8.2.21 Electronic Volume Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	DV3	DV2	DV1	DV0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: AH)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	※	DV6	DV5	DV4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: BH)

(At the time of reset: {DV6~DV0} = 00H)

※ Mark shows “Don’t care”

The DV register can control V0 voltage.

The DV register has 7-bits, so can select 128 level voltage.

DV6	DV5	DV4	DV3	DV2	DV1	DV0	Output voltage
0	0	0	0	0	0	0	Smaller
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	Larger

The output voltage at VREG is specified by equation (1).

VREG = VREF * N * 0.9----------(1)

(N: Number of boosting steps)

The LCD driver voltage V0 is determined by VREG level and electronic volume code equation (2).

V0 = 0.5 * VREG + M * (VREG – 0.5VREG) / 127 ----------(2)

(M: DV6 to DV0 register values)

In order to prevent transient voltage from generating when an electronic volume code is set, the circuit design is such that the set value is not reflected as a level immediately after only the upper bits (DV6-DV4) of the electronic code have been set. The set value becomes valid when the lower bits (DV3-DV0) of the electronic control volume code have also been set.

8.2.22 Internal Register Read Address

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	RA3	RA2	RA1	RA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {RA3, RA2, RA1, RA0} = CH)

The RA register set to specify the address for register read operation. The EM65567 has many registers and has register bank. Therefore, it is need 4-steps to read to read the specific register in maximum case.

(1) Write 04H to RE register for access to RA register.

(2) Writes specific register address to RA register.

(3) Write specific register bank to RE register.

(4) Read specific contents.

8.2.23 Resistance Ratio of CR Oscillator

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	※	RF2	RF1	RF0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {RF2, RF1, RF0} = 0H, read address: DH)

※ Mark shows “Don’t care”

The RF registers can control resistance ratio of CR oscillator. Therefore frame frequency can change RF registers setting. When change RF registers value, should be need to check LCD display quality.

RF2	RF1	RF0	Operation
0	0	0	Initial Resistance Ratio
0	0	1	0.8 times of initial Resistance Ratio
0	1	0	0.9 times of initial Resistance Ratio
0	1	1	1.1 times of initial Resistance Ratio
1	0	0	1.2 times of initial Resistance Ratio
1	0	1	Prohibit Code
1	1	0	Prohibit Code
1	1	1	Prohibit Code

8.2.24 Extended power control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	※	※	HPM	DIS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

At the time of reset: {HPM, DIS} = 0H, {BF1,BF0}=0H;read address: EH)

※mark shows "Don't care"

The DIS register can control capacitors discharged that connected between the power supply V1-V4 for LCD drive voltage and VSS. **Caution**: V0 is discharged to VDD.

DIS = "0": Discharge OFF

DIS = "1": Discharge start

The HPM register is the power control for the power supply circuit for liquid crystal drive.

HPM = "H": High power mode

HPM = "L": Normal mode

BF1~BF0: The operating frequency in the booster is selected. When the boosting frequency is high, the driving ability of booster become high, but the current consumption is increased. Adjust the boosting frequency considering the external capacitors and the current consumption.

BF1	BF0	Operating clock frequency in the booster
0	0	1.5K Hz * 8
0	1	1.5K Hz * 4
1	0	1.5K Hz * 2
1	1	1.5 K Hz

9. Relationship between Setting and Common/Display RAM

The relationship between the COM pin numbers and the addresses in the Y-direction on the display RAM changes according to the SHIFT command. LCD Duty Set command. Display Starting Common Position Set command, and Display Starting Line Set command.

When “0” is selected for the display starting line:
The relationship between the COM pin and the addresses in the vertical direction of the display RAM (hereafter called MY) changes on an 8-dots basis according to the LCD Duty Set command and the Display Starting Common Position Set command. When the SHIFT bit is “0”, the common position change in the forward direction. When “1” they change reverse direction. When “0” is selected as the values for LA5 to LA0 in the Display Starting Line Set command, the MY number corresponding to the display starting position is “0”. The MY numbers are sequentially shifted backward when display occurs. In any case, the relations of COMA = MY64 and COMB = MY65 do not change.

When non-zero is selected for the display starting line:
The relationship between the COM pins and the addresses in the vertical direction on the display RAM, MY changes on an 8-dots basis according to the information in the LCD Duty Set command and Display Starting Common Position Set command. The common positions change in the forward when the SHIFT bit is “0”, and change in the reverse direction when the SHIFT bit is “1”. If non-zero is selected for the values for LA5 to LA0 by the Display Starting Line set command. the MY number corresponding to the display starting position shifts by the set value. The MY number shifts backward when display occurs. If it exceeds 63, it returns to 0, and the shifts sequentially. In any case, the relations of COMA = MY64 and COMB = MY65 do not change.

10. Absolute maximum ratings

10.1 Absolute maximum ratings

Item	*Symbol*	*Condition*	*Pin use*	*Rating*	*Unit*
Supply voltage (1)	VDD	Ta=25℃	VDD	-0.3 ~ + 4.0	V
Supply voltage (2)	VEE		VEE	-0.3 ~ + 4.0	V
Supply voltage (3)	VOUT		VOUT	--0.3 ~ + 13.0	V
Supply voltage (4)	VREG		VREG	-0.3 ~ + 13.0	V
Supply voltage (5)	V0		V0	-0.3 ~ + 13.0	V
Supply voltage (6)	V1,V2,V3,V4		V1,V2,V3,V4	-0.3 ~ V0+ 0.3	V
Input voltage	VI		*1	-0.3 ~ VDD+ 0.3	V
Storage temperature	Tstg			-45 ~ +125	℃

※1: D0~D15, CSB, RS, M/S, M86, P/S, WRB, RDB, CK, CKS, LP, FLM, M, CLK, RESB, TEST, VREF Pins

10.2 Recommended operating conditions

Item	*Symbol*	*Application Pin*	*Min.*	*Max.*	*Unit*	*Note*
Supply voltage	VDD1	VDD	1.8	3.3	V	*1
	VEE	VEE	2.4	3.3	V	*2
Operating voltage	V0	V0	5	12	V	*3
	VOUT	VOUT		12	V	
	VREG	VREG		10.8	V	
	VREF	VREF	2.4	3.3	V	*4
Operating temperature	Topr		-30	80	℃	

※1 shows applying voltage to VSS pin.

※2 shows applying voltage to VSS pin. Usually, if applying voltage is same as VDD. Connect to VDD pin.

※3 shows the voltage relationship of V0>V1>V2>V3>V4>VSS is required.

※4 shows applying voltage to VSS pin.. In the case of using the voltage regulator. The voltage relationship of VREF≦VEE is required.

11. DC characteristics

VSS=0V , VDD = 1.8~3.3V , Ta = -30 ~80 ℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
High level input voltage	VIH		0.8VDD	0.9VDD	VDD	V	※ 1
Low level input voltage	VIL		0	0.1VDD	0.2VDD	V	※ 1
High level output current	IOH1	VOH = VDD-0.4V	-0.4	-0.5	-0.6	mA	※ 2
Low level output current	IOL1	VOL= 0.4V	0.4	0.5	0.6	mA	※ 2
High level output current	IOH2	VOH = VDD-0.4V	-0.1	-0.2	-0.3	mA	※ 3
Low level output current	IOL2	VOL= 0.4V	0.1	0.2	0.3	mA	※ 3
Input leakage current	ILI	VI = VSS or VDD	-2	0	2	µA	※ 4
Output leakage current	ILO	VI = VSS or VDD	-2	0	2	µA	※ 5
LCD driver output resistance	RON	Δ |Von| = 0.5V, V0=10V	1.0	1.3	1.6	KΩ	※ 6
		Δ |Von| = 0.5V, V0=6V	1.2	1.7	2.2		
LCD driver output resistance	RON	Δ |Von| = 0.5V, VDD=3V	1.5	2	2.5	KΩ	※ 7
Standby current through VDD pin	ISTB	CK=0, CSB=VDD, Ta=25℃, VDD=3V		5	15	µA	※ 8
Oscillator frequency (variable gradation mode)	fosc	VDD=3V, Ta=25℃, Rf setting = (Rf2,Rf1,Rf0)=(000)	260	372	484	KHz	※ 9
Oscillator frequency (8 gradation mode)	fosc	VDD=3V, Ta=25 ℃, Rf setting = (Rf2,Rf1,Rf0)=(00 0)	58	84	110	KHz	※10
Oscillator frequency (monochrome mode)	fosc	VDD=3V , Ta=25℃, Rf setting = (Rf2,Rf1,Rf0)=(000)	8	12	16	KHz	※11
Booster output voltage on VOUT pin	VOUT1	Four times boosting RL = 500KΩ (VOUT-VSS)	4*VEE *0.95			V	※12
	VOUT2	Three times boosting RL = 500KΩ (VOUT-VSS)	3*VEE *0.95			V	※13
	VOUT3	Two times boosting RL = 500KΩ(VOUT-VSS)	2*VEE *0.95			V	※14
Current consumption	IDD1	VDD = 3V, 4 times booster All ON pattern		55	70	µA	※15
	IDD2	VDD = 3V, 4 times booster Checker pattern		130	160	µA	※16
	IDD2	VDD = 3V, 3 times booster All ON pattern		30	40	µA	※17
	IDD2	VDD = 3V, 3 times booster Checker pattern		65	80	µA	※18
VREG output voltage	VREG	VEE =2.4V~3.3V, VREF=2.4~3.3, N times boosting (N=2 to 4)	(VREF*N*0.9) *0.95	VREF*N *0.9	(VREF*N*0.9) *1.05	V	※19

Relationship of oscillating frequency (fosc) and external clock frequency (fCK) to LCD frame frequency (fFLM) is each display mode

Original oscillating clock	Display mode	Ratio of display duty cycle (1/D)				Pin used
		1/66, 1/58, 1/50	1/42, 1/34, 1/26	1/18	1/10	
When use built-in oscillating circuit (fosc)	Variable gradation	fosc/(2*31*D)	fosc/(4*31*D)	fosc/(8*31*D)	fosc/(16*31*D)	FLM
	Simple gradation	fosc/(2*7*D)	fosc/(4*7*D)	fosc/(8*7*D)	fosc/(16*7*D)	
	Monochrome	fosc/(2*1*D)	fosc/(4*1*D)	fosc/(8*1*D)	fosc/(16*1*D)	
When use external clock from CK pin. (fCK)	Variable gradation	fCK/(2*31*D)	fCK /(4*31*D)	fCK /(8*31*D)	fCK /(16*31*D)	
	Simple gradation	fCK /(2*7*D)	fCK /(4*7*D)	fCK /(8*7*D)	fCK /(16*7*D)	
	Monochrome	fCK /(2*1*D)	fCK /(4*1*D)	fCK /(8*1*D)	fCK /(16*1*D)	

Pin used:

※ **1** D0-D15, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, CLK, LP, FLM, M, P/S, RESB, TEST pins.

※ **2** D0~D15 pins

※ **3** LP, FLM, M, CLK pins

※ **4** CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins

※ **5** Applied when D0~D15, CLK, LP, FLM, and M are in the state of high impedance.

※ **6** SEGA0~SEGA95, SEGB0~SEGB95, SEGC0~SEGC95. COM0~COM63, COMA, COMB pins Resistance when being applied 0.5V between each output pin and each power supply (V0, V1, V2, V3, V4) and when being applied 1/9 bias.

※ **7** SSEG, SCOM pins

※ **8** VDD pin, VDD pin current without load at the stoppage of original oscillating clock and at non-select (CSB=VDD)

※ **9** Oscillating frequency, when using the built-in oscillating circuit (variable gradation display mode)

※ **10** Oscillating frequency, when using the built-in oscillating circuit (8 gradation fixed display mode)

※ **11** Oscillating frequency, when using the built-in oscillating circuit (monochrome display mode)

※ **12** VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 4 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/66 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”

※ **13** VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 3 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/66 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”

※ **14** VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 2 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/66 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”

※ **15** VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from

MPU. This pin is applied. Boosting 4 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display ALL ON pattern (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE=VREF, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”

※ **16** VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 4 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display a checkered pattern (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE=VREF, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”

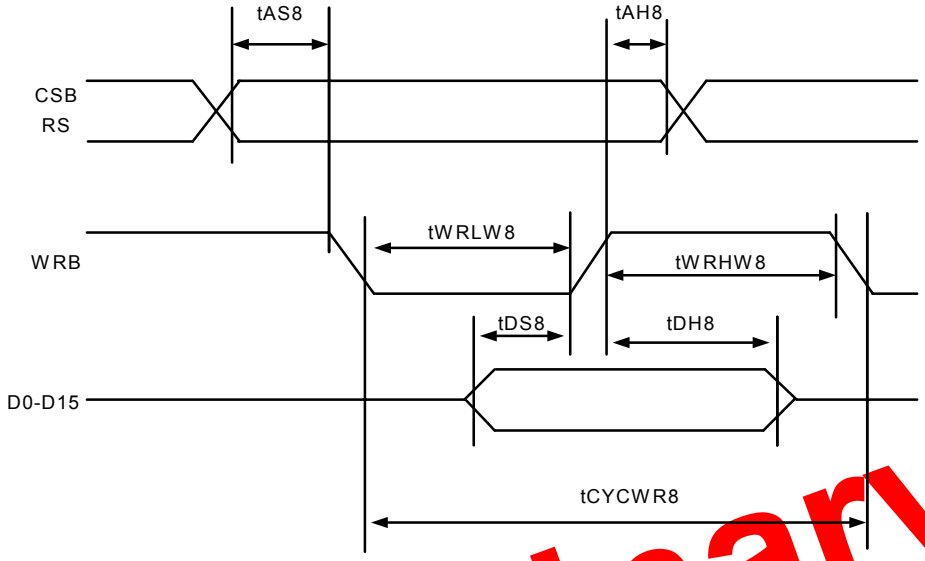
※ **17** VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 3 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display ALL ON pattern (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE=VREF, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”

※ **18** VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 3 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display a checkered pattern (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE=VREF, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”

※ **19** VREG pin. Measuring conditions: VEE=VREF=2.4~3.3 V, bias=1/5~1/9, 1/66 duty.

12. AC characteristic

(1) 80-family MCU write timing



VSS=0V, VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in write	tCYCWR8		250			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		60			ns	
Write pulse “H” width	tWRHW8		185			ns	
Data setup time	tDS8		60			ns	D0~D15
Data hold time	tDH8		5			ns	

VSS=0V, VDD = 2.4~2.7V , Ta = -30~+85℃

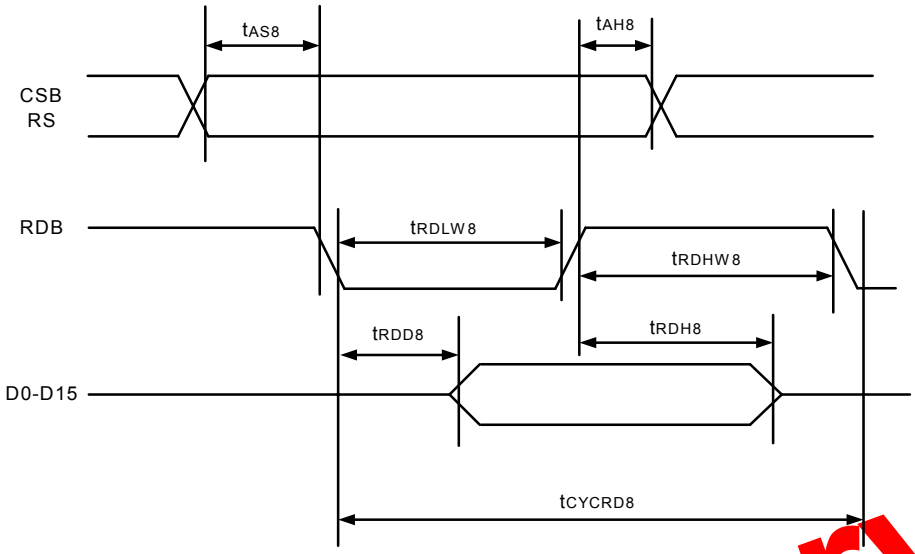
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in write	tCYCWR8		330			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		80			ns	
Write pulse “H” width	tWRHW8		240			ns	
Data setup time	tDS8		80			ns	D0~D15
Data hold time	tDH8		10			ns	

VSS=0V, VDD = 2.4~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in write	tCYCWR8		660			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		140			ns	
Write pulse “H” width	tWRHW8		500			ns	
Data setup time	tDS8		100			ns	D0~D15
Data hold time	tDH8		20			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(2) 80-family MCU read timing



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in read	tCYCRD8		450			ns	RDB(E)
Read pulse “L” width	tRDLW8		200			ns	
Read pulse “H” width	tRDHW8		185			ns	
Data setup time	tRDD8	CL = 80 pF			250	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85℃

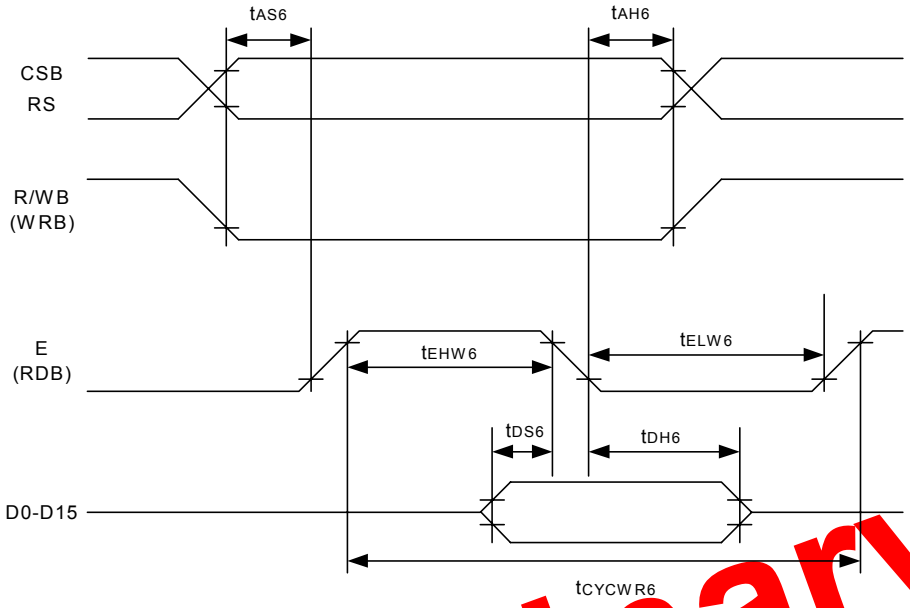
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in read	tCYCRD8		600			ns	RDB(E)
Read pulse “L” width	tRDLW8		220			ns	
Read pulse “H” width	tRDHW8		240			ns	
Data setup time	tRDD8	CL = 80 pF			350	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in read	tCYCRD8		1000			ns	RDB(E)
Read pulse “L” width	tRDLW8		450			ns	
Read pulse “H” width	tRDHW8		500			ns	
Data setup time	tRDD8	CL = 80 pF			650	ns	D0~D15
Data hold time	tRDH8		10			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(3) 68-family MCU write timing



VSS=0V , VDD = 2.7 ~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCWR6		250			ns	RDB(E)
Write pulse “L” width	tELW6		60			ns	
Write pulse “H” width	tEHW6		185			ns	
Data setup time	tDS6		60			ns	D0~D15
Data hold time	tDH6		5			ns	

VSS=0V , VDD = 2.4 ~2.7V , Ta = -30~+85℃

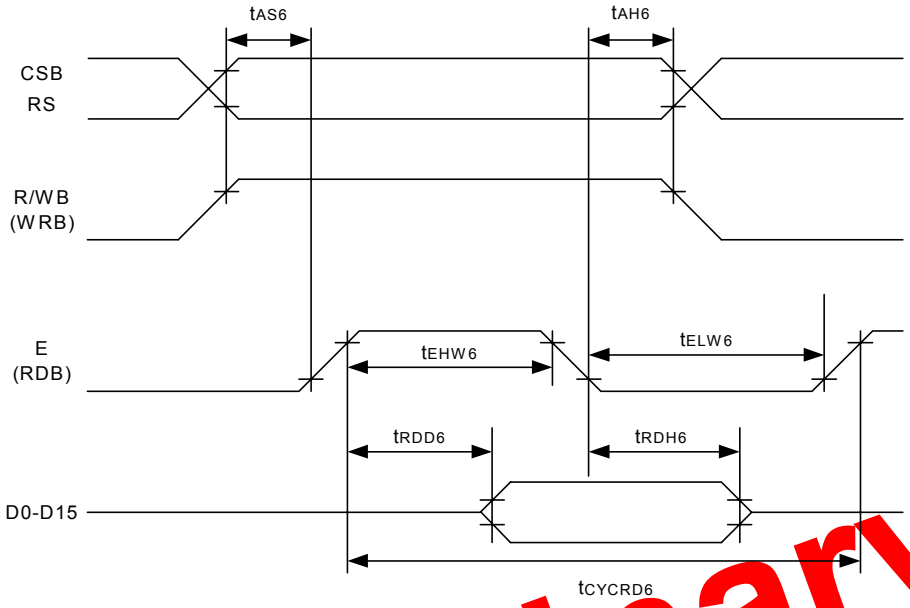
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCWR6		330			ns	RDB(E)
Write pulse “L” width	tELW6		80			ns	
Write pulse “H” width	tEHW6		240			ns	
Data setup time	tDS6		80			ns	D0~D15
Data hold time	tDH6		10			ns	

VSS=0V , VDD = 1.8 ~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCWR6		660			ns	RDB(E)
Write pulse “L” width	tELW6		140			ns	
Write pulse “H” width	tEHW6		500			ns	
Data setup time	tDS6		100			ns	D0~D15
Data hold time	tDH6		20			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(4) 68-family MCU read timing



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCRD6		450			ns	RDB(E)
Write pulse “L” width	tELW6		200			ns	
Write pulse “H” width	tEHW6		185			ns	
Data setup time	tRDD6	CL=80pF			250	ns	D0~D15
Data hold time	tRDH6		10			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85℃

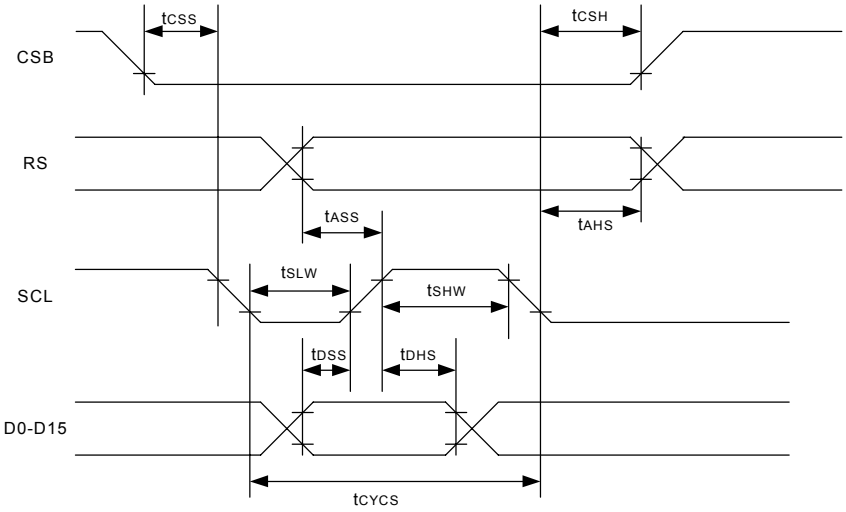
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCRD6		600			ns	RDB(E)
Write pulse “L” width	tELW6		220			ns	
Write pulse “H” width	tEHW6		240			ns	
Data setup time	tRDD6	CL=80pF			350	ns	D0~D15
Data hold time	tRDH6		10			ns	

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCRD6		1000			ns	RDB(E)
Write pulse “L” width	tELW6		450			ns	
Write pulse “H” width	tEHW6		500			ns	
Data setup time	tRDD6	CL=80pF			650	ns	D0~D15
Data hold time	tRDH6		10			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(5) Serial interface timing diagram



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		40			ns	RS
Address hold time	tAHS		40			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		40			ns	CSB
CSB hold time	tCSH		40			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85℃

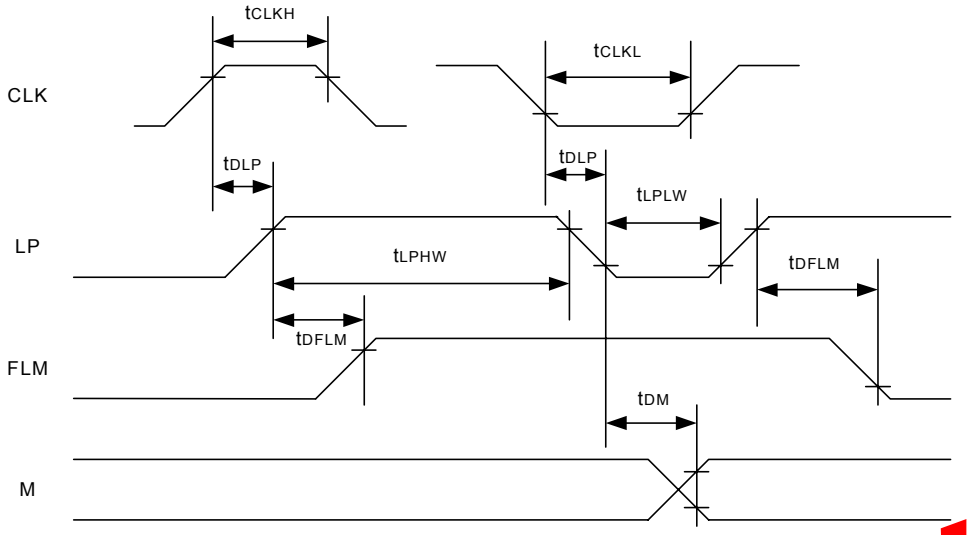
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		250			ns	SCL
SCL pulse “H” width	tSHW		100			ns	
SCL pulse “L” width	tSLW		100			ns	
Address setup time	tASS		50			ns	RS
Address hold time	tAHS		50			ns	
Data setup time	tDSS		100			ns	SDA
Data hold time	tDHS		100			ns	
CSB-SCL time	tCSS		50			ns	CSB
CSB hold time	tCSH		50			ns	

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		1000			ns	SCL
SCL pulse “H” width	tSHW		400			ns	
SCL pulse “L” width	tSLW		400			ns	
Address setup time	tASS		80			ns	RS
Address hold time	tAHS		80			ns	
Data setup time	tDSS		400			ns	SDA
Data hold time	tDHS		400			ns	
CSB-SCL time	tCSS		80			ns	CSB
CSB hold time	tCSH		80			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(6) Display control timing



Input timing (Slave mode) VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CLK pulse “H” width	tCLKH		1.6			µs	CLK
CLK pulse “L” width	tCLKL		1.6			µs	
LP pulse “H” width	tLPHW		80			µs	LP
LP pulse “L” width	tLPLW		80			µs	
LP delay time	tDLP		-1		1	µs	
FLM delay time	tDFLM		-1		1	µs	FLM
M delay time	tDM		-1		1	µs	M

Input timing (Slave mode) VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CLK pulse “H” width	tCLKH		1.6			µs	CLK
CLK pulse “L” width	tCLKL		1.6			µs	
LP pulse “H” width	tLPHW		80			µs	LP
LP pulse “L” width	tLPLW		80			µs	
LP delay time	tDLP		-1		1	µs	
FLM delay time	tDFLM		-1		1	µs	FLM
M delay time	tDM		-1		1	µs	M

output timing (Master mode) VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

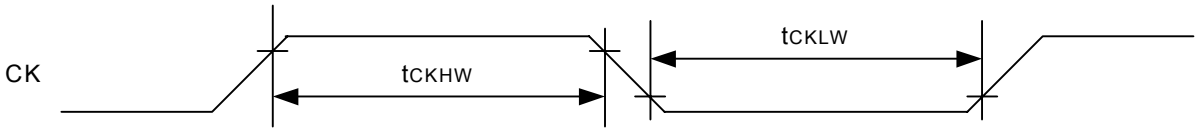
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
LP delay time	tDLP	CL =15 pF	10		500	ns	LP
FLM delay time	tDFLM		10		500	ns	FLM
M delay time	tDM		10		500	ns	M

output timing (Master mode) VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
LP delay time	tDLP	CL =15 pF	10		1000	µs	LP
FLM delay time	tDFLM		10		1000	µs	FLM
M delay time	tDM		10		1000	µs	M

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(7) Master clock input timing



VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CK pulse "H" width (1)	tCKHW1		1.2		1.4	μs	CK
CK pulse "L" width (1)	tCKLW1		1.2		1.4	μs	※ 1
CK pulse "H" width (2)	tTCKHW2		5.4		6.5	μs	CK
CK pulse "L" width (2)	tCKLW2		5.4		6.5	μs	※ 2
CK pulse "H" width (3)	tCKHW3		38		45	μs	CK
CK pulse "L" width (3)	tCKLW3		38		45	μs	※ 3

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

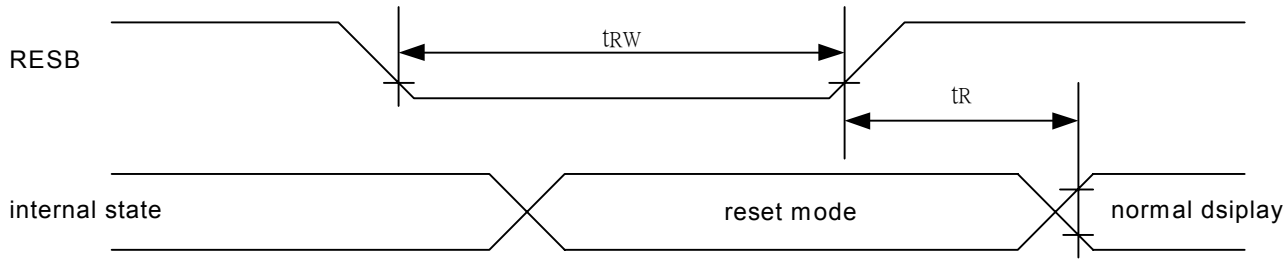
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CK pulse "H" width (1)	tCKHW1	Note1	1.2		1.4	μs	CK
CK pulse "L" width (1)	tCKLW1	Note1	1.2		1.4	μs	※ 1
CK pulse "H" width (2)	tCKHW2	Note2	5.4		6.5	μs	CK
CK pulse "L" width (2)	tCKLW2	Note2	5.4		6.5	μs	※ 2
CK pulse "H" width (3)	tCKHW3	Note3	3.8		4.5	μs	CK
CK pulse "L" width (3)	tCKLW3	Note3	3.8		4.5	μs	※ 3

※ 1 Applied when the gradation display mode.

※ 2 Applied when the simple gradation mode.

※ 3 Applied when the monochrome mode.

(8) Reset timing



VSS=0V, VDD = 2.4~3.3V, Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Reset time	tR				1	µs	
Reset pulse "L" width	tRW		10			µs	RESB

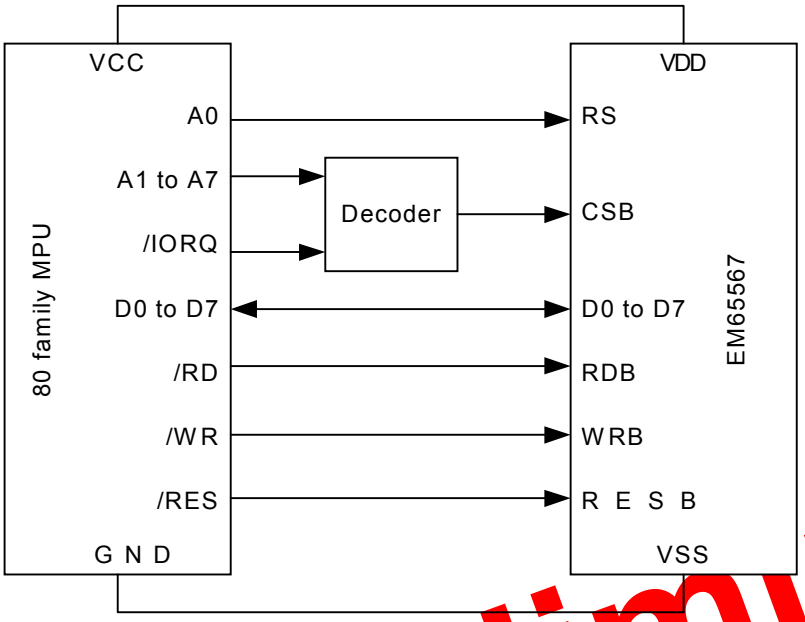
VSS=0V, VDD = 1.8~2.4V, Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Reset time	tR				1.5	µs	
Reset pulse "L" width	tRW		10			µs	RESB

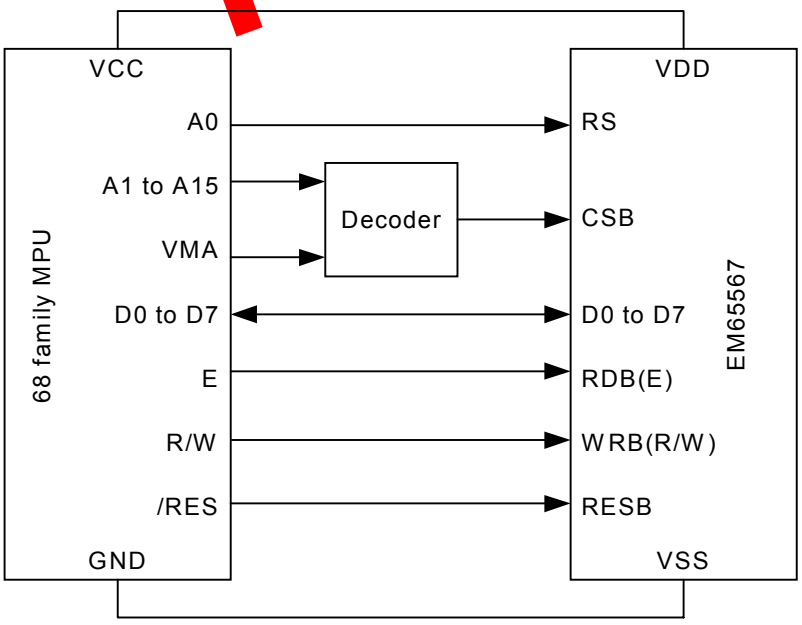
Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

13. Application circuit

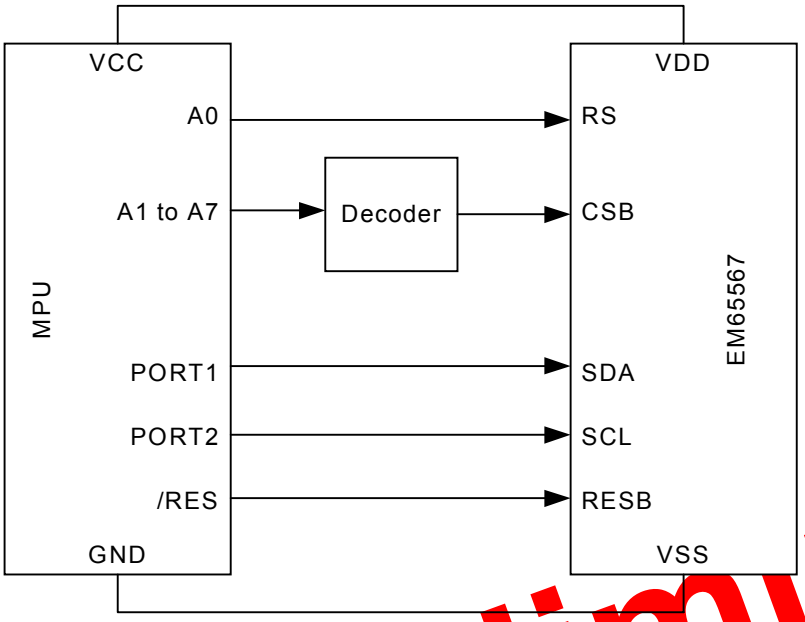
(1) Connection to 80-family MCU



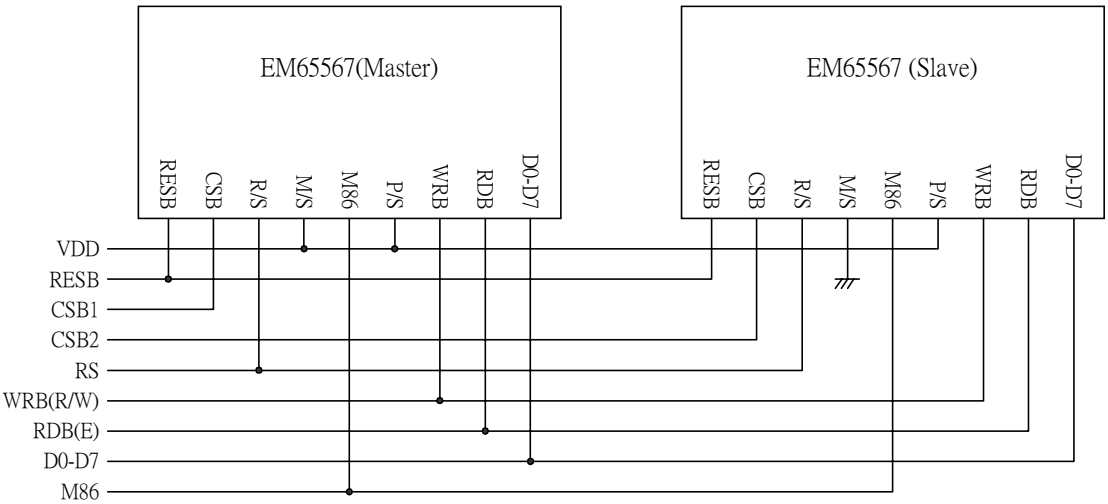
(2) Connection to 68-family MCU



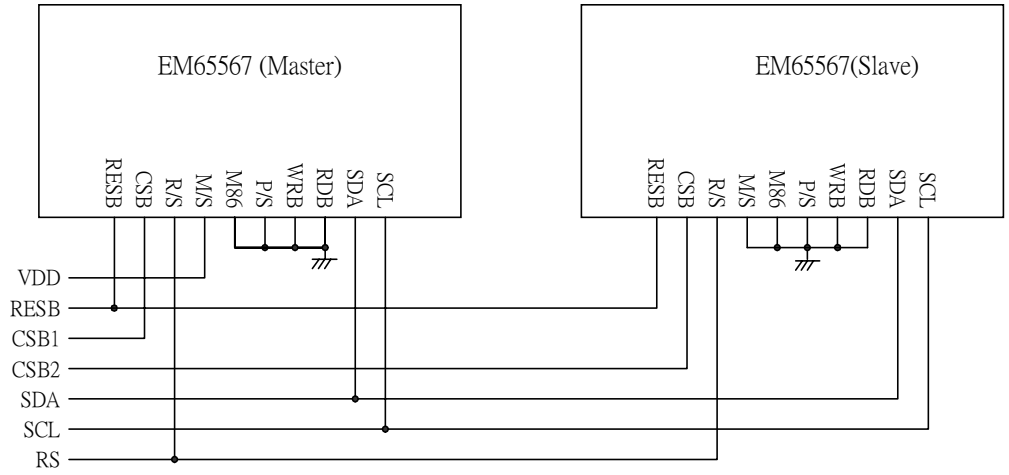
(3) Connection to the MCU with serial interface



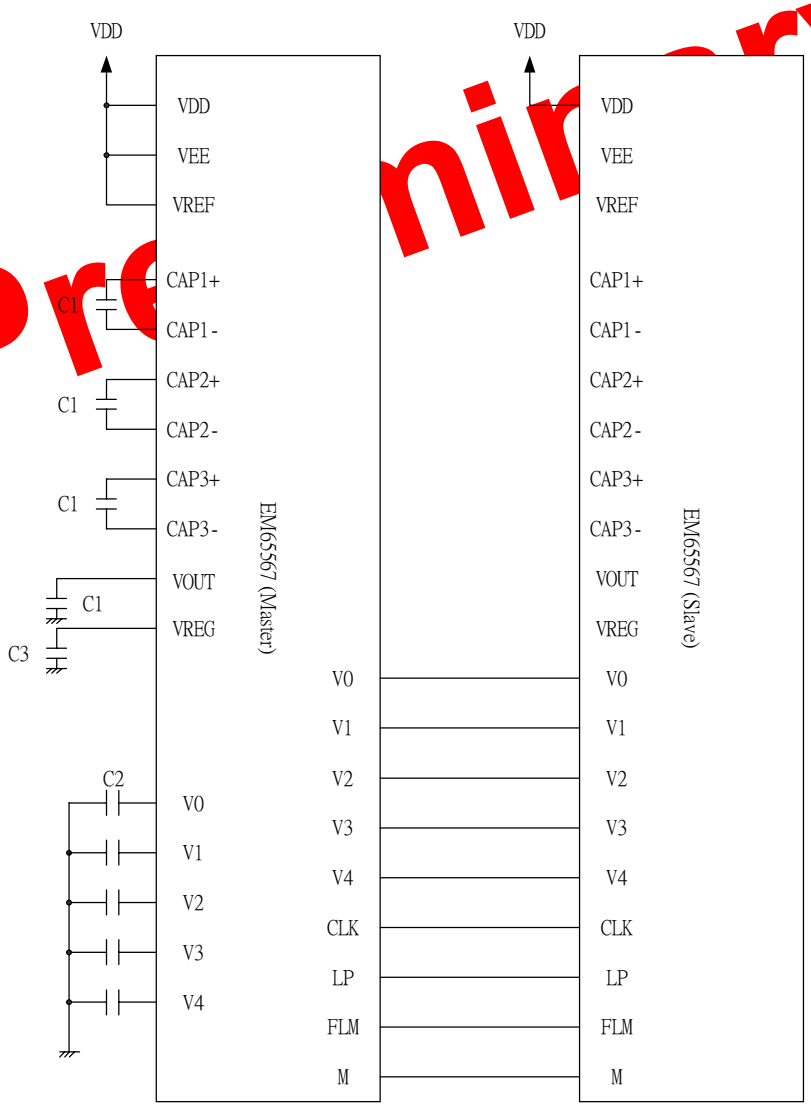
(4) Connection to Master / Slave about interface (parallel interface)



(5) Serial interface



(6) Connection to master / slave about power block



Caution of application about master / slave

* The master chip control display timing (CLK,LP,FLM, and M). When making display OFF on the master chip, the master chip can not output the display timing. When making display OFF , beforehand set display OFF to the slave chip and set display OFF to the master chip.

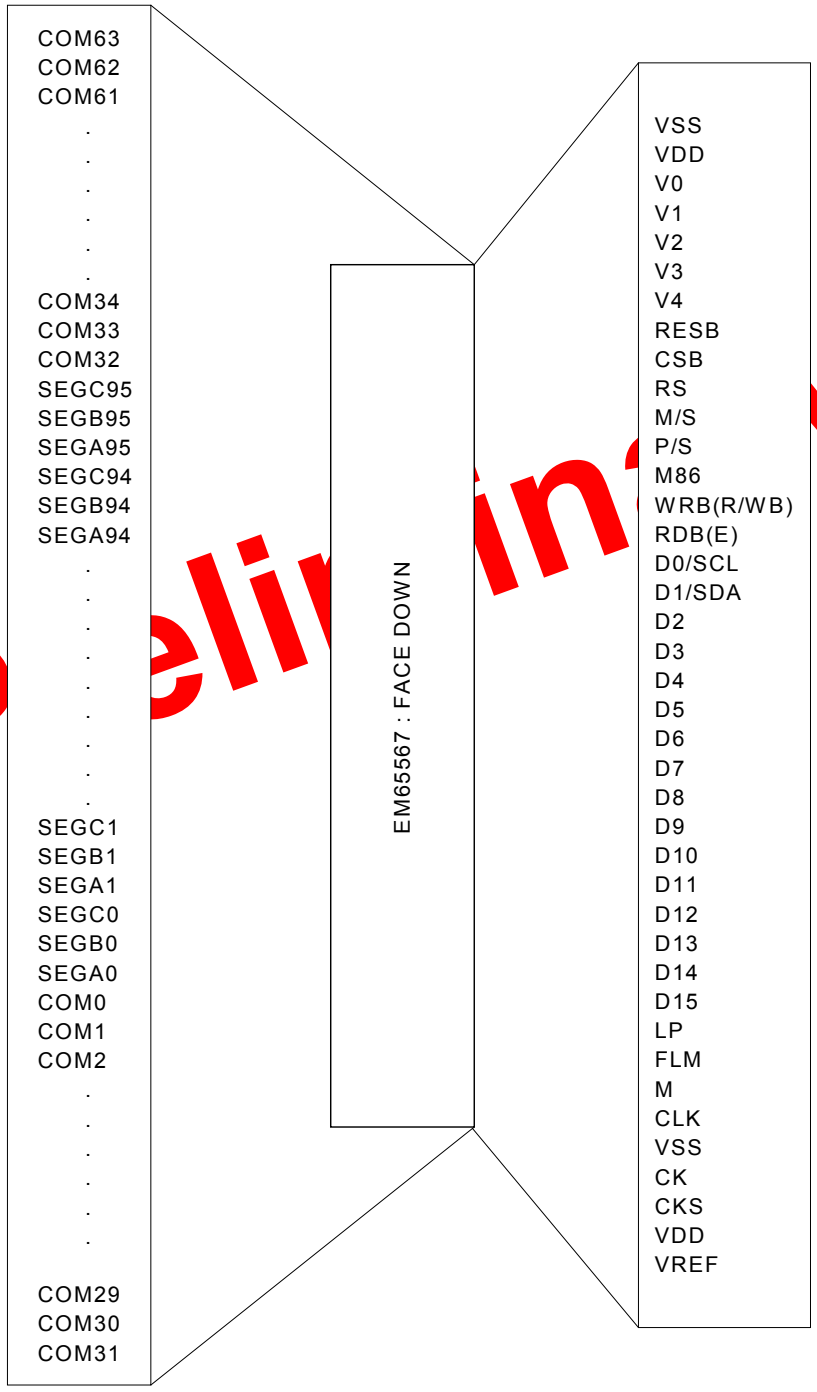
* When setting halt command, turn off the internal power supply, and output VSS level from LCD drive output pins , is set display OFF state. Because the master chip can not supply output voltage to the slave chip, beforehand set display OFF to the slave chip.

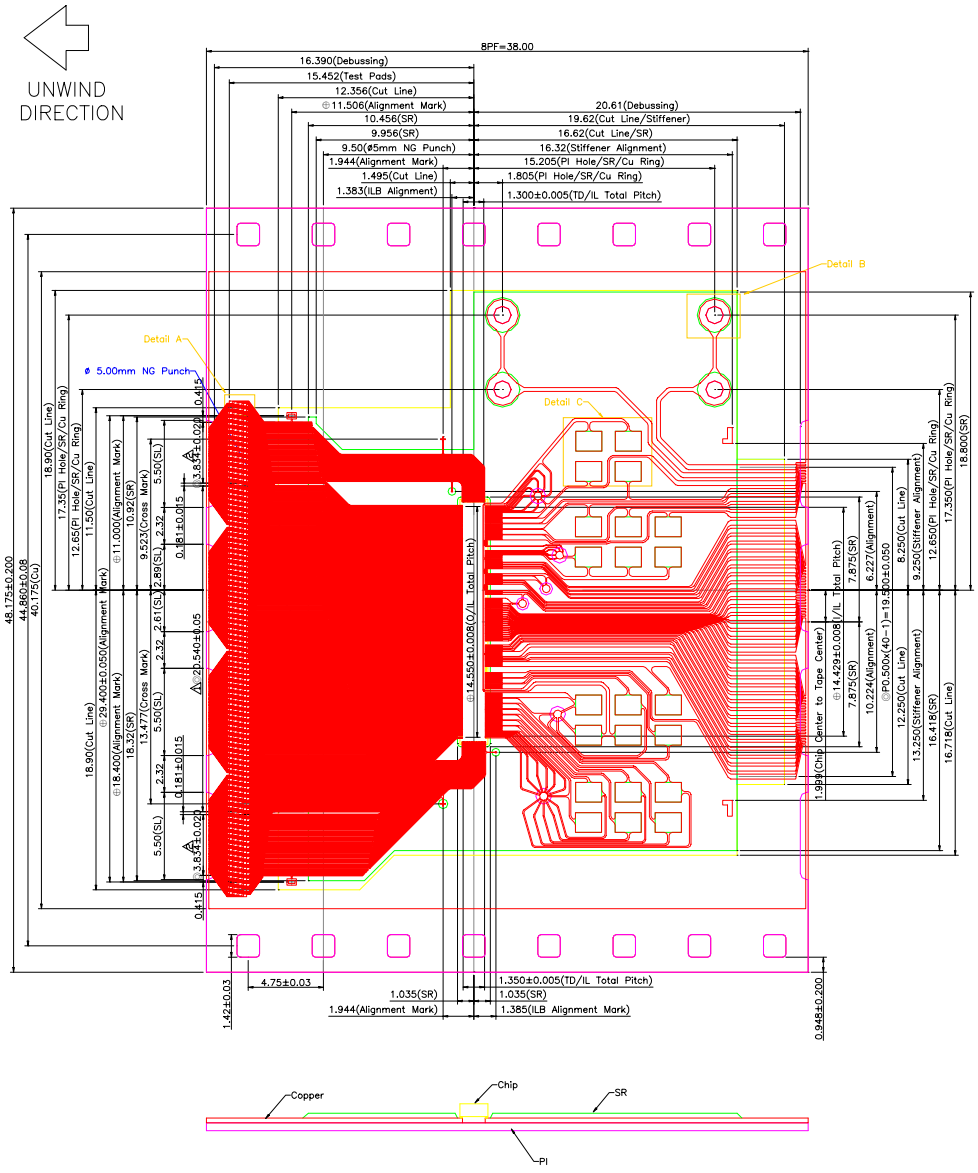
*In above connection example, the master chip is only available the electronic volume control.

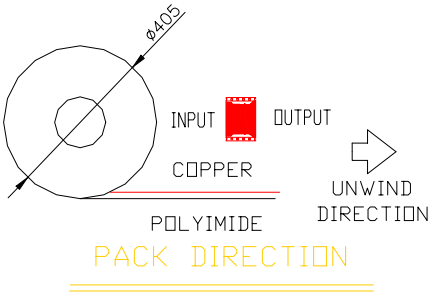
14. COF information

EM65567AF package

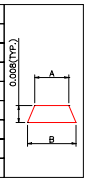
Pin connection diagram (64 x 96RGB outputs)



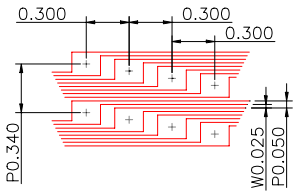




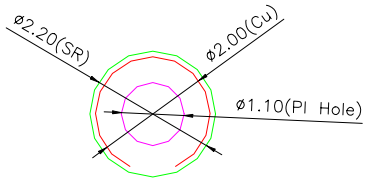
◎ Inner Lead Cross Section		
Item	A (Top)	B (Bottom)
Input IL	Min. 25um	35±8um
Output IL	Min. 18um	25±5um
TD IL	Min. 18um	25±5um
⊕ Outer Lead Cross Section		
Input OL	Min. 290um	310±20um
⚠1 Output OL	Min. 30um	40±10um
⚠2 Output OL	Min. 35um	50±15um



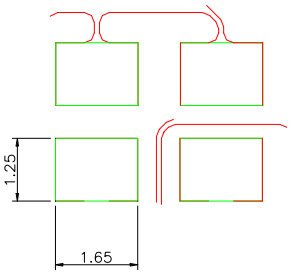
TAPE SPEC		48SW
PRODUCT PITCH		8 PERFORATIONS (38.00mm)
MATERIAL	Toyo CCL	PI: Kapton 38±3μm
		Copper: 8±1.5μm
	SOLDER RESIST	NPR-90 5~25μm
	PLATING	⊕Au 0.5±0.15μm ⊕Ni Min 0.50μm



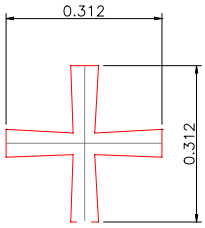
Detail A
Scale 5:1



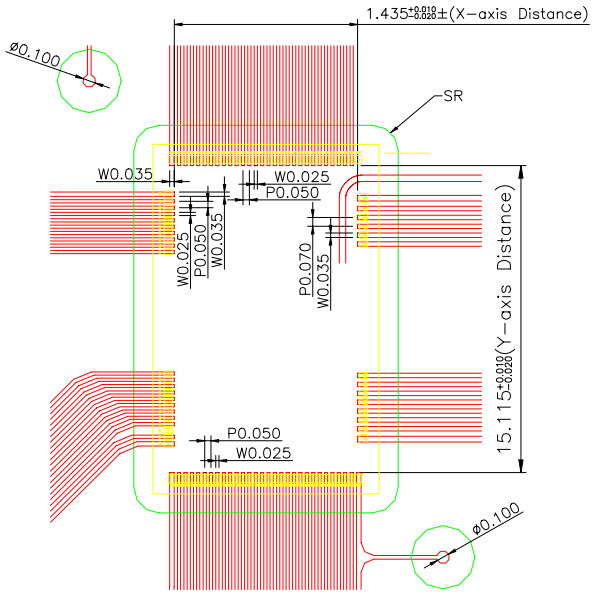
Detail B
Scale 2:1



Detail C
Scale 2:1



Detail of Cross Mark
Scale 20:1



Detail IL
Scale 10:1

NOTES:

1. All Chamfer is R0.20mm if not specified
2. All SR Dimension Tolerance ±0.200mm if not specified
3. All SL Dimension Tolerance ±0.05mm if not specified
4. PKG Reel Size : ø405mm
5. Input IL total pitch from top 2nd to bottom 2nd
6. Output IL total pitch from top 2nd to bottom 2nd
7. IL total pitch in TD from right 2nd to left 2nd
8. MIN Pitch=55um(IL)
9. NG Punch size is ø5.00mm