

## GENERAL DESCRIPTION

The EM6112K800V is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

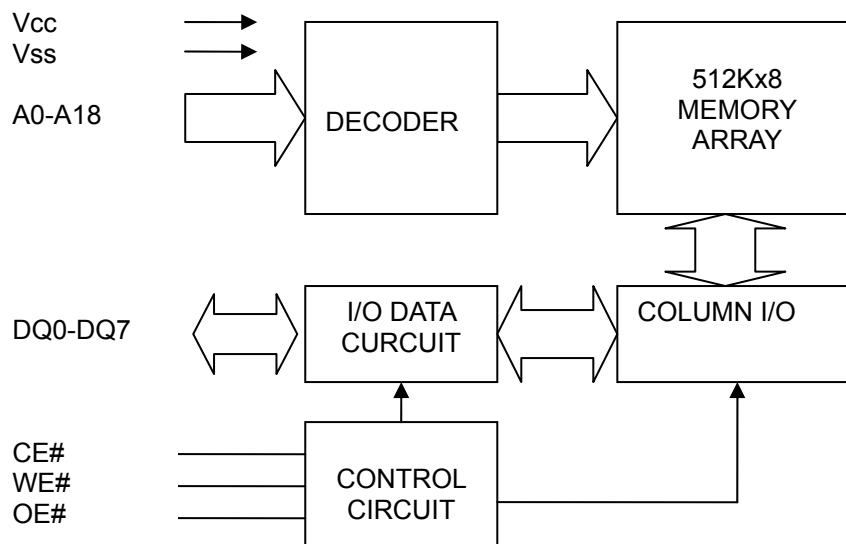
The EM6112K800V is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The EM6112K800V operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

## FEATURES

- Fast access time: 45/55/70ns
- Low power consumption:  
Operating current:  
40/30/20mA (TYP.)  
Standby current: -L/-LL version  
20/2μA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage: 1.5V (MIN.)
- Package:  
32-pin 450 mil SOP  
32-pin 8mm x 20mm TSOP-I  
32-pin 8mm x 13.4mm STSOP  
36-ball 6mm x 8mm TFBGA

## FUNCTIONAL BLOCK DIAGRAM

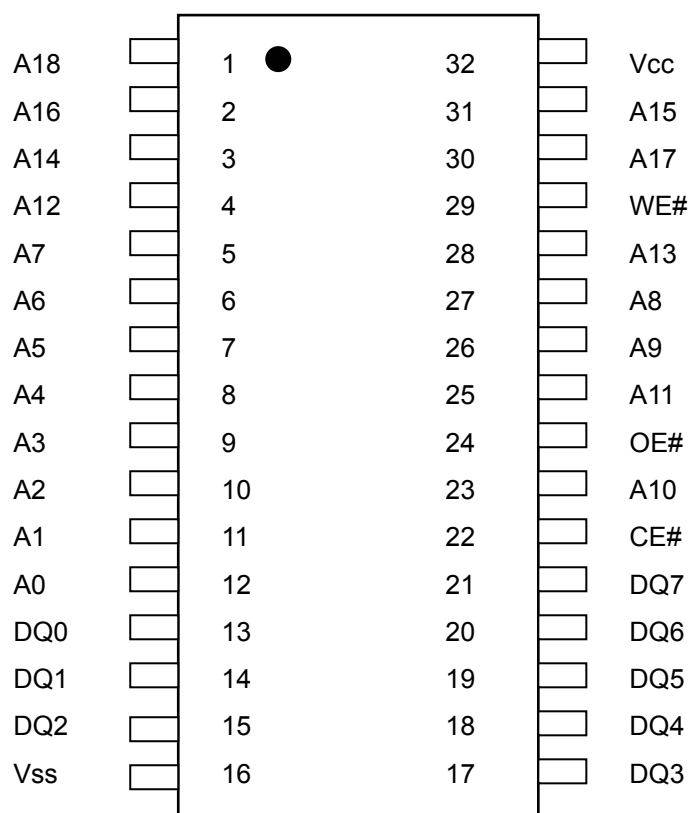


## PIN DESCRIPTION

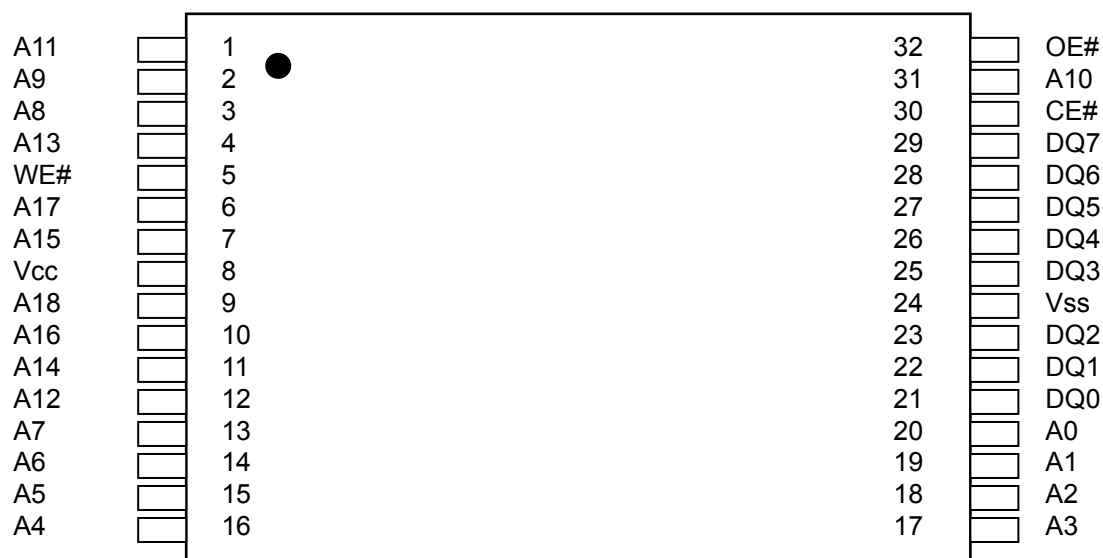
| SYMBOL    | DESCRIPTION         |
|-----------|---------------------|
| A0 - A18  | Address Inputs      |
| DQ0 – DQ7 | Data Inputs/Outputs |
| CE#       | Enable Input        |
| WE#       | Write Enable Input  |
| OE#       | Output Enable Input |
| Vcc       | Power Supply        |
| Vss       | Ground              |

## PIN CONFIGURATION

### SOP



### TSOP-I/STSOP



TFBGA

|   |     |     |     |     |     |     |
|---|-----|-----|-----|-----|-----|-----|
| A | A0  | A1  | NC  | A3  | A6  | A8  |
| B | DQ4 | A2  | WE# | A4  | A7  | DQ0 |
| C | DQ5 |     | NC  | A5  |     | DQ1 |
| D | Vss |     |     |     |     | Vcc |
| E | Vcc |     |     |     |     | Vss |
| F | DQ6 |     | A17 | A18 |     | DQ2 |
| G | DQ7 | OE# | CE# | A16 | A15 | DQ3 |
| H | A9  | A10 | A11 | A12 | A13 | A14 |
|   | 1   | 2   | 3   | 4   | 5   | 6   |

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER                                        | SYMBOL              | RATING             | UNIT |
|--------------------------------------------------|---------------------|--------------------|------|
| Terminal Voltage with Respect to V <sub>SS</sub> | V <sub>TERM</sub>   | -0.5 to 4.6        | V    |
| Operating Temperature                            | T <sub>A</sub>      | 0 to 70(C grade)   | °C   |
|                                                  |                     | -20 to 80(E grade) |      |
|                                                  |                     | -40 to 85(I grade) |      |
| Storage Temperature                              | T <sub>STG</sub>    | -65 to 150         | °C   |
| Power Dissipation                                | P <sub>D</sub>      | 1                  | W    |
| DC Output Current                                | I <sub>OUT</sub>    | 50                 | mA   |
| Soldering Temperature (under 10 sec)             | T <sub>SOLDER</sub> | 260                | °C   |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | CE# | OE# | WE# | I/O OPERATION    | SUPPLY CURRENT                     |
|----------------|-----|-----|-----|------------------|------------------------------------|
| Standby        | H   | X   | X   | High-Z           | I <sub>SB</sub> , I <sub>SB1</sub> |
| Output Disable | L   | H   | H   | High-Z           | I <sub>CC</sub> , I <sub>CC1</sub> |
| Read           | L   | L   | H   | D <sub>OUT</sub> | I <sub>CC</sub> , I <sub>CC1</sub> |
| Write          | L   | X   | L   | D <sub>IN</sub>  | I <sub>CC</sub> , I <sub>CC1</sub> |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

| PARAMETER                              | SYMBOL             | TEST CONDITION                                                                                           | MIN. | TYP. *5 | MAX.                 | UNIT |
|----------------------------------------|--------------------|----------------------------------------------------------------------------------------------------------|------|---------|----------------------|------|
| Supply Voltage                         | V <sub>CC</sub>    |                                                                                                          | 2.7  | 3.0     | 3.6                  | V    |
| Input High Voltage                     | V <sub>IH</sub> *1 |                                                                                                          | 2.0  | -       | V <sub>CC</sub> +0.3 | V    |
| Input Low Voltage                      | V <sub>IL</sub> *2 |                                                                                                          | -0.2 | -       | 0.6                  | V    |
| Input Leakage Current                  | I <sub>LI</sub>    | V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>                                                      | -1   | -       | +1                   | μA   |
| Output Leakage Current                 | I <sub>LO</sub>    | V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> ,<br>Output Disabled                                | -1   | -       | 1                    | μA   |
| Output High Voltage                    | V <sub>OH</sub>    | I <sub>OH</sub> = -1mA                                                                                   | 2.2  | 2.7     | -                    | V    |
| Output Low Voltage                     | V <sub>OL</sub>    | I <sub>OL</sub> = 2mA                                                                                    | -    | -       | 0.4                  | V    |
| Average Operating Power supply Current | I <sub>CC</sub>    | Cycle time = Min.<br>CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA                                      | -45  | -       | 40                   | mA   |
|                                        |                    |                                                                                                          | -55  | -       | 30                   | mA   |
|                                        |                    |                                                                                                          | -70  | -       | 20                   | mA   |
|                                        | I <sub>CC1</sub>   | Cycle time = 1μs<br>CE# ≤ 0.2V and I <sub>I/O</sub> = 0mA<br>other pins at 0.2V or V <sub>CC</sub> -0.2V | -    | 4       | 5                    | mA   |
| Standby Power Supply Current           | I <sub>SB</sub>    | CE# = V <sub>IH</sub>                                                                                    | -    | 0.3     | 0.5                  | mA   |
|                                        | I <sub>SB1</sub>   | CE# V ≥ V <sub>CC</sub> - 0.2V                                                                           | -L   | -       | 20                   | μA   |
|                                        |                    |                                                                                                          | -LL  | -       | 2                    | μA   |

Notes:

1. V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
2. V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. 10μA for special request
5. Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

| PARAMETER                | SYMBOL    | MIN. | MAX. | UNIT |
|--------------------------|-----------|------|------|------|
| Input Capacitance        | $C_{IN}$  | -    | 6    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | -    | 8    | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

|                                          |                                                                              |
|------------------------------------------|------------------------------------------------------------------------------|
| Input Pulse Levels                       | 0.2V to $V_{CC} - 0.2\text{V}$                                               |
| Input Rise and Fall Times                | 3ns                                                                          |
| Input and Output Timing Reference Levels | 1.5V                                                                         |
| Output Load                              | $C_L = 30\text{pF} + 1\text{TTL}$ , $I_{OH}/I_{OL} = -1\text{mA}/2\text{mA}$ |

**AC ELECTRICAL CHARACTERISTICS****READ CYCLE**

| PARAMETER                          | SYM.        | -45  |      | -55  |      | 70   |      | UNIT |
|------------------------------------|-------------|------|------|------|------|------|------|------|
|                                    |             | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |      |
| Read Cycle Time                    | $t_{RC}$    | 45   | -    | 55   | -    | 70   | -    | ns   |
| Address Access Time                | $t_{AA}$    | -    | 45   | -    | 55   | -    | 70   | ns   |
| Chip Enable Access Time            | $t_{ACE}$   | -    | 45   | -    | 55   | -    | 70   | ns   |
| Output Enable Access Time          | $t_{OE}$    | -    | 25   | -    | 30   | -    | 35   | ns   |
| Chip Enable to Output in Low-Z     | $t_{CLZ}^*$ | 10   | -    | 10   | -    | 10   | -    | ns   |
| Output Enable to Output in Low-Z   | $t_{OLZ}^*$ | 5    | -    | 5    | -    | 5    | -    | ns   |
| Chip Disable to Output in High-Z   | $t_{CHZ}^*$ | -    | 15   | -    | 20   | -    | 25   | ns   |
| Output Disable to Output in High-Z | $t_{OHZ}^*$ | -    | 15   | -    | 20   | -    | 25   | ns   |
| Output Hold from Address Change    | $t_{OH}$    | 10   | -    | 10   | -    | 10   | -    | ns   |

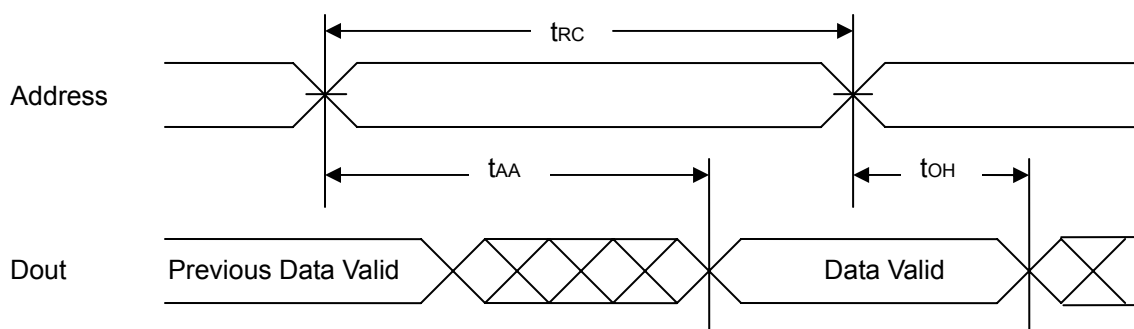
**WRITE CYCLE**

| PARAMETER                        | SYM.        | -45  |      | -55  |      | 70   |      | UNIT |
|----------------------------------|-------------|------|------|------|------|------|------|------|
|                                  |             | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |      |
| Write Cycle Time                 | $t_{WC}$    | 45   | -    | 55   | -    | 70   | -    | ns   |
| Address Valid to End of Write    | $t_{AW}$    | 40   | -    | 50   | -    | 60   | -    | ns   |
| Chip Enable to End of Write      | $t_{CW}$    | 40   | -    | 50   | -    | 60   | -    | ns   |
| Address Set-up Time              | $t_{AS}$    | 0    | -    | 0    | -    | 0    | -    | ns   |
| Write Pulse Width                | $t_{WP}$    | 35   | -    | 45   | -    | 55   | -    | ns   |
| Write Recovery Time              | $t_{WR}$    | 0    | -    | 0    | -    | 0    | -    | ns   |
| Data to Write Time Overlap       | $t_{DW}$    | 20   | -    | 25   | -    | 30   | -    | ns   |
| Data Hold from End of Write Time | $t_{DH}$    | 0    | -    | 0    | -    | 0    | -    | ns   |
| Output Active from End of Write  | $t_{OW}^*$  | 5    | -    | 5    | -    | 5    | -    | ns   |
| Write to Output in High-Z        | $t_{WHZ}^*$ | -    | 15   | -    | 20   | -    | 25   | ns   |

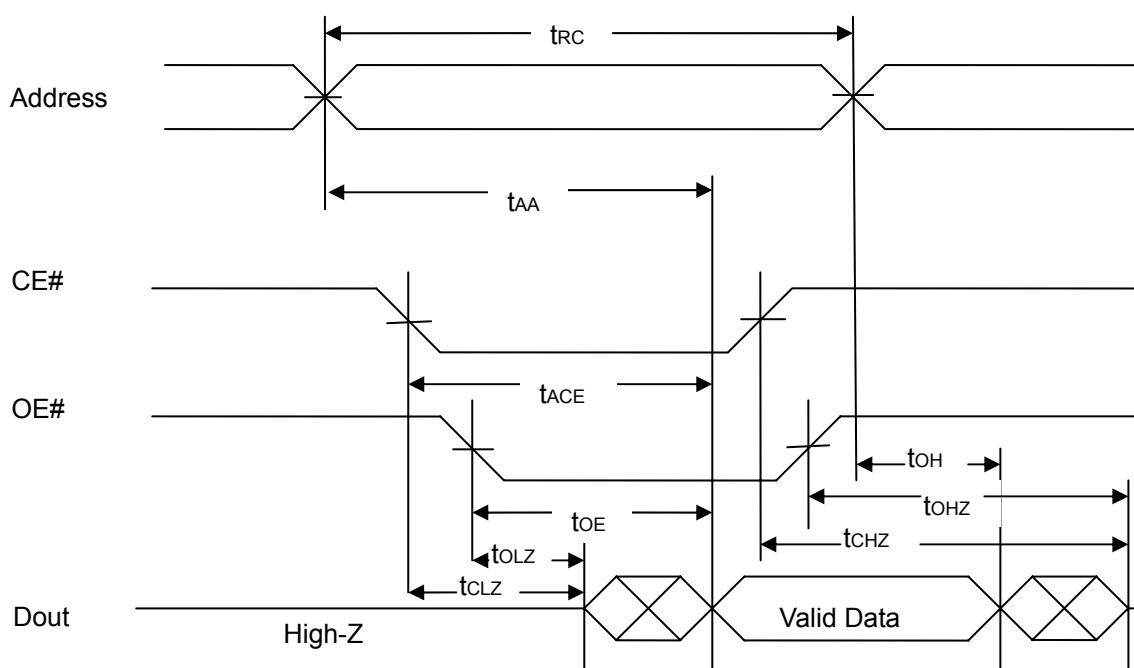
\*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

## READ CYCLE 1 (Address Controlled) (1,2)

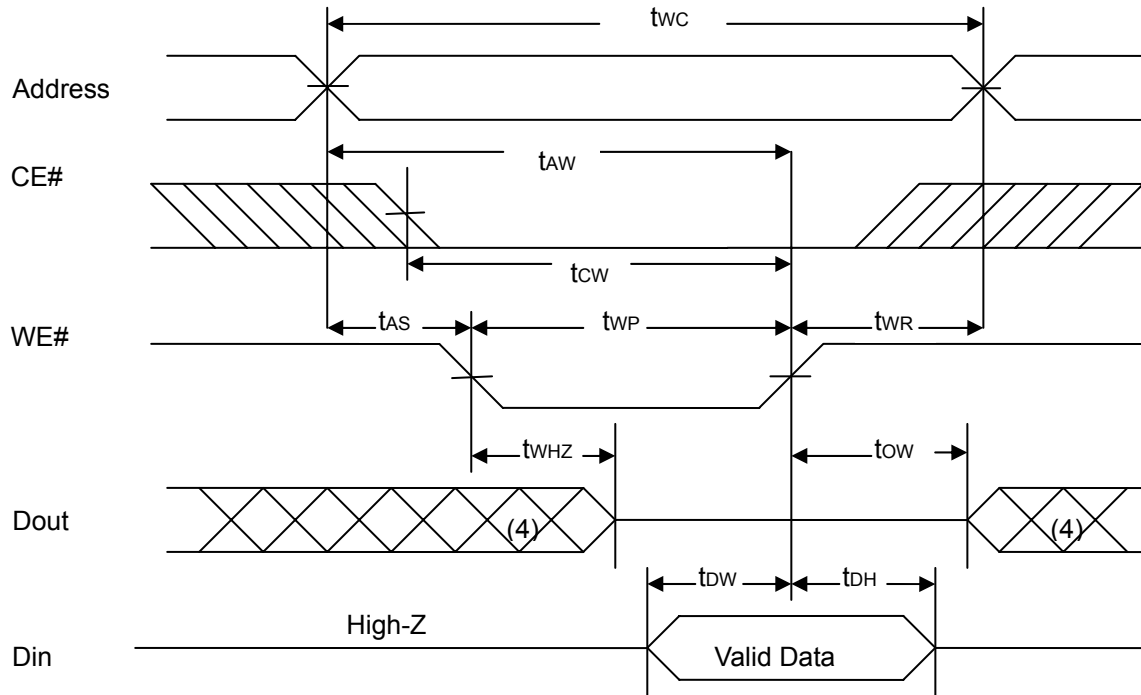
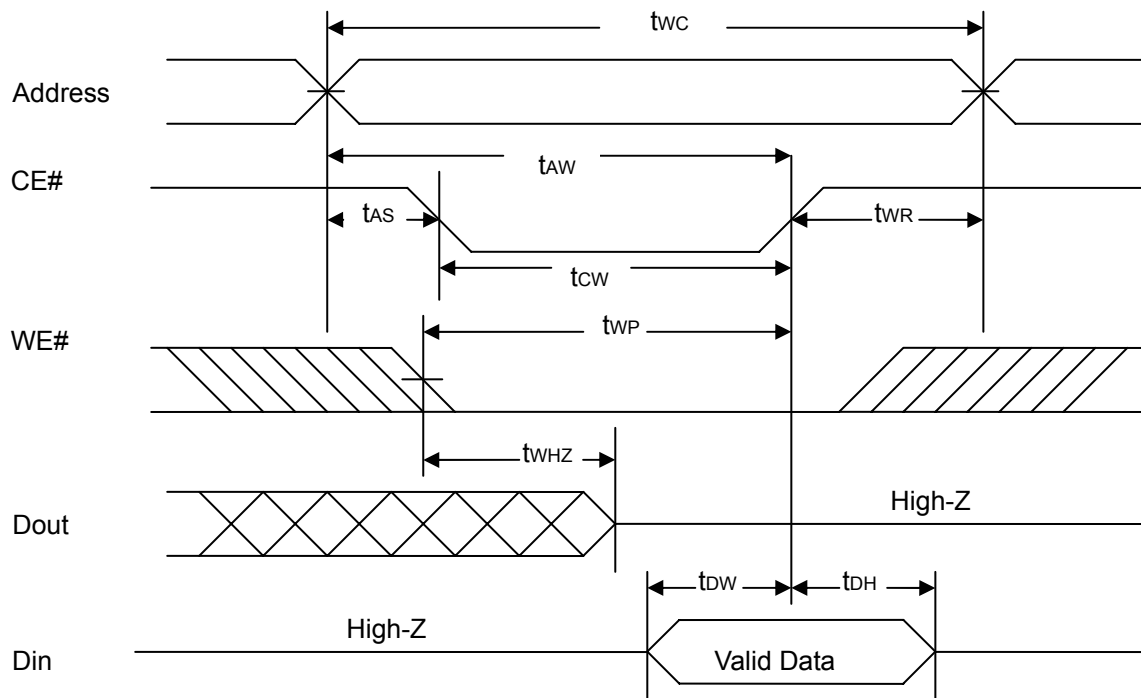


## READ CYCLE 2 (CE#, CE2 and OE# controlled) (1,3,4,5)



## Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)****WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)****Notes :**

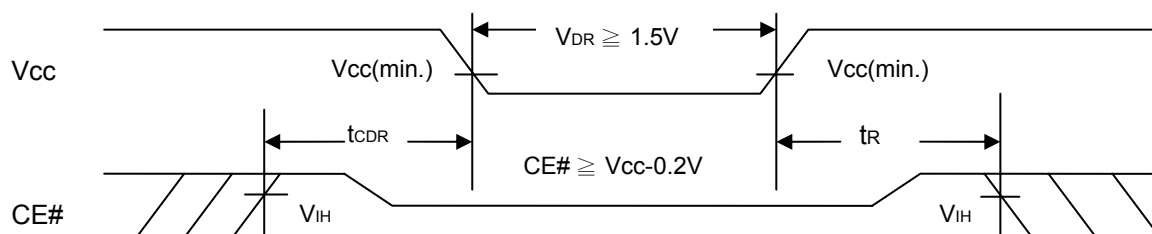
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tow and twhz are specified with CL = 5pF. Transition is measured  $\pm 500\text{mV}$  from steady state.

## DATA RETENTION CHARACTERISTICS

| PARAMETER                           | SYMBOL           | TEST CONDITION                                                | MIN.              | TYP. | MAX. | UNIT    |
|-------------------------------------|------------------|---------------------------------------------------------------|-------------------|------|------|---------|
| VCC for Data Retention              | V <sub>DR</sub>  | CE# V $\geq$ V <sub>CC</sub> - 0.2V                           | 1.5               | -    | 3.6  | V       |
| Data Retention Current              | I <sub>DR</sub>  | V <sub>CC</sub> = 1.5V<br>CE# V $\geq$ V <sub>CC</sub> - 0.2V | -L                | -    | 1    | $\mu$ A |
|                                     |                  |                                                               | -LL               | -    | 0.5  | $\mu$ A |
|                                     |                  |                                                               | -LLE              | 0.5  | 12   | $\mu$ A |
|                                     |                  |                                                               | -LLI              |      |      |         |
| Chip Disable to Data Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)                          | 0                 | -    | -    | ns      |
| Recovery Time                       | t <sub>R</sub>   |                                                               | t <sub>RC</sub> * | -    | -    | ns      |

t<sub>RC</sub>\* = Read Cycle Time

## DATA RETENTION WAVEFORM





### 32 pin 450 mil SOP Package Outline Dimension

The mechanical drawing of the 74VHC00 package includes the following views and dimensions:

- Top View:** Shows a rectangular package with a width of 20.45 mm (maximum) and a height of 11.30 mm. Pin 1 is located at the bottom-left corner. Pin 16 is at the bottom-right corner. Pins 32 and 17 are at the top-left and top-right corners, respectively.
- Side View:** Shows the package height of 3.00 mm (maximum) and a pin pitch of 1.00 mm (maximum).
- Cross-sectional View:** Shows the package thickness of 0.22 ± 0.05 mm, the solder thickness of 0.20 ± 0.04 mm, and the lead height of 1.42 mm. The lead angle is specified as 0° to 8°. The distance from the package body to the lead tip is 0.80 ± 0.20 mm. The total length of the package is 14.14 ± 0.30 mm.
- Other Dimensions:** The distance from the package body to the first pin is 1.27 mm. The distance from the package body to the last pin is 0.15 ± 0.12 mm (minimum 0.10 mm).
- Material and Surface Finish:** The drawing includes a circular symbol with a cross-hatch pattern and a diameter of 0.10 mm, and a circular symbol with a cross-hatch pattern and a diameter of 0.15 mm (M).
- Surface Finish:** The drawing includes a circular symbol with a cross-hatch pattern and a diameter of 0.10 mm, and a circular symbol with a cross-hatch pattern and a diameter of 0.15 mm (M).

INDEX MARK

18.5(.728)  
18.3(.720)

20.2(.795)  
19.8(.780)

0.50(.020)  
BSC

7.50(.295)  
REF

0.25(.010)  
0.15(.006)

8.20(.323)  
7.80(.307)

1.20(.047) MAX

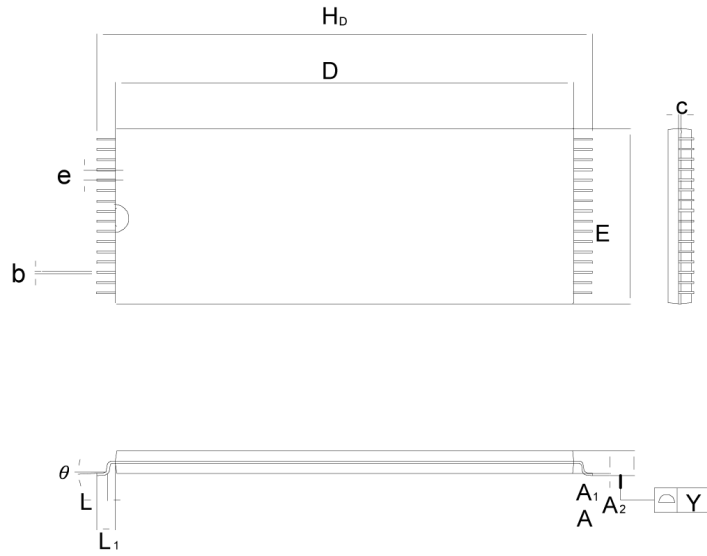
0.15(.006)  
0.05(.002)

0/5 REF

0.20(.008)  
0.10(.004)

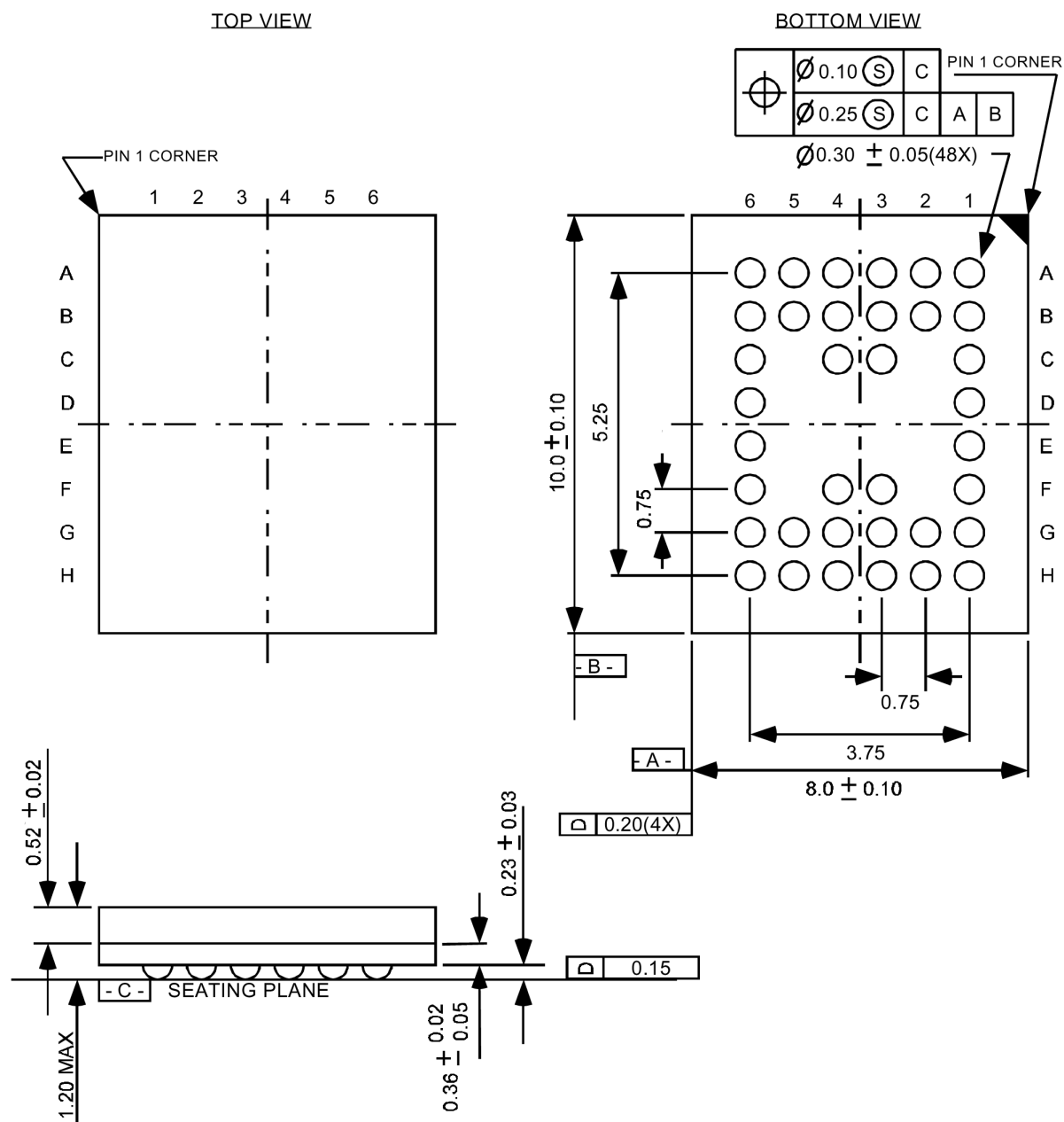
0.70(.028)  
0.50(.020)

32 pin 8mm x 13.4mm STSOP Package Outline Dimension

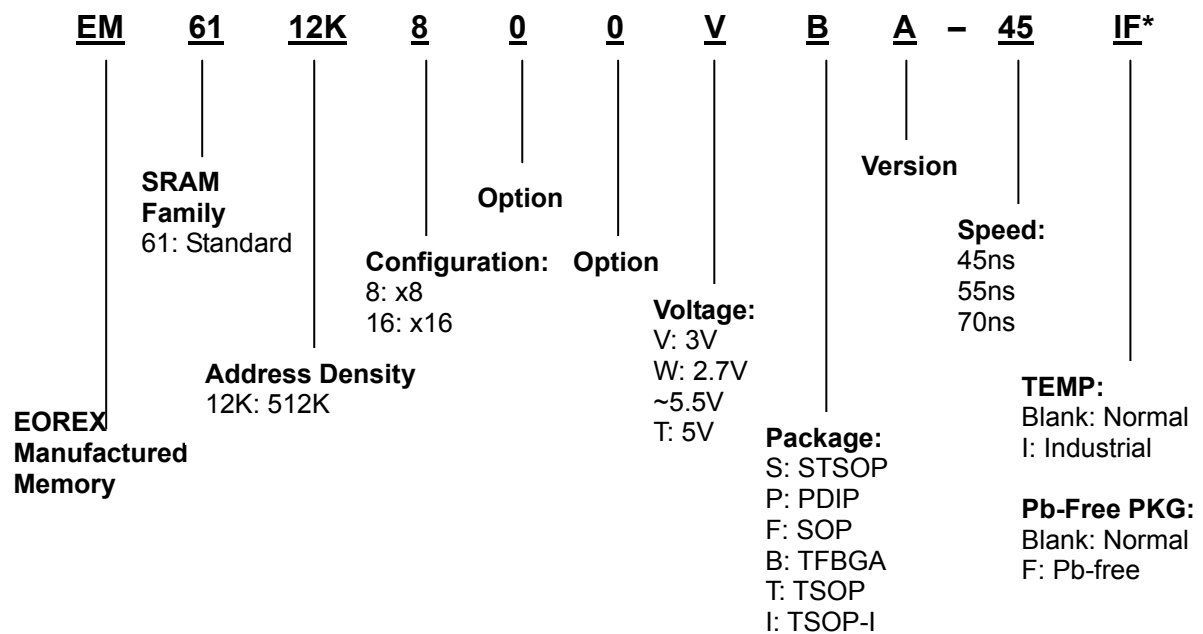


| Symbol         | Dimension in Inches |       |       | Dimension in mm |       |      |
|----------------|---------------------|-------|-------|-----------------|-------|------|
|                | Min.                | Nom.  | Max.  | Min.            | Nom.  | Max. |
| A              |                     |       | 0.047 |                 |       | 1.20 |
| A <sub>1</sub> | 0.002               |       | 0.006 | 0.05            |       | 0.15 |
| A <sub>2</sub> | 0.035               | 0.040 | 0.041 | 0.95            | 1.00  | 1.05 |
| b              | 0.007               | 0.009 | 0.010 | 0.17            | 0.22  | 0.27 |
| c              | 0.004               | ----- | 0.008 | 0.10            | ----- | 0.21 |
| D              |                     | 0.488 |       |                 | 12.40 |      |
| E              |                     | 0.315 |       |                 | 8.00  |      |
| H <sub>D</sub> |                     | 0.551 |       |                 | 14.00 |      |
| e              |                     | 0.020 |       |                 | 0.50  |      |
| L              | 0.020               | 0.024 | 0.028 | 0.50            | 0.60  | 0.70 |
| L <sub>1</sub> |                     | 0.031 |       |                 | 0.80  |      |
| Y              | 0.000               |       | 0.004 | 0.00            |       | 0.10 |
| $\theta$       | 0                   | 3     | 5     | 0               | 3     | 5    |

36-ball 6mm × 8mm TFBGA Package Outline Dimension



Product ID Information



\* Product ID example

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