Universal LCD Controller with Low Mux and Static LCD Driver

Features

- I^2C & 3 wires serial interface.
- Programmable multiplex rates 8, 4, 3, 2 and static.
- All segments ON by SET bit command
- All segments OFF by BLANK bit command
- Cascadable for large LCD applications
- On chip voltage bias and mux signals generation
- Internal or external oscillator
- Internal or external bias resistors
- Internal LCD bias generation with voltage-followers
- Internal or external synchronisation
- Interface with Double RAM function
- Interface with Shift register function
- High noise immunity on inputs
- Low operating current consumption
- Separate logic and LCD supply voltage pins
- Wide V_{DD} supply voltage range from 1.8V to 5V
- Wide V_{LCD} supply voltage range from 3V to 7V
- Operation temperature range: -40°C to +85°C
- Packages TQFP64, COG, COB.

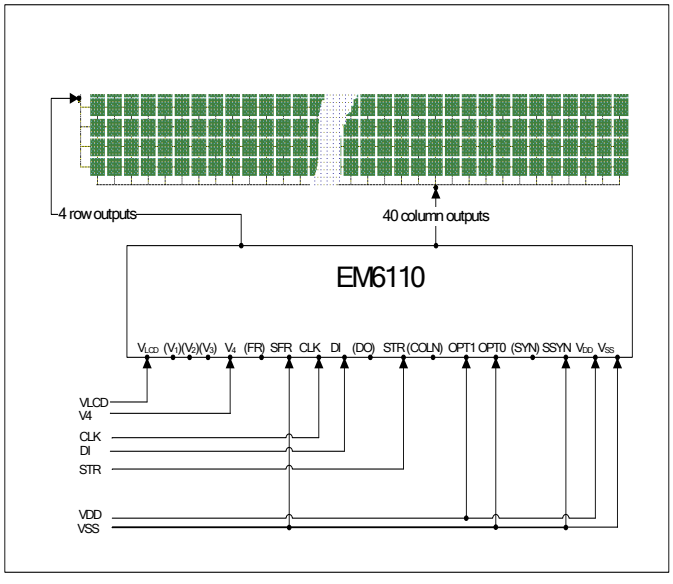
Description

EM6110 is a bit map low multiplex controller and driver for full dot matrix B/W TN and STN LCD displays. The driving capability is 8 rows x 32 columns or 4, 3, 2, 1 rows x 40 columns. The display refresh is implemented internally. The display data are entered by a 3-wire or I^2C interface.
The display data are stored in 2 selectable 8x40 RAM (Double RAM mode). The RAM data correspond directly to the LCD pixels (segments): a set bit in the RAM results in an activated LCD pixel.
EM6110 can be easily cascaded and it can be used in large display applications. The very low current consumption, the large voltage range and the wide temperature range give the EM6110 a real advantage for use in various applications.

Applications

- Industrial measuring instruments (Balances and scales, utility meters, …)
- Portable, battery operated products
- Large displays (public information panels)

Typical Operating Configuration



1 Block Diagram

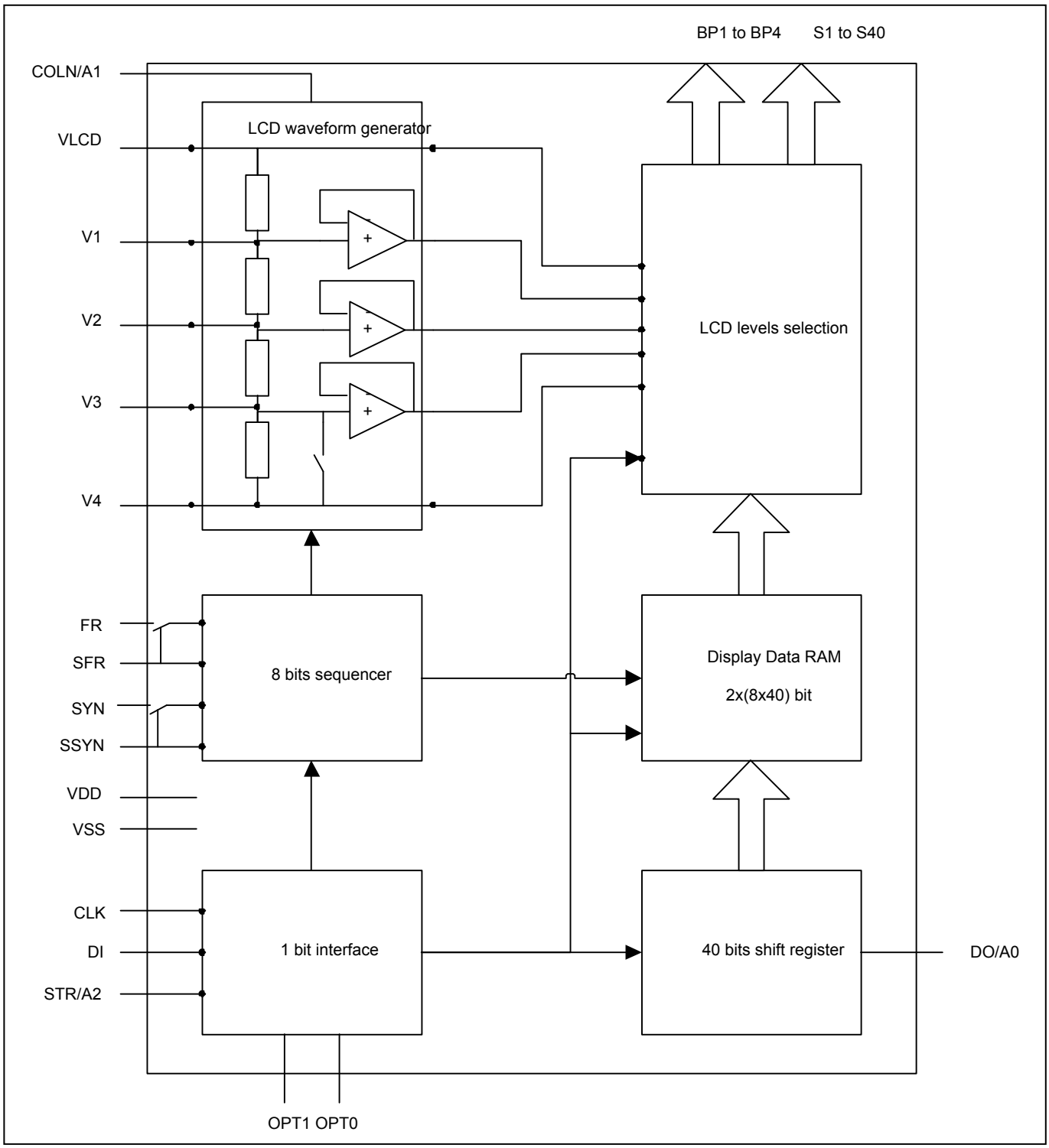
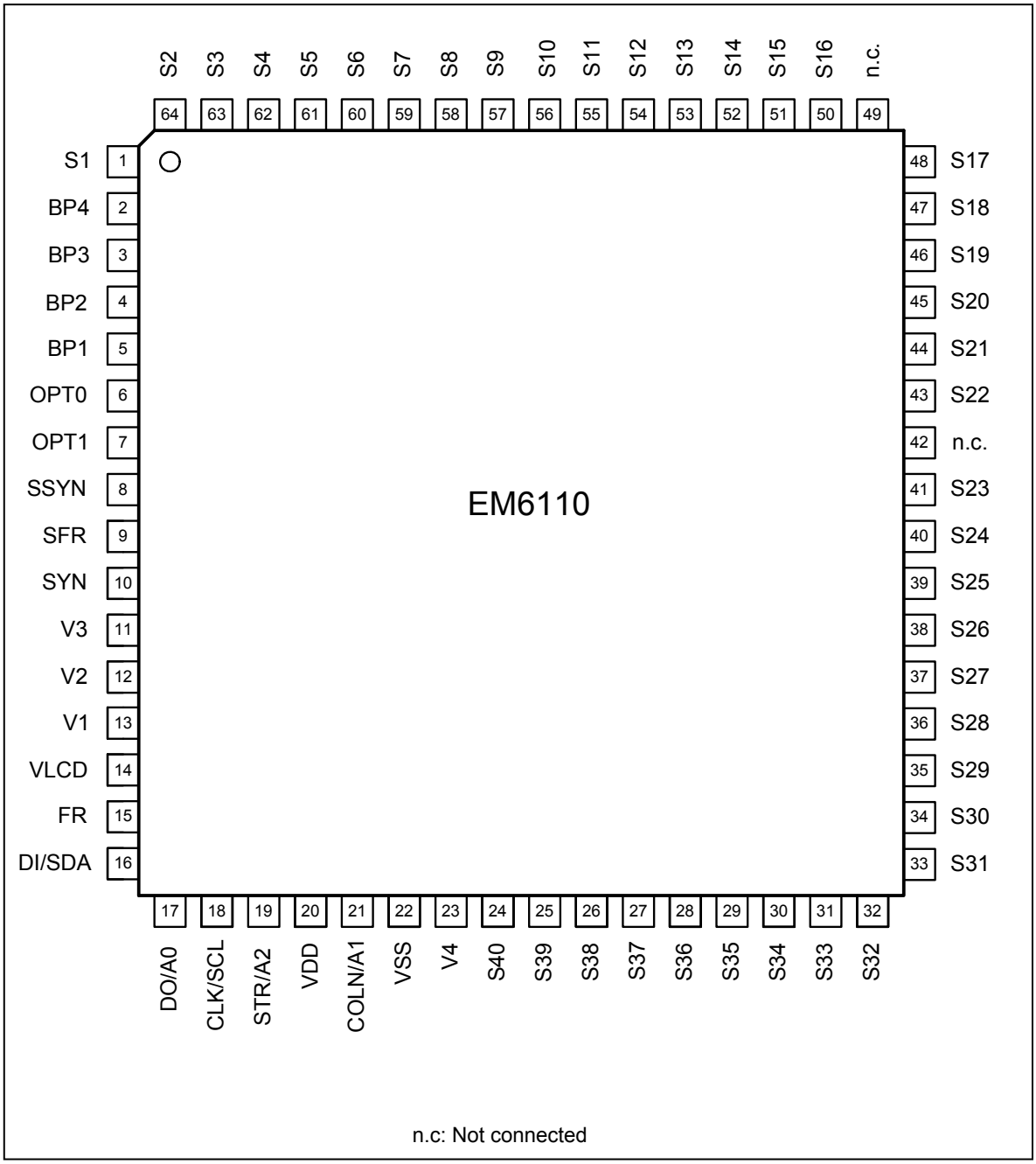


Fig. 1

2 TQFP64 Pin out



n.c: Not connected

3 Pin and Pad descriptions

Name	TQFP64	PAD	Pin Direction	Function
BP_1 to BP_4	5, 4, 3, 2	16-17	Output	Backplane outputs
S_1 to S_{40}	1, 64-50, 48-43, 41-33, 32-24	20-59	Output	Segment outputs
V_4	23	60	LCD voltage bias level V4	V4 must be externally connected to V_{SS} See Chapter 3 Operating Conditions
V_3	11	10	Input, if external bias generation Output, if internal bias generation	LCD voltage bias level V3 (Note 1)
V_2	12	9	Input, if external bias generation Output, if internal bias generation	LCD voltage bias level V2 (Note 1)
V_1	13	8	Input, if external bias generation Output, if internal bias generation	LCD voltage bias level V1 (Note 1)
V_{LCD}	14	7	Supply for display voltages	Positive power supply for the LCD See Chapter 3 Operating Conditions
V_{DD}	20	1	Supply voltage for logic part	Positive power supply See Chapter 3 Operating Conditions
V_{SS}	22	61	Ground power supply for logic part	Ground power supply See Chapter 3 Operating Conditions
CLK / SCL	18	3	Input	Data clock input
DI/SDA	16	5	Input/Output	Serial Data
DO/A0	17	4	Input/Output	Serial Data Output / A0 I2C Slave Address
COLN/A1	21	62	Input	Column Control / Blank / A1 I2C Slave Address
STR/A2	19	2	Input	Data strobe, blank, switch RAM input / A2 I2C Slave Address
FR	15	6	Input/Output	Frame Source
SFR	9	12	Input	FR selection: Select FR as internally or externally generated signal. (Note 2)
SYN	10	11	Input/Output	Synchronisation Signal Generation
SSYN	8	13	Input	SYN selection: Select SYN as internally or externally generated signal.
OPT0	6	15	Input	OPT0, OPT1: Mode selection (Refer to Table 2)
OPT1	7	14	Input	
N.C	42, 49			Not connected internally

Table 1

Note 1: Internal or external bias is set by mask
Note 2: If externally generated FR is selected, an adequate signal must be applied at FR to avoid static DC voltages at the LCD display (§9.6)

The EM6110 can be configured in 4 different interface modes by the OPT1 and OPT0 option inputs:

Mode	Max Segments	Multiplex Rate	OPT1	OPT0	See Chapter:
I2C interface	160	4	1	1	9.1 I2C Interface
	120	3			
	80	2			
	40	1			
Serial interface	160	4	1	0	9.2 Serial interface
	120	3			
	80	2			
	40	1			
Double RAM	256	8	0	1	9.4 Double RAM configuration
	144	4			
	76	2			
Shift register	40	-	0	0	9.3 Shift Register configuration

Table 2

The option inputs OPT1, OPT0 should be fixed to the selected value and remain in this state as long as the EM6110 is supplied by V_{DD} and V_{LCD}.

4 Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to GND	V_{DD}	-0.3 to + 6V
Voltage at V_{LCD} to GND	V_{LCD}	-0.3 to + 12V
All input voltages	V_{LOGIC}	-0.3 to V_{DD} + 0.3V
Voltages at BP_1 to BP_4 and S_1 to S_{40}	$V_{DISPLAY}$	-0.3 to V_{LCD} + 0.3V
Storage temperature range	T_{STO}	-65 to + 150°C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{ESD}	1000V
Maximum soldering conditions	T_{SMAX}	260°C × 10s

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

5 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS components. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

6 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Logic supply voltage	V_{DD}	1.8	5.0	5.5	V
LCD supply voltage	V_{LCD}	3.0	5.0	7.0	V
Operating temperature	T_A	-40	+25	+85	°C

7 Electrical Characteristics

Unless otherwise specified: V_{DD} = 5.0V, V_{LCD} = 7.0V, T_A = -40 to +85°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current:						
Normal LCD refresh mode	I_{LCD}	(note 1)		100		µA
Normal LCD refresh mode	I_{DD}	(note 1)		12		µA
RAM access mode	I_{DD}	(note 2)		35		µA
Inputs:						
Input leakage	I_{in}	V_{in} = GND / V_{DD}			±1	µA
Low level input voltage	V_{IL}				1.5	V
High level input voltage	V_{IH}		3.5			V
Outputs (DO, FR, SYN):						
Low level output current	I_{OL}	V_{OL} = 0.9V	1			mA
High level output current	I_{OH}	V_{OH} = 4.0V			-1	mA
LCD Outputs:						
LCD Output impedance (note 3)	R_{LCD}	I_{OUT} = 0.2mA, T_A = 25°C		1.2	2.0	KΩ
Bias voltage tolerance (note 4)	V_{bias_tol}	T_A = 25°C			± 100	mV

Table 3

Note 1: All outputs open, STR, SSYN at GND, FR = 400Hz, all other inputs at V_{DD}, Mux = 4, Checker pattern, I2C or Serial Mode

Note 2: All outputs open, STR at GND, FR = 400Hz, f_{CLK} = 1MHz, all other inputs at V_{DD}, OPT1 = 1, OPT0 = 0.

Note 3: Impedance of a BP or SEG driver; measured against V_{SS} for output levels V_{LCD}, V1 and V2 and against V_{LCD} for output levels V_{SS}, V3 and V2. The output must be driven to the appropriate level. Mux = 8; (tested at outputs BP_1, S_1 and S_{40})

Note 4: V1, V2 and V3 bias voltage levels on BP_1, S_1 and S_{40}, Mux = 8, no load
V_{bias_tol} is: $V_{bias} - V_{bias\_theor}$ (V_{bias_theor}: see §9; e.g. for V1: 0.75xV_{LCD} at Mux = 8)

8 Timing Characteristics

Unless otherwise specified: V_{DD} = 5.0V, V_{LCD} = 7.0V, T_A=-40 to +85°C

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Internal frame frequency for LCD refresh	f_{FR}	(note 1)		64 x mux		Hz
I2C timing characteristics						
SCL frequency	f_{I2C}				400	kHz
SCL low period	t_{LOW}		600			ns
SCL high period	t_{HIGH}		1000			ns
SDA setup time	t_{SUDAT}		150			ns
SDA hold time	t_{HDDAT}		300			ns
SCL and SDA rise time	t_R				200	ns
SCL and SDA fall time	t_F				200	ns
Setup time for a repeated start condition	t_{SUSTA}		200			ns
Hold time for a start condition	t_{HDSTA}		150			ns
Setup time for a stop condition	t_{SUSTO}		300			ns
Spike width on SCL and SDA	t_{SW}				10	ns
Time before a new transmission can start	t_{BUF}		1000			ns
Serial bus timing characteristics						
CLK frequency	f_{CLK}				4	MHz
CLK low period	t_{CL}		50			ns
CLK high period	t_{CH} (note 2)		100			ns
CLK and FR rise time	t_{CR}	FR is input			100	ns
CLK and FR fall time	t_{CF}	FR is input			100	ns
DI setup time	t_{DS}		50			ns
DI hold time	t_{DH}		50			ns
DO output propagation	t_{PD}	C_{LOAD}=50pF			150	ns
STR pulse width	t_{STR}		100			ns
CLK falling to STR rising	t_P		50			ns
STR falling to CLK falling	t_D		300			ns

Table 4

Note 1: Measured on pin FR, SFR = VSS (config. FR as output)
Note 2: For cascade function: $t_{CH} > t_{PD} + t_{DS}$

8.1 Serial interface timing Waveforms

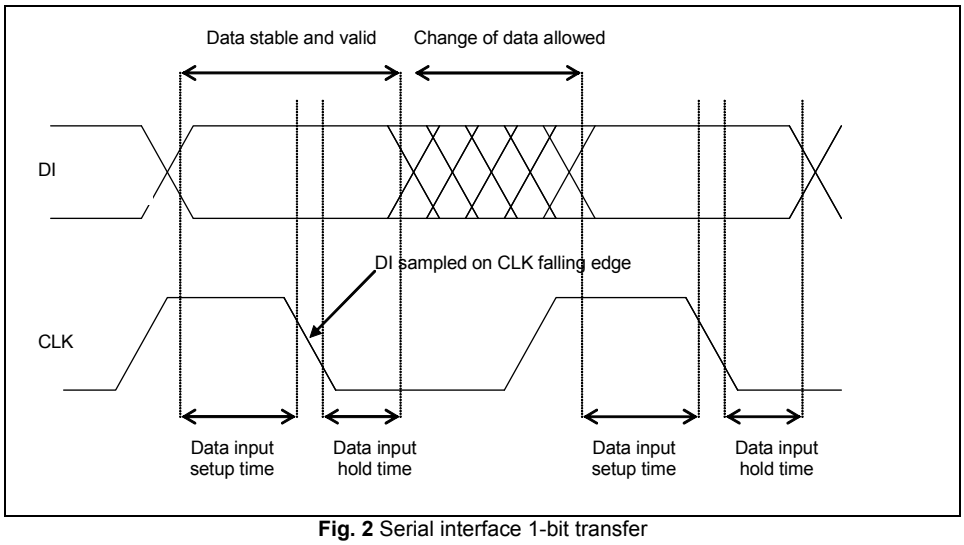


Fig. 2 Serial interface 1-bit transfer

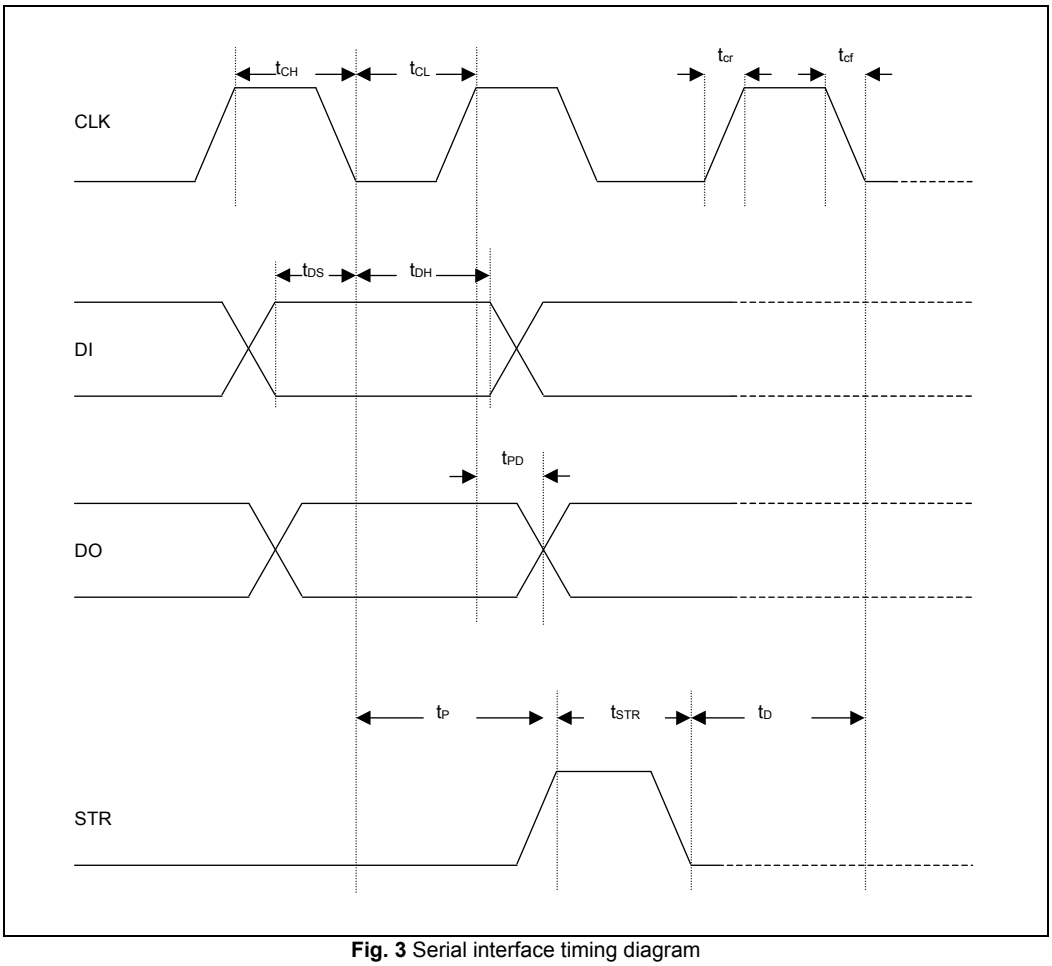


Fig. 3 Serial interface timing diagram

8.2 I2C interface timing Waveforms

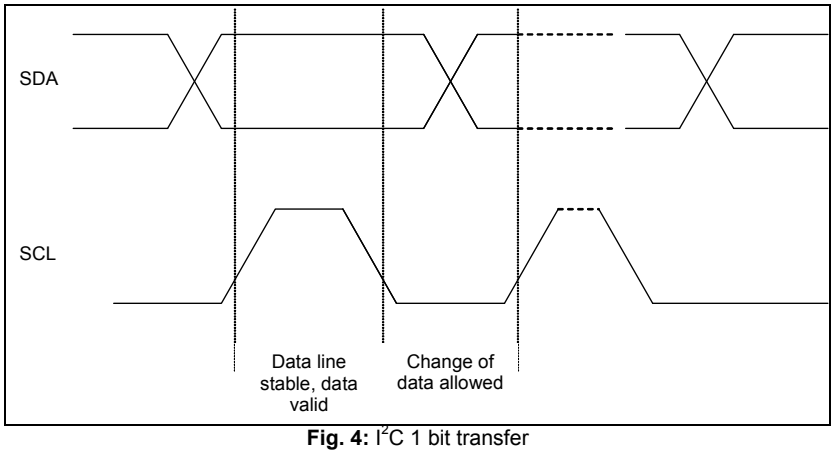


Fig. 4: I²C 1 bit transfer

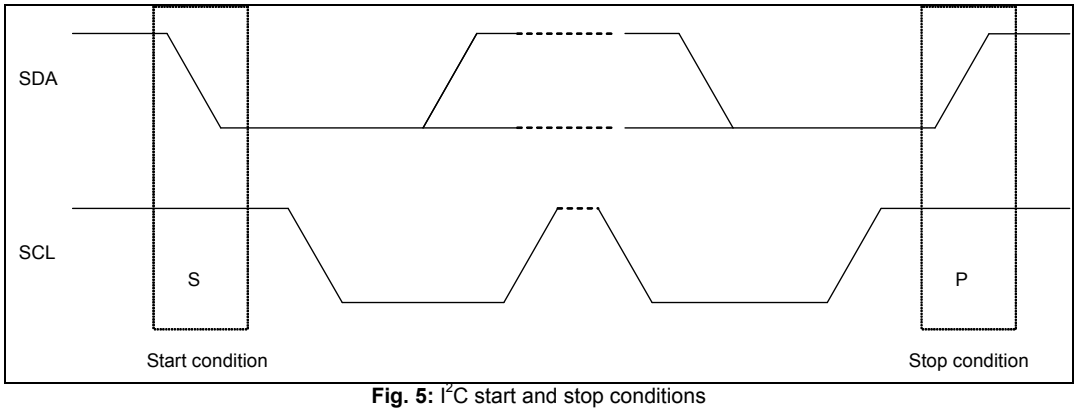


Fig. 5: I²C start and stop conditions

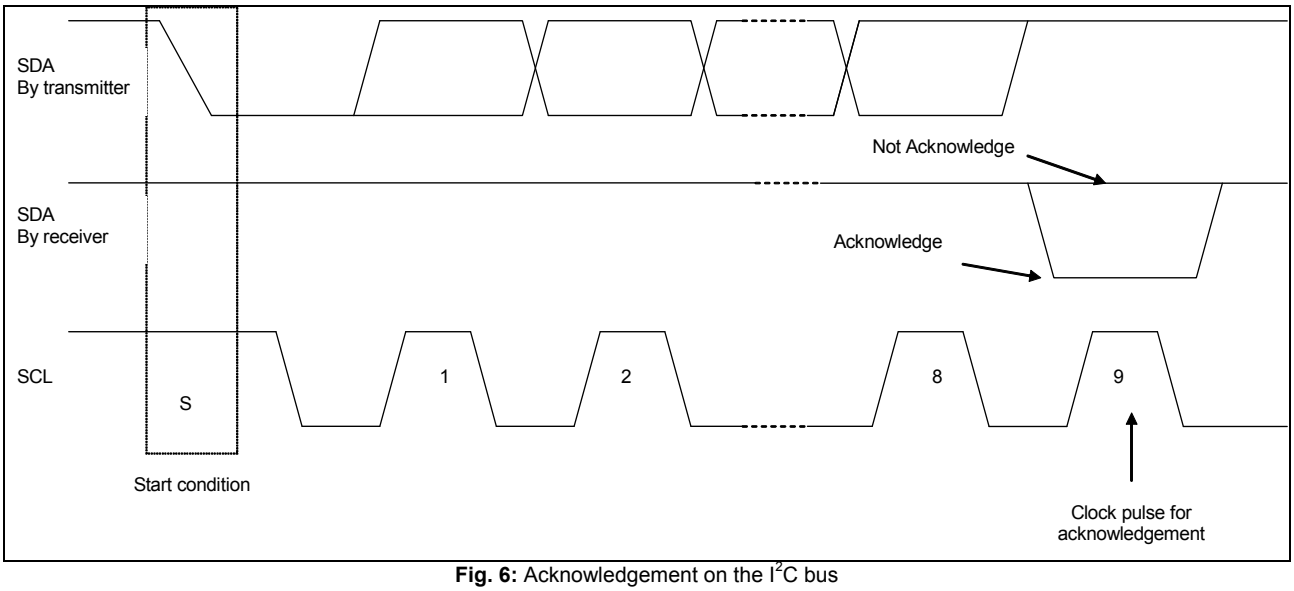


Fig. 6: Acknowledgement on the I²C bus

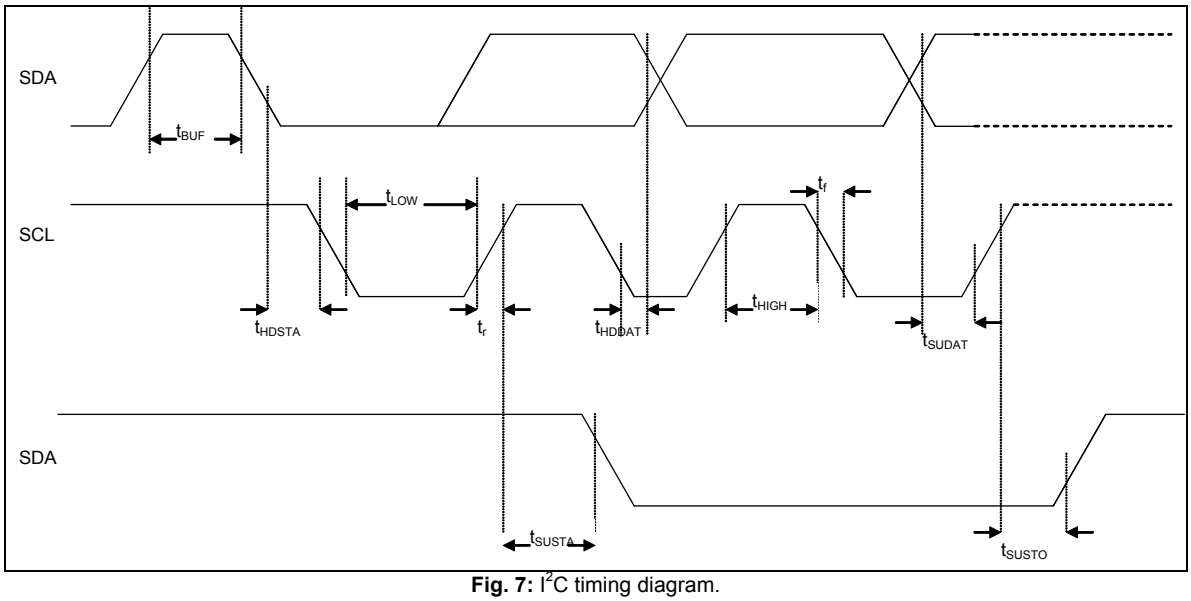


Fig. 7: I²C timing diagram.

9 Functional Description

9.1 I²C Interface

9.1.1 Pin assignment

Pad Name	Function	Pin Direction
BP_1 to BP_4	Row1 to Row4	Backplane / Row output
S_1 to S_{40}	Col1 to Col40	Segment / Col output
V_4	LCD voltage bias level	V_4 must be externally connected to V_{SS}, See chapter 6
V_3	LCD voltage bias level V3	Input, if external bias generation Output, if internal bias generation
V_2	LCD voltage bias level V2	Input, if external bias generation Output, if internal bias generation
V_1	LCD voltage bias level V1	Input, if external bias generation Output, if internal bias generation
V_{LCD}	LCD supply voltage	See chapter 6
V_{DD}	Supply voltage for logic part	See chapter 6
GND = V_{SS}	Ground power supply for logic part	See chapter 6
CLK = SCL	Clock input	Input
DI = SDA	Serial data input /output	Input / Output
A0 (DO)	I2C slave address	Input
A1 (COLN)	I2C slave address	Input
A2 (STR)	I2C slave address	Input
FR	Frame signal	Input if SFR=1 Output it SFR=0
SFR	Frame generation selection *0= Internal FR generation* *1= External FR generation*	Input
SYN	Synchronisation Signal	Input if SSYN=1 Output it SSYN=0
SSYN	SYN generation selection *0= Internal SYN generation* *1 = External SYN generation*	Input
OPT1	Option input to set the interface mode	1
OPT0	Option input to set the interface mode	1

Table 5

9.1.2 General

The EM6110 has an I²C slave interface, which is activated by the setting of the option pins OPT1=1 and OPT0=1. The pin CLK is then the I²C SCL serial clock input and the pin DI is the I²C SDA serial data input or output.
According to the I²C definition, the pin SDA (DI) has an open drain transistor. An external pull up element has to be used acc. the I²C definition.
The EM6110 I²C interface implements the functions: initialisation, RAM write and status read.
The EM6110 slave address is defined by 7 bits: A2,A1,A0,0,0,1,0. (A2 is at the pin STR, A1 at the pin COLN, A0 at the pin DO, when the I²C mode is activated).
As the first byte sent by an I²C master is the slave address, the EM6110 will acknowledge, if the address is correct (pulling SDA down during the 9th clock SCL).
The 8th bit of the first byte sent (=R/W) defines the function Read/Write of the EM6110: if at 0, the I²C master writes data to the EM6110, if at 1, the I²C master reads data from EM6110 (read the status byte, which is the data of the control byte sent before at initialisation 0.

The I2C slave address (first byte to be sent) is defined as shown:

A2	A1	A0	0	0	1	0	RW

RW: 0: EM6110 receives data
1: EM6110 outputs the status byte (see 9.1.2.5)

9.1.2.1 Start and stop conditions

Data transfer begins by a falling edge on SDA when SCL is at high level, this is the start condition (S), initiated by the I^2C bus master. It is stopped with a rising edge on SDA and SCL at high level, this is the stop condition (P) (see Fig. 5: I2C start and stop conditions).

9.1.2.2 Bit transfer

One data bit is transferred during each SCL pulse. The data on the SDA input must remain stable during the high period of SCL pulse, as any changes at this time would be interpreted as start or stop conditions. Data is always transfered with MSB first.

9.1.2.3 Acknowledge

After a start condition, data bits are transfered to EM6110. Each byte is followed by an acknowledge bit: the master lets the SDA line high (no pull down) and generates an SCL pulse; if transfer concerns the EM6110 slave receiver and has performed correctly, the EM6110 generates a low SDA level (pull down activated). SDA remains stable during the high period of the acknowledge related SCL pulse. After acknowledge, EM6110 lets SDA line free, enabling the transmitter to continue transfer or to generate a stop condition.

9.1.2.4 Write mode

If the RW bit of the first byte after start is at 0, the EM6110 receives data from the master.

Data can be control bytes, command bytes or data bytes. Data transfer always begins with a control byte. This sets the bits C_0, DC (see Fig. 9).

C_0 is the continuation bit:

- If C_0 = 1, the control byte is followed by 1 data byte only, the next byte is a new control byte.
- If C_0 = 0, all the following bytes are data bytes until data transfer is stopped.

The bit DC selects data bytes or command bytes to be send after the control byte:

- If DC = 1, the following byte is a data byte written into the Display Data RAM.
  First data byte is stored at the address specified by the x-address and y-address pointers. Data pointers are automatically updated for each byte written in the DDRAM (see 9.1.4 DDRAM Architecture).
- IF DC = 0, the following data byte is a command byte. It enables initialisation of functions (multiplex rate, Blank, Set, x-address and y-address).

With bit Ini[0] of the control byte, one of the two initialisation registers can be selected.

9.1.2.5 Read Mode (RW = 1)

The EM6110 will output the status byte in this case after the slave address is transmitted. This status byte consists in the 8 initialisation bits, previously set by a command byte or by the reset cycle (see **Fig. 9 Instructions for I2C**).

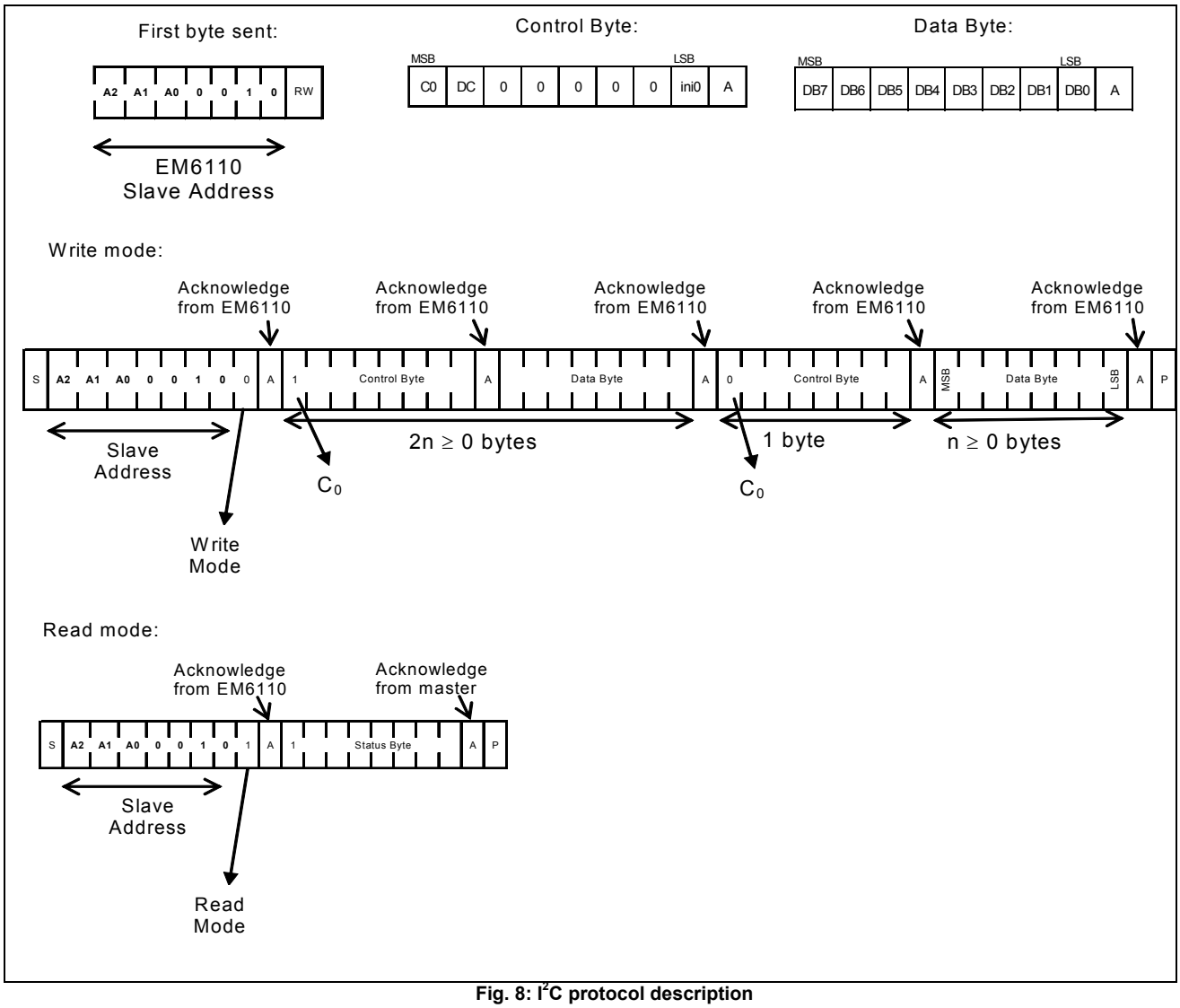


Fig. 8: I²C protocol description

9.1.3 Initialisation

Data loaded in EM6110 can be divided in two parts:

- The bits stored in the DDRAM, which are corresponding to LCD pixels.
- The command bits, which are stored in registers and used to set functions of the LCD controller.

The organisation of these bits is described in Fig. 9 below:

	Instruction	RW	Control Byte								Data Byte								Description
			CO	DC	0	0	0	0	0	ini[0]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Initialisation of functions	Initialisation 0	0	1	0	0	0	0	0	0	0	Blank	Set	Y Add0	Y Add1	0	0	Mux1	Mux0	Blank and Set functions Line address Mux mode DB3 and DB2 must be set to 0
	Initialisation 1	0	1	0	0	0	0	0	0	1	X Add0	X Add1	X Add2	0	0	0	0	0	Bank address DB4 to DB0 must be set to 0
Write DDRAM	Write 1 byte in DDRAM	0	1/0	1	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Write data byte to the Display Data Ram
Read Status	Read 1 byte in initialisation	1	-	-	-	-	-	-	-	-	Blank	Set	Y Add0	Y Add1	0	0	Mux1	Mux0	Read Status Byte from EM6110 Status Byte = initialisation 0 using I²C interface

Fig. 9 Instructions for I2C

9.1.3.1 Description of instructions

9.1.3.1.1 BLANK

The BLANK bit forces all column outputs to V_{SS}. The consequence is that the display is OFF.
The BLANK bit is active at logic 1 level. The BLANK function has priority over the SET function.

9.1.3.1.2 SET

The SET bit forces all column outputs ON.
The SET bit is activated when at logic 1 level.

9.1.3.1.3 Y-Address

These two bits of Initialisation 0 set the address of the RAM acc. Table 5:

RAM y-address	Add1	Add0	Mux 4	Mux 3	Mux 2	Mux 1
1	0	0	Row1	Row1	Row1	Row1
2	0	1	Row2	Row2	Row2	
3	1	0	Row3	Row3		
4	1	1	Row4			
	DB4	DB5				

Table 6

9.1.3.1.4 Mux Mode

These two bits of Initialisation 0 set the multiplex rate acc. Table 6: (Mux = 1 is static mode, Mux = 8 only in Double RAM mode)

Mux Mode	Mux1	Mux0
4	1	0
3	0	1
2	0	0
1	1	1
	DB1	DB0

Table 7

9.1.3.1.5 X-Address

These three bits of Initialisation 1 set the bank address of the RAM acc. Table 7: (see also Fig. 10 … 13)

RAM x-address BANK	X Add2	X Add1	X Add0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
	DB5	DB6	DB7

Table 8

9.1.4 DDRAM Architecture

The EM6110 contains a RAM, which stores the display data; there is direct correspondence between the bits stored in the RAM and LCD pixels.

The DDRAM ("Display Data RAM") consists in a RAM of 4 x 40 bits, corresponding to

- 4 rows
- 40 columns

The DDRAM is read row by row for display refresh. Each row corresponds to one output, which is activated when the corresponding row is read.

In this mode, the DDRAM is written via the I²C interface. Data are stored in the position of the RAM defined by X-Address and Y-Address in the initialisation 0 and initialisation 1 bytes. In Mux 1 mode the address is assigned automatically to Row1.

The table 8 below represents the allowed addresses and their assigned rows for different Mux mode selections:

	Selected Row of the DDRAM			
y-address	Mux mode 4	Mux mode 3	Mux mode 2	Static
00	1	1	1	1
01	2	2	2	
10	3	3		
11	4			

Table 9

If **Mux Mode = 4, 3, 2 or 1**, the DDRAM provides 4, 3, 2 or 1 rows and 40 columns. The DDRAM is divided in 5 banks as shown in figures below. Each pixel in the display corresponds to 1 bit in the RAM.

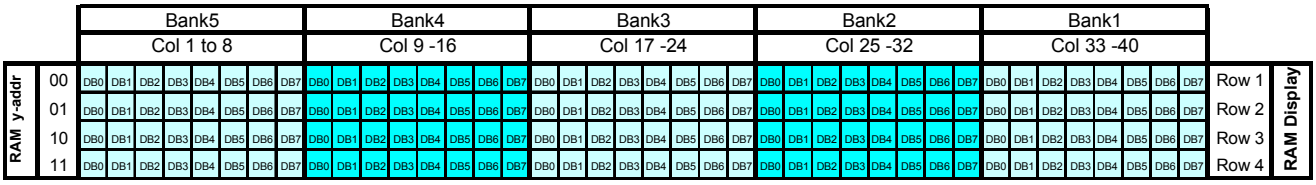


Fig. 10 DDRAM with Mux Mode = 4

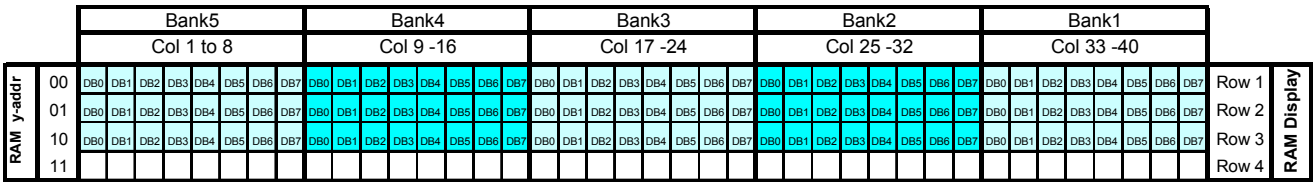


Fig. 11 DDRAM with Mux Mode = 3

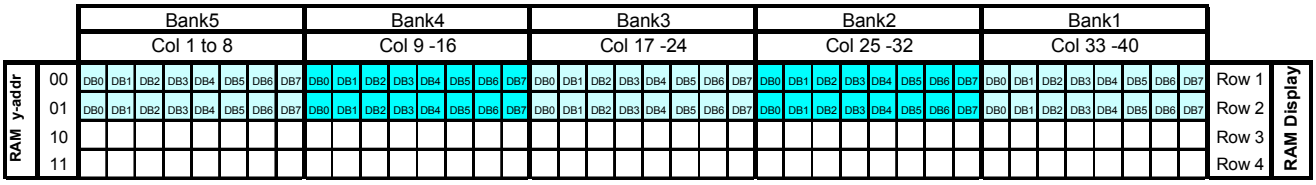


Fig. 12 DDRAM with Mux Mode = 2

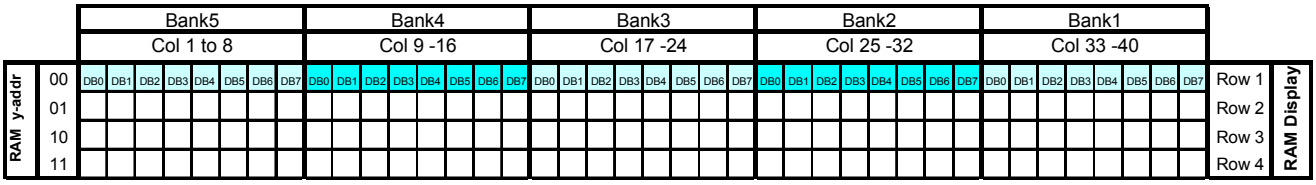


Fig. 13 DDRAM with Mux Mode = 1

9.1.4.1 DDRAM addressing

The X-Address and the Y-Address pointers are used to address RAM cells. They are set by instructions “initialisation 0” and “initialisation 1”. As EM6110 offers 4 digitally programmable multiplex rates, number of row drivers is not fixed.

As DDRAM is an image of the LCD display, address ranges also depend on multiplex rate (Mux Mode):

- If Mux Mode = 4: 000b ≤ x-address ≤ 100b
  00b ≤ y-address ≤ 11b
- If Mux Mode = 3: 000b ≤ x-address ≤ 100b
  00b ≤ y-address ≤ 10b
- If Mux Mode = 2: 000b ≤ x-address ≤ 100b
  00b ≤ y-address ≤ 01b
- If Mux Mode = 1: 000b ≤ x-address ≤ 100b
  y-address = 00b

Addresses outside these ranges are not allowed.

When writing data into the DDRAM, if DC=1, the X-Address increments after each byte written into the RAM. After the last X-Address, the X-Address is reset to 1 and the Y-Address increments.

The table below represents the next address select after pointers are in the last allowed address:

Mux Mode	Last allowed address		Next address	
	x-address	y-address	x-address	y-address
4	5	4	1	1
3	5	3	1	1
2	5	2	1	1
1	5	1	1	1

Table 10

The following tables represent the way that the pointers X-Address and Y-Address are working according to the setting of the Mux Mode:

Mux 4:

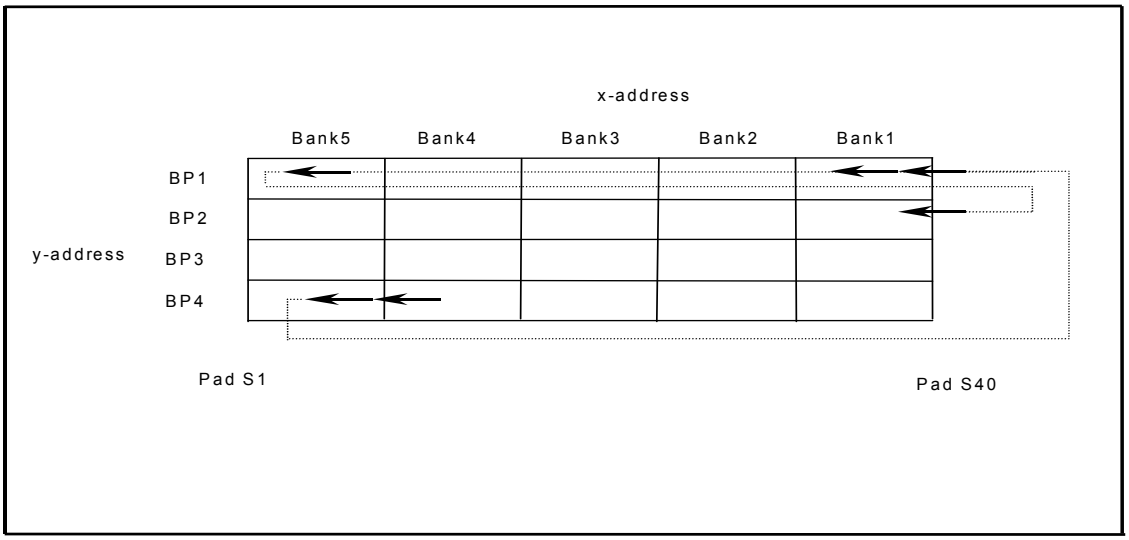


Fig. 14

(I^2C Mode Description)

Mux 3:

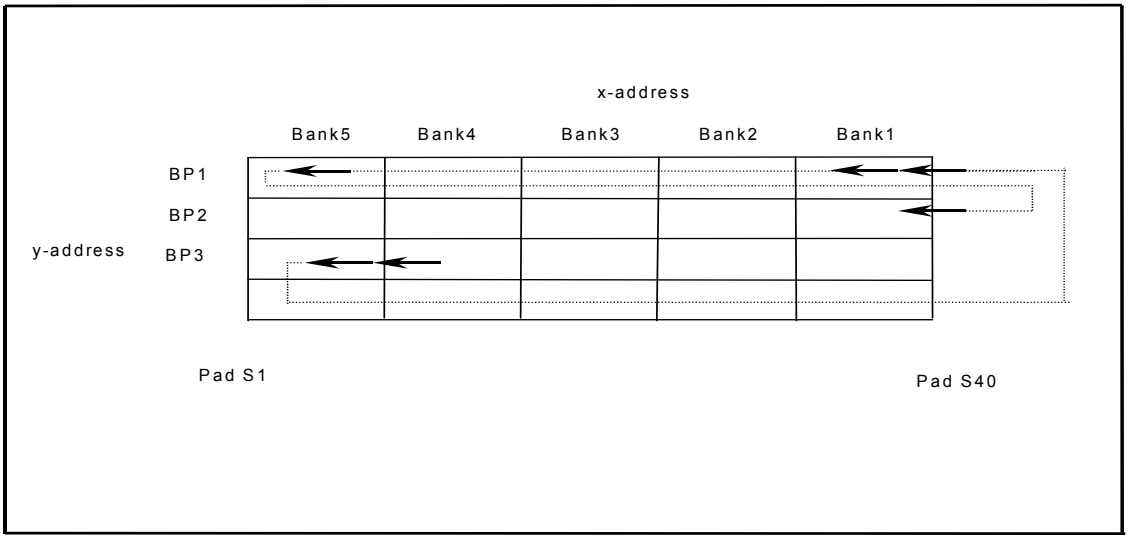


Fig. 15

Mux 2:

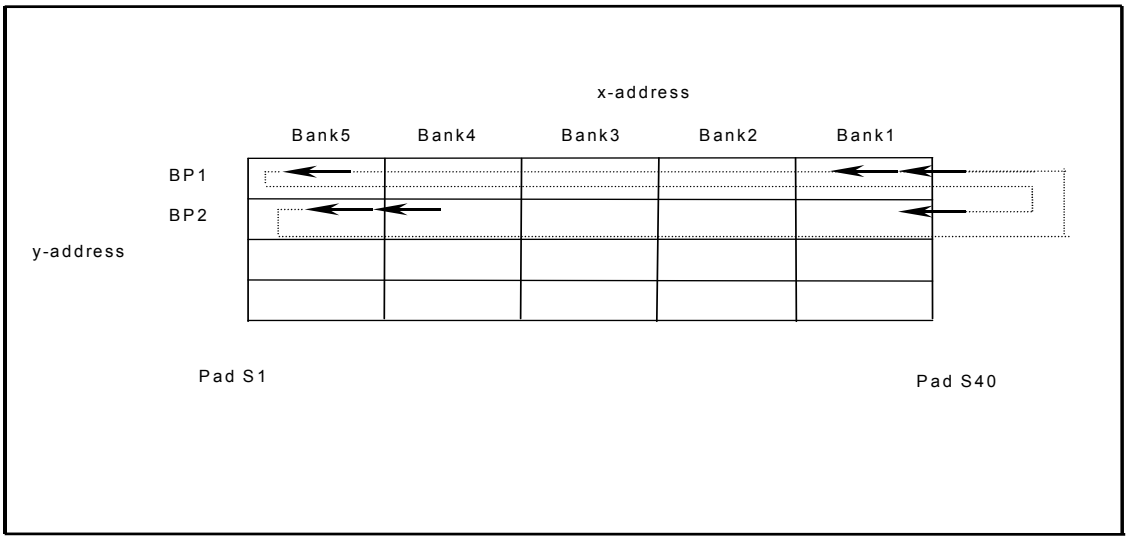


Fig. 16

Static:

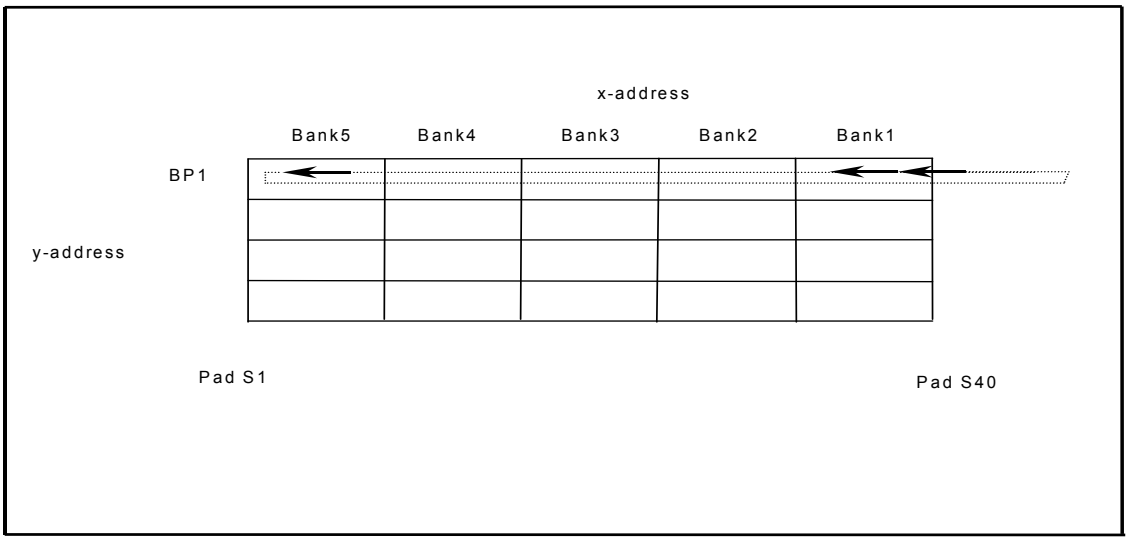


Fig. 17

9.1.4.2 Row selection

Depending on the selected Mux mode, the BP outputs are connected to the rows of the DDRAM as shown in the table 10:

Mux Mode	BP1	BP2	BP3	BP4
4	Row1	Row2	Row3	Row4
3	Row1	Row2	Row3	Row1
2	Row1	Row2	Row1	Row2
1	Row1	Row1	Row1	Row1

Table 11

This allows the possibility to increase current capability of BP pads by connecting pads which supply the same signal together.

9.1.5 Power on Reset

In I2C mode, the Power On Reset function of the EM6110 is active. The circuit is reset to the following starting condition:

- BP1 to BP4 outputs are set to V_{ss}.
- All segment outputs S1 to S40 are set to V_{ss}.
- The I2C- interface is initialised.
- Y-Address and X-Address registers are initialised to 00b and 000b respectively.

The segment and backplane outputs start working after the first initialisation, independently of internal or external FR mode or multiplex setting.

(I²C Mode Description)

9.1.6 Cascading

In large display configurations, up to 8 EM6110 can be addressed on the same I²C-bus by using 3 inputs (A0, A1 and A2) as programmable I²C-bus slave address. In this configuration DO, COLN and STR pads are used in the function of address as in the table bellow:

Slave address Pads	Corresponding pad name in others options
A0	DO
A1	COLN
A2	STR

Table 12

In cascaded applications, one EM6110 has to provide the backplane signals (BP1 to BP4) to drive the rows of the display and the other drivers will act as pure column drivers (see Fig below). When cascading devices, all SCL lines should be tied together and all SDA should be tied together. Only one of the LCD drivers in the cascaded group must define the frame frequency, with its FR as output. In this case all FR lines must be tied together.

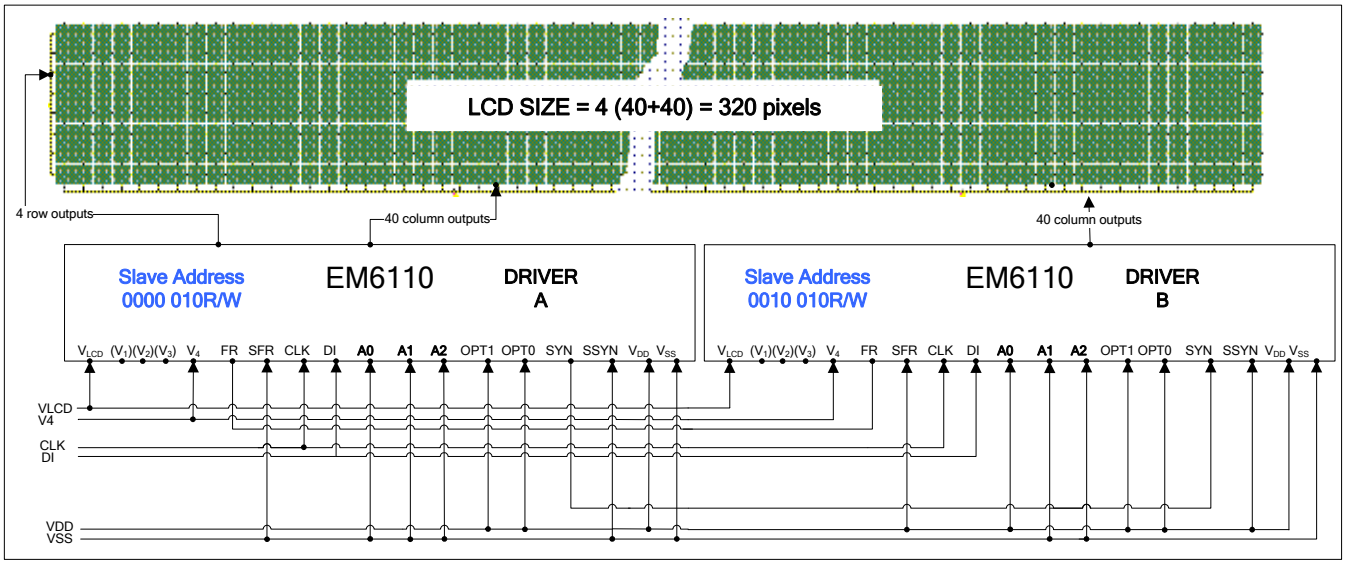


Fig. 18: Example of two cascaded LCD drivers in Mux mode 4 with two EM6110

Note1
In a system with several EM6110 cascaded, only one EM6110 with SFR=0 is allowed. In other case differences in the frequency of the LCD drivers could create bad synchronisation in the display.

Note2
When cascading EM6110s, only one EM6110 with SSYN=0 is allowed. Only one driver generates the synchronisation.

Note3
When cascading EM6110s never combine one mux mode with another. If an EM6110 mux mode 4 is used to drive the rows, then only EM6110s mux mode 4 can be cascaded with it.

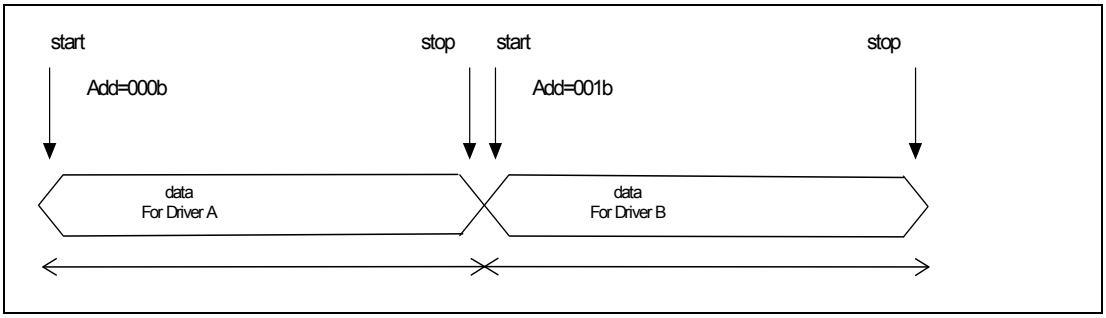
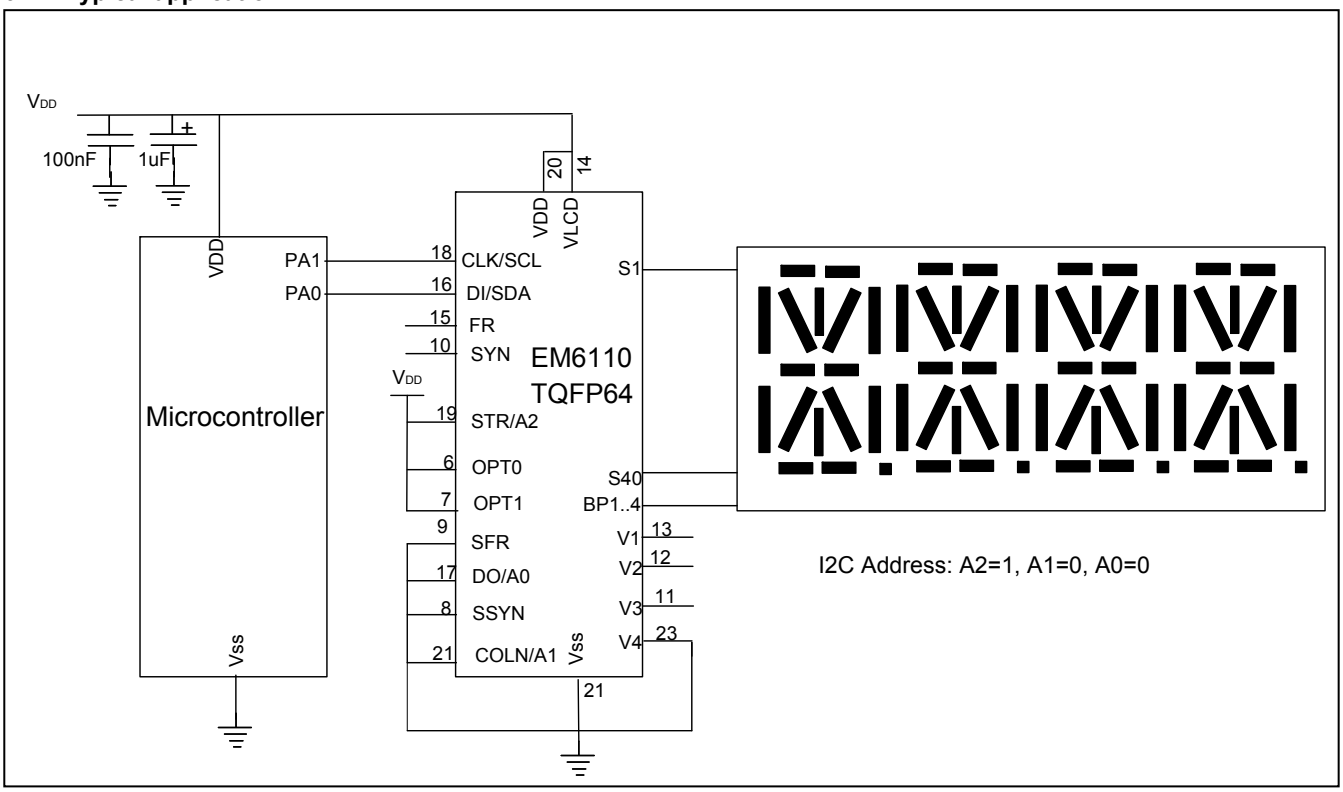


Fig. 19

Note4: For synchronisation see chapter 9.5 Synchronisation

(I²C Mode Description)

9.1.7 Typical application



(Serial Mode Description)

9.2 Serial interface

9.2.1 Pin assignment

Pad Name	Function	Pin Direction
BP_1 to BP_4	Row1 to Row4	Backplane / Row Output
S_1 to S_{40}	Col1 to Col40	Segment / Column Output
V_4	LCD voltage bias level	V_4 must be externally connected to V_{SS}, See chapter 6
V_3	LCD voltage bias level V3	Input, if external bias generation Output, if internal bias generation
V_2	LCD voltage bias level V2	Input, if external bias generation Output, if internal bias generation
V_1	LCD voltage bias level V1	Input, if external bias generation Output, if internal bias generation
V_{LCD}	LCD supply voltage	See chapter 6
V_{DD}	Supply voltage for logic part	See chapter 6
GND = V_{SS}	Ground power supply for logic part	See chapter 6
CLK	Serial clock input	Input
DI	Serial data input	Input
DO	Serial data output	Output
COLN	Not used	Connect to V_{DD}
STR	Data strobe	Input
FR	Frame signal	Input if SFR=1 Output it SFR=0
SFR	Frame generation selection *0= Internal generation* *1= External generation*	Input
SYN	Synchronisation Signal	Input, if SSYN=1 Output, it SSYN=0
SSYN	SYN generation selection *0= Internal generation* *1 = External generation*	Input
OPT1	Option input to set the interface mode	1
OPT0	Option input to set the interface mode	0

Table 13

9.2.2 Protocol

The serial interface mode implements a 3-wire data transmission protocol with the signals Serial Clock CLK, Data Input DI and Strobe STR.
The data transfer is enabled, when STR is at low level. STR must be hold at low level during the transfer. After the last bit has been transferred, a positive pulse at STR stops the transmission and latches the shifted data into EM6110 internal registers or RAM with its negative edge.

The information at the data input DI is shifted into the LCD driver at CLK falling edge, data word length is 48 bit. The transfer begins with the column data, this means 40 bit and finishes with the command byte of 8 bit.

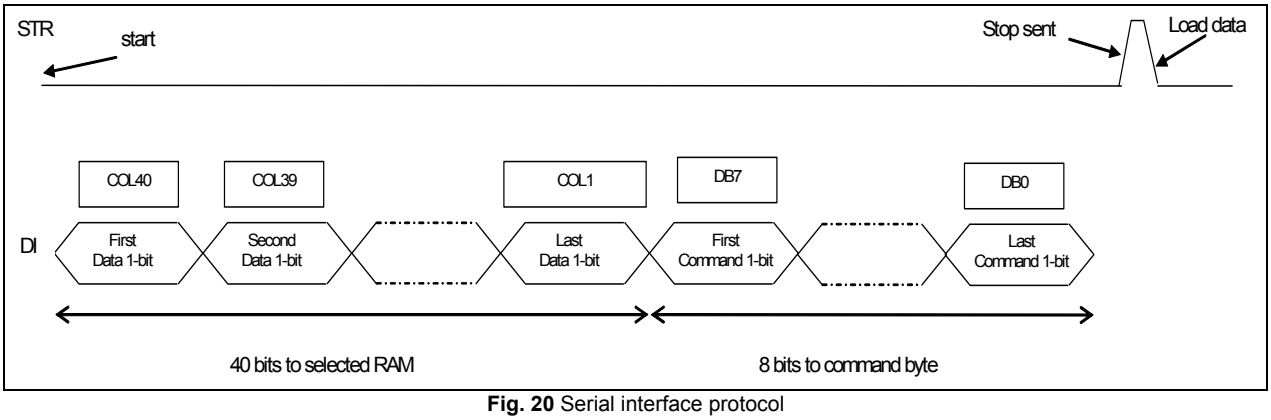


Fig. 20 Serial interface protocol

Column data is transfered with MSB bit first, setting data for COL_{40}, until LSB bit, setting data for COL_1

The column data is organised as shown in Fig.21:

MSB-first											LSB-last
data1	data2	data3	data4	data5	data6	data7	…	…	…	…	data40
COL40	COL39	COL38	COL37	COL36	COL35	COL34	…	…	…	…	COL1
40-bits											

Fig. 21

The command byte data is organised as shown in Fig.22:

MSB-first							LSB-last
Blank	SET	Add0	Add1	0	0	Mux1	Mux0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
8 bits							

Fig. 22

9.2.3 Initialisation

To initialise the EM6110 to execute the intended functions, the corresponding bits in the command byte have to be set to define the BLANK or SET function, to set the RAM address and to define the Mux mode. (Refer to Fig. 22)

9.2.3.1 Detailed Description of command bits

9.2.3.1.1 BLANK

With a logic 1 level, the BLANK bit forces all column outputs to V_{SS}, so that the display is OFF.
The BLANK function has priority over the SET function.

9.2.3.1.2 SET

The SET bit forces all column outputs ON, if it is activated with a logic 1 level.

9.2.3.1.3 Y-Address

These two bits (bit5 and bit4 of the command byte) set the Y-Address of the DDRAM, acc. Table 13:

RAM Y-Address	Add1	Add0	Mux 4	Mux 3	Mux 2	Static
1	0	0	Row1	Row1	Row1	Row1
2	0	1	Row2	Row2	Row2	
3	1	0	Row3	Row3		
4	1	1	Row4			
	DB4	DB5				

Table 14

9.2.3.1.4 Mux Mode

The bits 1 and 0 of the command byte set the multiplex, see Table 14:

Mux Mode	Mux1	Mux0
4	1	0
3	0	1
2	0	0
1	1	1
	DB1	DB0

Table 15

9.2.4 DDRAM Architecture

(General description of the DDRAM: see I2C mode, page 14)

In this mode, the DDRAM is written via the Serial interface. Data are stored in the position of the RAM defined by the Y-Address in the initialisation byte. In Mux 1 mode, the address is assigned automatically to Row1.

The Table 15 below represents the allowed addresses and their assigned rows for different Mux mode selections:

	Selected Row of the DDRAM			
y-address	Mux mode 4	Mux mode 3	Mux mode 2	Static
00	1	1	1	1
01	2	2	2	
10	3	3		
11	4			

Table 16

If **Mux Mode = 4, 3, 2 or 1**, the DDRAM provides 4, 3, 2 or 1 rows and 40 columns. The DDRAM is divided in 5 banks as shown in figures below. Each pixel in the display corresponds to 1 bit in the RAM.

		Col 1	Col 2	Col 3	Col 4		Col 37	Col 38	Col 39	Col 40		
RAM y-address	00	data40	data39	data38	data37		data4	data3	data2	data1	Row 1	RAM Display
	01	data40	data39	data38	data37		data4	data3	data2	data1	Row 2	
	10	data40	data39	data38	data37		data4	data3	data2	data1	Row 3	
	11	data40	data39	data38	data37		data4	data3	data2	data1	Row 4	

Fig. 23 DDRAM description with Mux Mode = 4

		Col 1	Col 2	Col 3	Col 4		Col 37	Col 38	Col 39	Col 40		
RAM y-address	00	data40	data39	data38	data37		data4	data3	data2	data1	Row 1	RAM Display
	01	data40	data39	data38	data37		data4	data3	data2	data1	Row 2	
	10	data40	data39	data38	data37		data4	data3	data2	data1	Row 3	
	11										Row 4	

Fig. 24 DDRAM description with Mux Mode = 3

		Col 1	Col 2	Col 3	Col 4		Col 37	Col 38	Col 39	Col 40		
RAM y-address	00	data40	data39	data38	data37		data4	data3	data2	data1	Row 1	RAM Display
	01	data40	data39	data38	data37		data4	data3	data2	data1	Row 2	
	10										Row 3	
	11										Row 4	

Fig. 25 DDRAM description with Mux Mode = 2

		Col 1	Col 2	Col 3	Col 4		Col 37	Col 38	Col 39	Col 40		
RAM y-address	00	data40	data39	data38	data37		data4	data3	data2	data1	Row 1	RAM Display
	01										Row 2	
	10										Row 3	
	11										Row 4	

Fig. 26 DDRAM description with Mux Mode = 1

9.2.4.1 DDRAM addressing

The Y-Address pointer is used to address the RAM cells. As EM6110 offers 4 programmable multiplex rates, the number of row drivers is not fixed.

As DDRAM is an image of LCD display, address ranges also depend on multiplex rate (Mux Mode):

- If Mux Mode = 4: 00b ≤ y-address ≤ 11b
- If Mux Mode = 3: 00b ≤ y-address ≤ 10b
- If Mux Mode = 2: 00b ≤ y-address ≤ 01b
- If Mux Mode = 1: y-address = 00b

Addresses outside these ranges are not allowed.

9.2.4.2 Rows selection

Depending on the selected Mux mode, the BP outputs correspond to the rows of the RAM as shown in the Table 16:

Mux Mode	BP1	BP2	BP3	BP4
4	Row1	Row2	Row3	Row4
3	Row1	Row2	Row3	Row1
2	Row1	Row2	Row1	Row2
1	Row1	Row1	Row1	Row1

Table 17

This offers the possibility to increase the current capability of BP pads by connecting the pads whith the same signal together.

9.2.5 Power on Reset

In Serial mode, the Power On Reset function of the EM6110 is active. The circuit is reset to the following starting condition:

- BP1 to 4 outputs are set to V_{ss}.
- All segments outputs S1 to S40 are set to V_{ss}.
- Y-Address register is initialised to 00b.

The segment and backplane outputs start working after the first initialisation, independently of internal or external FR mode or multiplex setting.

9.2.6 Cascading

In cascaded applications, one EM6110 has to provide the backplane signals (BP1 to BP4) to drive the rows of the display and the other drivers will act as pure column drivers (see Fig below). When cascading devices, all CLK, DI, STR should be tied together. Only one of the LCD drivers in the cascaded group must define the frame frequency, with its FR as output. In this case all FR lines must be tied together.

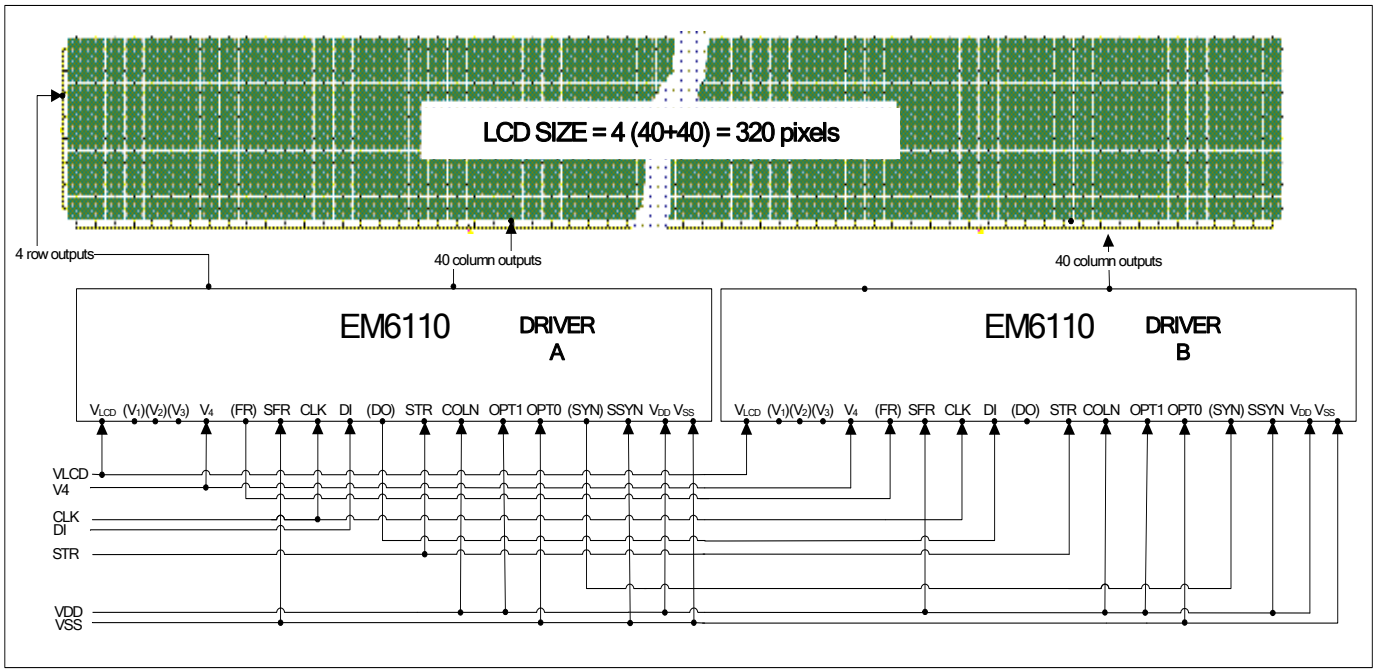


Fig. 27 : Example of two cascaded LCD drivers in Mux mode 4

Note1

In a system with several cascaded EM6110, only one EM6110 with SFR=0 is allowed. In other case differences in the frequency of the LCD drivers could create bad synchronisation in the display.

Note2

When cascading EM6110s, only one EM6110 with SSYN=0 is allowed. Only one driver generates the synchronisation.

Note3

When cascading EM6110s, never cascade one mux mode with another. If e.g. an EM6110 with Mux mode 4 is used to drive the rows, then only EM6110s Mux mode 4 can be cascaded with it.

(Serial Mode Description)

The data output pin, DO, is used in cascaded applications to transfer the data to the next cascaded chip DI input.

(The data at DO corresponds to the data at DI delayed by 48 clock periods.)

To cascade EM6110 circuits, the DO of one chip must be connected to DI of the following chip. The 48 bit data for the last EM6110 (DO is not connected) must be entered first and the data for the first EM6110 (DI is connected to the µ-processor output) entered last. All STR lines must be tied together.

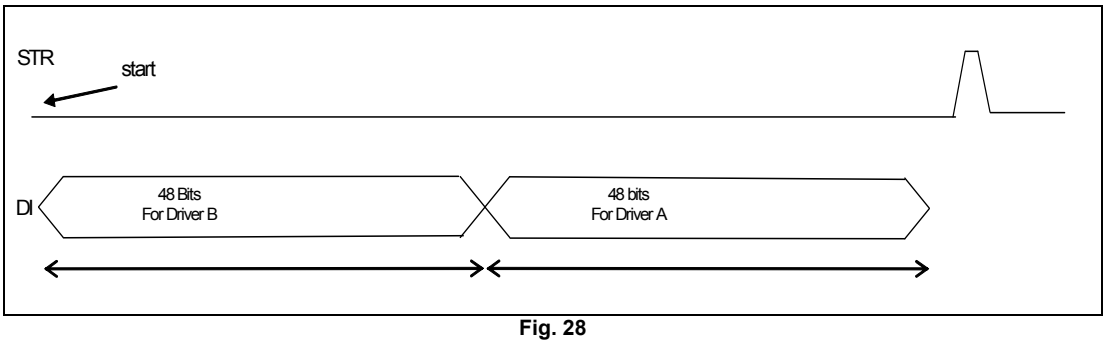


Fig. 28

Note4: For synchronisation see chapter 9.5 Synchronisation

(Shift Register Mode Description)

9.3 Shift Register configuration

9.3.1 Pin assignment

Pad Name	Function	Pin Direction
BP_1 to BP_4	Not used	Open, no connection
S_1 to S_{40}	SEG1 to SEG40	Segment output
V_4	LCD voltage bias level	V_4 must be externally connected to V_{SS}, See chapter 6
V_3	Not used	Open, no connection
V_2	Not used	Open, no connection
V_1	Not used	Open, no connection
V_{LCD}	LCD supply voltage	See chapter 6
V_{DD}	Supply voltage for logic part	See chapter 6
GND = V_{SS}	Ground power supply for logic part	See chapter 6
CLK	Serial clock input	Input
DI	Serial data input	Input
DO	Serial data output	Output
COLN	BLANK display	Input
STR	Data strobe	Input
FR	Frame signal	Input, if SFR=1 Output, it SFR=0
SFR	Frame generation selection *0= Internal generation* *1= External generation*	Input
SYN	Not used	Open, no connection
SSYN	Not used	V_{SS}
OPT1	Option input to set the interface mode	0
OPT0	Option input to set the interface mode	0

Table 18

9.3.2 Protocol

The shift register mode implements a 3-wire 40-bit data transmission protocol with the signals Serial Clock CLK, Data Input DI and Strobe STR. There is no RAM used, only a 40 bit data register; the Mux mode is 1.
The data transfer is enabled, when STR is at low level. STR must be hold at low level during the transfer. After the last bit has been transfered, a positive pulse at STR stops the transmission and latches the shifted data into EM6110 internal register with its logic 1 level.
The information at the data input DI is shifted into the LCD driver at CLK falling edge, data word length is 40 bit.
The display corresponds to the latched data, the first data sent defines SEG40, etc. until the last data, which defines SEG1.

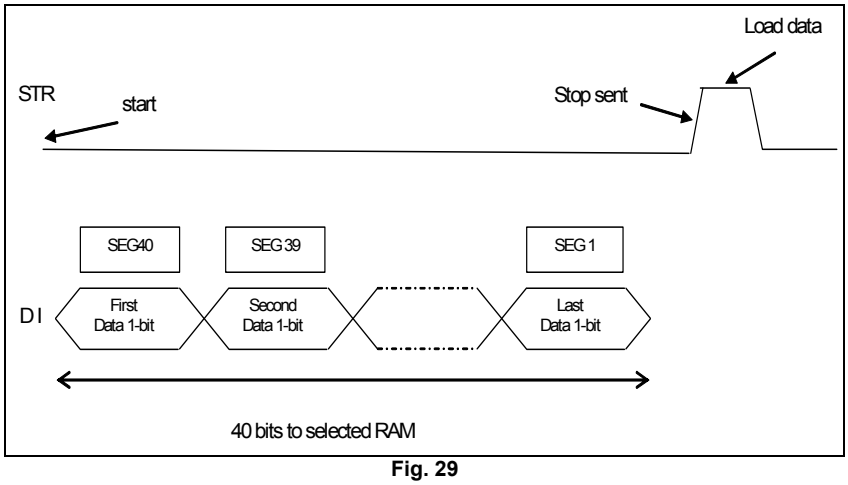


Fig. 29

9.3.3 Initialisation

No initialisation is needed.

9.3.4 DDRAM Architecture

The DDRAM is reduced to a 40 bit register. Each bit of the register corresponds to 1 pixel in the display.

SEG 1	SEG 2	SEG 3	SEG 4		SEG 37	SEG 38	SEG 39	SEG 40
data40	data39	data38	data37		data4	data3	data2	data1

Fig. 30 DDRAM description in Shift Register configuration

9.3.5 Power on Reset

There is no Power On Reset function in Shift Register mode. The display outputs start immediately with random S1 to S40 data. The BLANK function can be used to have a proper start-up of the display.

9.3.5.1 BLANK Function

This function allows to blank the display, using the input COLN.

In shift register mode, when COLN is at high level, the display is blanked: all segment and backplane outputs are at V_{SS} level. COLN does not clear the information in the 40-bit display data latch.

9.3.6 Cascading

In cascaded applications, one EM6110 has to provide the backplane (SEG1 output), the rest of the drivers will act as column drivers (see Fig. 32 below). When cascading devices, all CLK lines must be tied together and all STR lines must be tied together. Only one of the LCD drivers in a cascaded group generates the frame frequency (its FR is output), all other FR are input and are connected to the FR output.

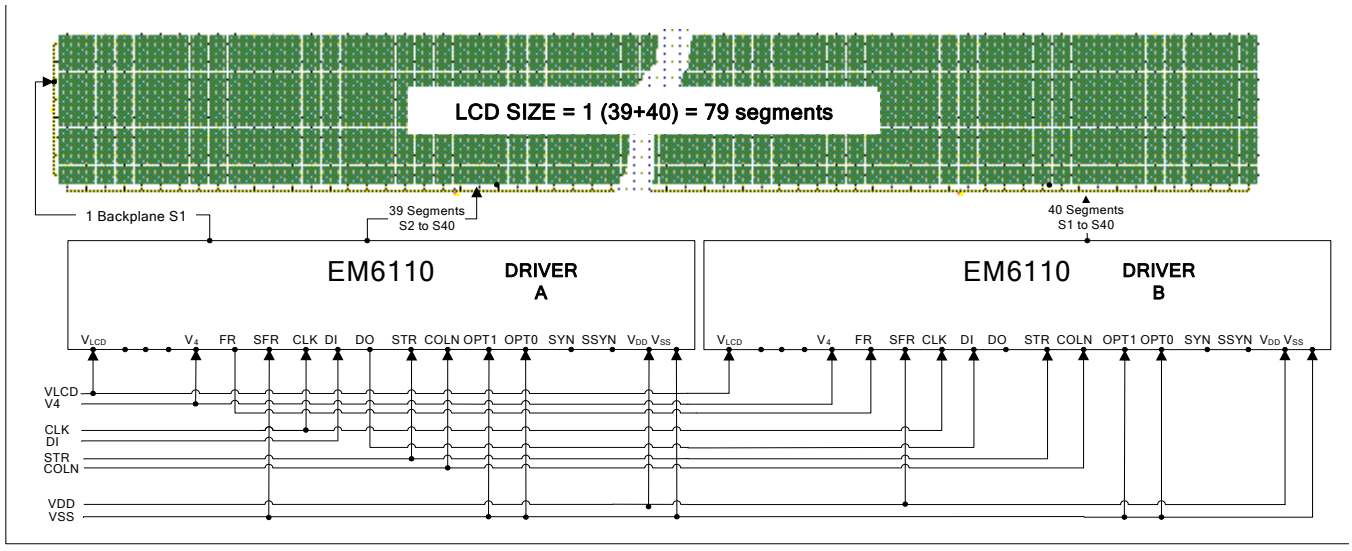


Fig. 31

Note that in a system with several cascaded EM6110 only one EM6110 with SFR=0 is allowed, configurating its FR as output. In other case differences in the frequency of the LCD drivers could create bad synchronisation in the display.

The data output pin DO is used in cascaded applications to transfer the data to the DI input of the next cascaded chip.
(The data at DO corresponds to the data at DI of the same chip, delayed by 40 clock periods.)

(Shift Register Mode Description)

To cascade EM6110 circuits, the DO of one chip must be connected to DI of the following chip. The 40 bit data for the last EM6110 (DO is not connected) must be entered first and the data for the first EM6110 (DI is connected to a µ-processor output) entered last. All STR lines must be tied together.

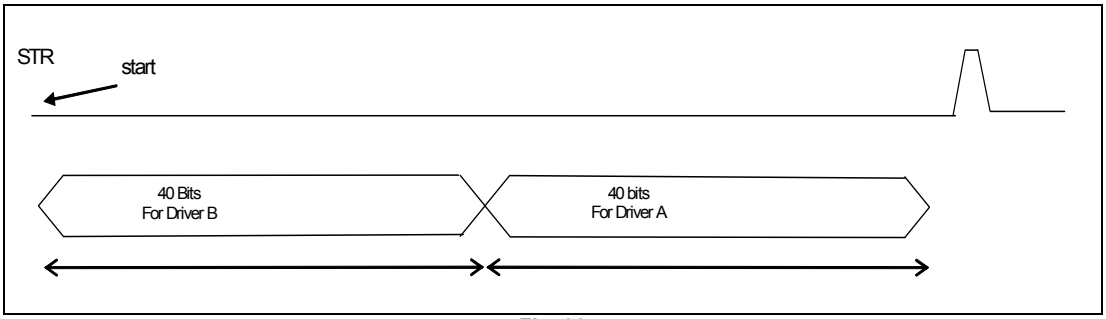


Fig. 32

Synchronisation is not needed in Shift Register configuration, the signals SYN and SSYN are not used.
(There is only one phase of FR, due to Mux mode 1.)

9.4 Double RAM configuration

9.4.1 Pin assignment

Pad Name	Function	Pin Direction
BP_1 to BP_4	Not used	Open, no connection
S_1 to S_{40}	See **Error! Reference source not found.**	Segment / Col Output
V_4	LCD voltage bias level	V_4 must be externally connected to V_{SS}, See chapter 6
V_3	LCD voltage bias level V3	Input, if external bias generation Output, if internal bias generation
V_2	LCD voltage bias level V2	Input, if external bias generation Output, if internal bias generation
V_1	LCD voltage bias level V1	Input, if external bias generation Output, if internal bias generation
V_{LCD}	LCD supply voltage	See chapter 6
V_{DD}	Supply voltage for logic part	See chapter 6
GND = V_{SS}	Ground power supply for Logic part	See chapter 6
CLK	Serial clock input	Input
DI	Serial data input	Input
DO	Serial data outputs	Output
COLN	Select row / column driver *1= row and column driver* *0 = column driver only*	Input
STR	Data strobe, blank, switch RAM input	Input
FR	Frame signal	Input, if SFR=1 Output, if SFR=0
SFR	Frame generation selection *0= Internal generation* *1= External generation*	Input
SYN	Synchronisation Signal	Input if SSYN=1 Output it SSYN=0
SSYN	SYN generation selection *0= Internal generation* *1= External generation*	Input
OPT1	Option input to set the interface mode	0
OPT0	Option input to set the interface mode	1

Table 19

Table 22 shows the distribution of row and col drivers to the outputs S_1 to S_{40}:

COLN	1			0
Mux mode	8	4	2	
S_1	Row1	Row1	Row1	Col1
S_2	Row2	Row2	Row2	Col2
S_3	Row3	Row3	Col3	Col3
S_4	Row4	Row4	Col4	Col4
S_5	Row5	Col5	Col5	Col5
S_6	Row6	Col6	Col6	Col6
S_7	Row7	Col7	Col7	Col7
S_8	Row8	Col8	Col8	Col8
S_{9}...S_{40}	Col9...40	Col9...40	Col9...40	Col9...40

Table 20

(Double RAM Mode Description)

9.4.2 Protocol

The double RAM mode implements a 3-wire data transmission protocol with the signals Serial Clock CLK, Data Input DI and Strobe STR. The Mux mode can be 2, 4 or 8. With input COLN = 0, the column only driver mode can be selected.

The data transfer is enabled, when STR is at low level. STR must be hold at low level during the transfer. After the last bit has been transfered, a positive pulse at STR stops the transmission and latches the shifted data into EM6110 internal registers or RAM with its negative edge.

The information at the data input DI is shifted into the LCD driver at CLK falling edge, data word length is 48 bit. The transfer begins with the column data, this means 40 bit and finishes with the command byte of 8 bit.

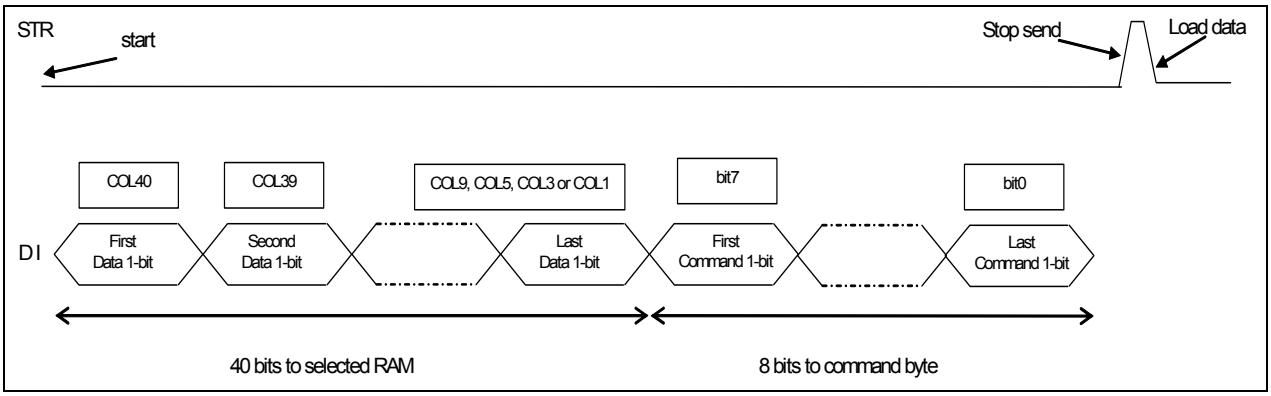


Fig. 33 Serial interface protocol

Column data is transfered with MSB bit first, setting data for COL_{40}, until LSB bit, setting data for COL_3 (Mux = 2), or COL_5 (Mux = 4) or COL_9 (Mux = 8).

The column data, if input COLN = 1, is organised as shown in Fig.35:

MSB-first												LSB-last
data1	data2	data3	data4	data5	data6	data7	…	…	…	data32, 36, or 38	…	
COL40	COL39	COL38	COL37	COL36	COL35	COL34	…	…	…	COL9, COL5 or COL3	8, 4 or 2 don't care	
40-bits												

Fig. 34

The column data, if input COLN = 0, is organised as shown in Fig.36: (Column only driver mode)

MSB-first																LSB-last
data1	data2	data3	data4	data5	data6	data7	…	…	…	…	…	…	…	…	…	data40
COL40	COL39	COL38	COL37	COL36	COL35	COL34	…	…	…	…	…	…	…	…	…	COL1
40-bits																

Fig. 35

The command byte data is organised as shown in Fig.37:

MSB-first							LSB-last
BLANK	SET	Add0	Add1	Add2	W	Mux1	Mux0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
8 bits							

Fig. 36

(Double RAM Mode Description)

Depending on the selected Mux mode there exist unused bits in the 40 bit display data word. The EM6110 has 40 display driver outputs that represent the column and row data.

In Mux 8 mode, there are 8 rows and 32 columns driven. 8 bits in the data word are not used.
In Mux 4 mode, there are 48 rows and 36 columns driven. 4 bits in the data word are not used.
In Mux 2 mode, there are 28 rows and 38 columns driven. 2 bits in the data word are not used.

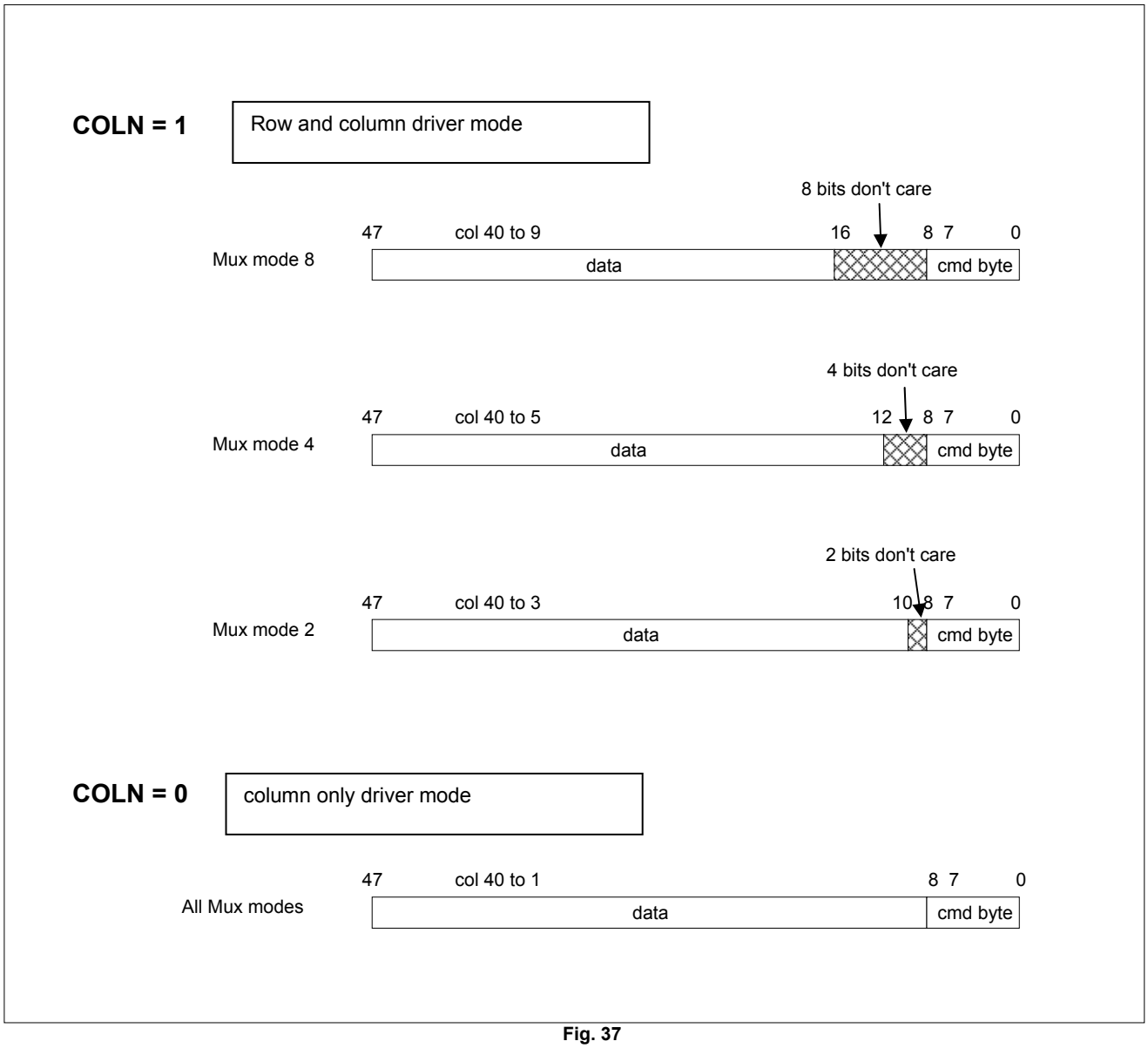


Fig. 37

9.4.3 Initialisation

To initialise the EM6110 to execute the intended functions, the corresponding bits in the command byte have to be set to define the BLANK or SET function, to define the Mux mode, to set the RAM address and to select the RAM (bit2 = W).

MSB-first							LSB-last
BLANK	SET	Add0	Add1	Add2	W	Mux1	Mux0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
8 bits							

Fig. 38

9.4.3.1 Description of instructions

9.4.3.1.1 BLANK

With a logic 1 level, the BLANK bit forces all segment outputs to the V_OFF signal as for an inactive row, so that the display is OFF. The backplane outputs BP1 to BP8 are working normally.
The BLANK function has priority over the SET function.

9.4.3.1.2 SET

The SET bit forces all segment outputs ON, if it is activated with a logic 1 level.

9.4.3.1.3 Y-Address

These three bits (bit5 to bit3 of the command byte) set the Y-Address of the DDRAM, acc. Table 19:

RAM Y-Address	Add2	Add1	Add0	Mux 8	Mux 4	Mux 2
1	0	0	0	Row1	Row1	Row1
2	0	0	1	Row2	Row2	Row2
3	0	1	0	Row3	Row3	
4	0	1	1	Row4	Row4	
5	1	0	0	Row5		
6	1	0	1	Row6		
7	1	1	0	Row7		
8	1	1	1	Row8		
	bit3	bit4	bit5			

Table 21

9.4.3.1.4 Mux Mode

The bits 1 and 0 of the command byte set the multiplex rate, see Table 20:

Mux Mode	Mux1	Mux0
2	0	0
-	0	1
4	1	0
8	1	1
	bit1	bit0

Table 22

9.4.3.1.5 RAM Selection

The bit 2 (W) in the command word selects which of the 2 RAMs is accessed for write or read (see page 34, RAM Selection).

9.4.4 DDRAM Architecture

(General description of the DDRAM: see I2C mode, page 14)

In this mode, two equivalent DDRAMs are available. Depending on the W-bit, one RAM is selected for write and the other for read access. For write access, the Y-Address in the initialisation byte defines the position in the RAM, where the serially shifted in data are written, see following Fig.s. Each RAM-bit corresponds directly to its related display pixel.

If **Mux Mode = 8 and COLN = 1**, the DDRAM provides 8 rows and 32 columns.

RAM y-address		Col 9	Col 10	Col 11	Col 12		Col 37	Col 38	Col 39	Col 40		RAM Display
	000	data32	data31	data30	data29		data4	data3	data2	data1	Row 1	
	001	data32	data31	data30	data29		data4	data3	data2	data1	Row 2	
	010	data32	data31	data30	data29		data4	data3	data2	data1	Row 3	
	011	data32	data31	data30	data29		data4	data3	data2	data1	Row 4	
	100	data32	data31	data30	data29		data4	data3	data2	data1	Row 5	
	101	data32	data31	data30	data29		data4	data3	data2	data1	Row 6	
	110	data32	data31	data30	data29		data4	data3	data2	data1	Row 7	
	111	data32	data31	data30	data29		data4	data3	data2	data1	Row 8	

Fig. 39 DDRAM description with Mux Mode = 8 and COLN = 1

If **Mux Mode = 8 and COLN = 0**, the DDRAM provides 8 rows and 40 columns. (Column driver mode)

RAM y-address		Col 1	Col 2	Col 3	Col 4		Col 37	Col 38	Col 39	Col 40		RAM Display
	000	data40	data39	data38	data37		data4	data3	data2	data1	Row 1	
	001	data40	data39	data38	data37		data4	data3	data2	data1	Row 2	
	010	data40	data39	data38	data37		data4	data3	data2	data1	Row 3	
	011	data40	data39	data38	data37		data4	data3	data2	data1	Row 4	
	100	data40	data39	data38	data37		data4	data3	data2	data1	Row 5	
	101	data40	data39	data38	data37		data4	data3	data2	data1	Row 6	
	110	data40	data39	data38	data37		data4	data3	data2	data1	Row 7	
	111	data40	data39	data38	data37		data4	data3	data2	data1	Row 8	

Fig. 40 DDRAM description with Mux Mode = 8 and COLN = 0

If **Mux Mode = 4 and COLN = 1**, the DDRAM provides 4 rows and 36 columns.

RAM y-address		Col 5	Col 6	Col 7	Col 8		Col 37	Col 38	Col 39	Col 40		RAM Display
	000	data36	data35	data34	data33		data4	data3	data2	data1	Row 1	
	001	data36	data35	data34	data33		data4	data3	data2	data1	Row 2	
	010	data36	data35	data34	data33		data4	data3	data2	data1	Row 3	
	011	data36	data35	data34	data33		data4	data3	data2	data1	Row 4	
	100											
	101											
	110											
	111											

Fig. 41 DDRAM description with Mux Mode = 4 and COLN = 1

(Double RAM Mode Description)

If **Mux Mode = 4 and COLN = 0**, the DDRAM provides 4 rows and 40 columns. (Column driver mode)

RAM y-address		Col 1	Col 2	Col 3	Col 4		Col 37	Col 38	Col 39	Col 40		RAM Display
	000	data40	data39	data38	data37		data4	data3	data2	data1	Row 1	
	001	data40	data39	data38	data37		data4	data3	data2	data1	Row 2	
	010	data40	data39	data38	data37		data4	data3	data2	data1	Row 3	
	011	data40	data39	data38	data37		data4	data3	data2	data1	Row 4	
	100											
	101											
	110											
	111											

Fig. 42 DDRAM description with Mux Mode = 4 and COLN = 0

If **Mux Mode = 2 and COLN = 1**, the DDRAM provides 2 rows and 38 columns.

RAM y-address		Col 3	Col 4	Col 5	Col 6		Col 37	Col 38	Col 39	Col 40		RAM Display
	000	data38	data37	data36	data35		data4	data3	data2	data1	Row 1	
	001	data38	data37	data36	data35		data4	data3	data2	data1	Row 2	
	010											
	011											
	100											
	101											
	110											
	111											

Fig. 43 DDRAM description with Mux Mode = 2 and COLN = 1

If **Mux Mode = 2 and COLN = 0**, the DDRAM provides 2 rows and 40 columns. (Column driver mode)

RAM y-address		Col 1	Col 2	Col 3	Col 4		Col 37	Col 38	Col 39	Col 40		RAM Display
	000	data40	data39	data38	data37		data4	data3	data2	data1	Row 1	
	001	data40	data39	data38	data37		data4	data3	data2	data1	Row 2	
	010											
	011											
	100											
	101											
	110											
	111											

Fig. 44 DDRAM description with Mux Mode = 2 and COLN = 0

9.4.4.1 DDRAM addressing

The Y-Address pointer is used to address the RAM rows, which correspond to display rows. As the EM6110 offers 3 programmable multiplex rates in this mode, the number of the row drivers is variable.

The address ranges depend on multiplex rate (Mux Mode) as follows:

- If Mux Mode = 8: 000b ≤ Y-Address ≤ 111b
- If Mux Mode = 4: 000b ≤ Y-Address ≤ 011b
- If Mux Mode = 2: 000b ≤ Y-Address ≤ 001b

Addresses outside these ranges are not allowed.

9.4.4.2 RAM Selection

The bit 2 (W) selects which of the 2 RAMs is accessed for write, respectively which RAM is read to display.

Detailed description:

If W = “0”, the EM6110 writes into RAM1 and reads from RAM2.

Switching to write RAM2 and read RAM1 (with W = “1”) occurs at the falling edge of FR, under the condition that Add2, Add1, Add0 is “000b” and a falling edge of STR occured before.

If W = “1”, the EM6110 writes into RAM2 and reads from RAM1.

9.4.4.2.1 Example: Switching from read RAM2 to read RAM1

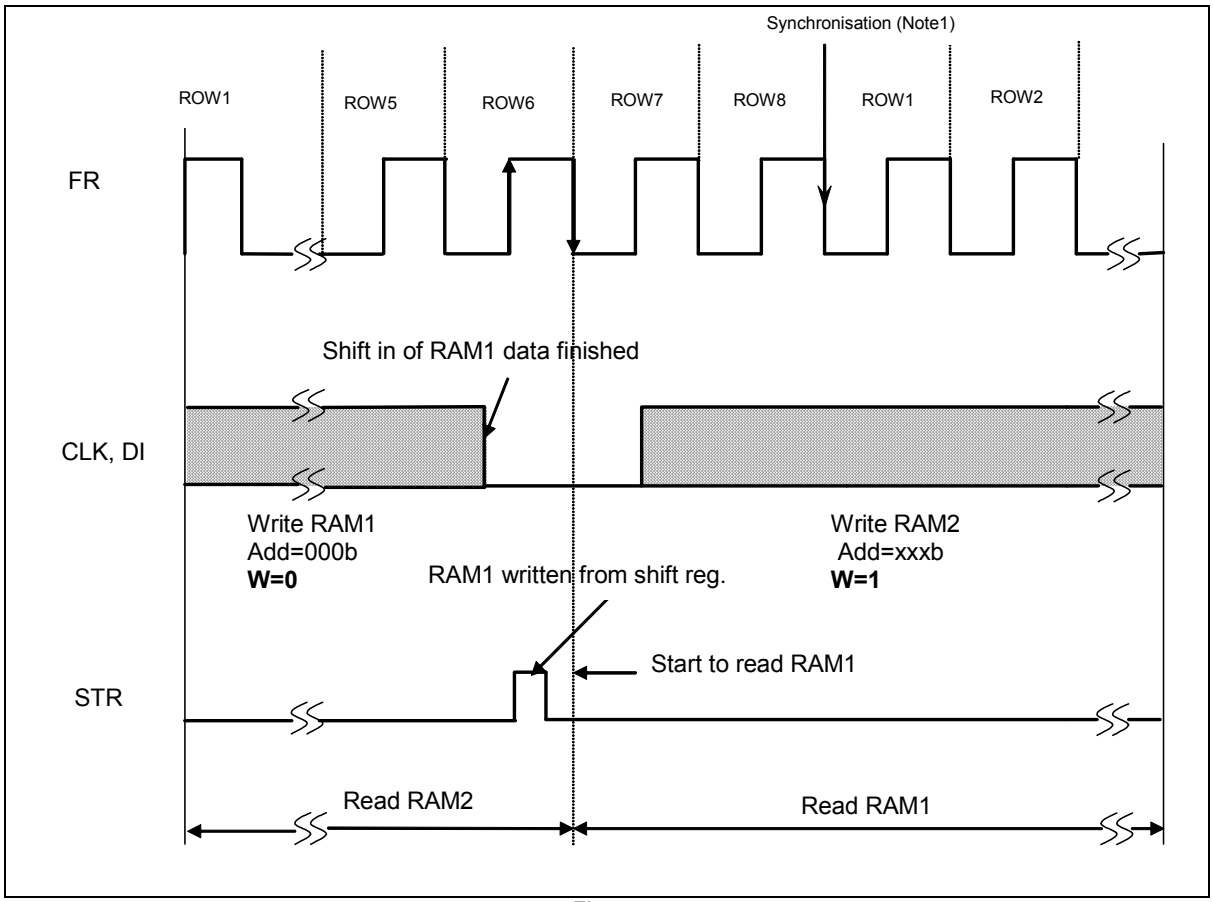


Fig. 45

Note 1: For synchronisation see chapter 9.5: Synchronisation

9.4.5 Power on Reset

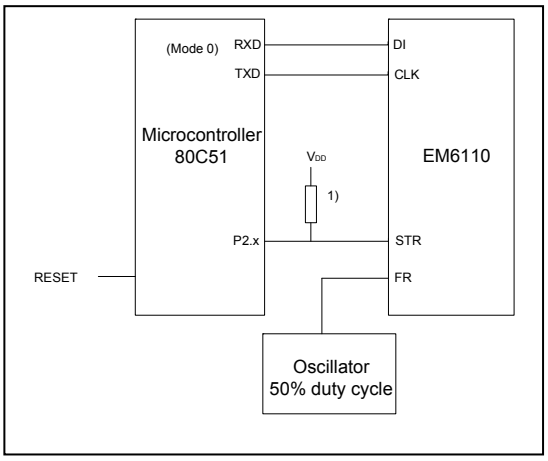
In the Double RAM mode is no Power On Reset function. The display output starts immediately with random segment data.

9.4.5.1 Blank Function

Besides the BLANK bit in the command byte, the display can be blanked in this mode by using input STR. When STR is at logic level 1, the display is OFF.

9.4.5.2 Example power-up for Double RAM configuration

After power up, the data in the shift register and the two display RAMs are undefined. The BLANK bit should be activated until valid data is written into the selected display RAM. To avoid parasitic display effects from power up until the BLANK bit in the command word is written, the input STR can blank the display according to the schematic shown below:



1) When the microprocessor is reset, the port pin for STR will be configured as input and so STR line would float. The pull-up resistor will ensure a logic level 1 and therefore a blanked LCD display while the system reset is active and until the port pin is set up by software.

Provide a blanked display while power up and until the BLANK bit is written using STR input:

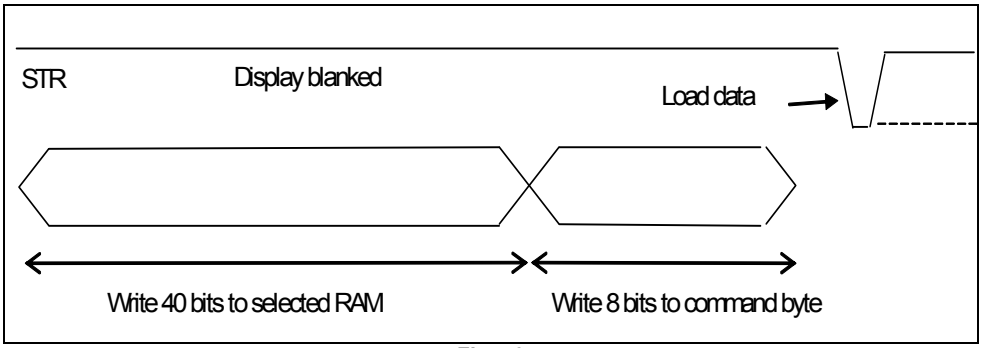


Fig. 46

9.4.6 Cascading

In cascaded applications, one EM6110 has to provide the backplane signals to drive the rows of the display and the other drivers will act as pure column drivers (COLN = 0). When cascading devices, all CLK and STR inputs should be tied together. Only one of the EM6110 in the cascaded group must defines the frame frequency, with its FR as output. In this case all FR lines must be tied together. (see Fig. 48 below)

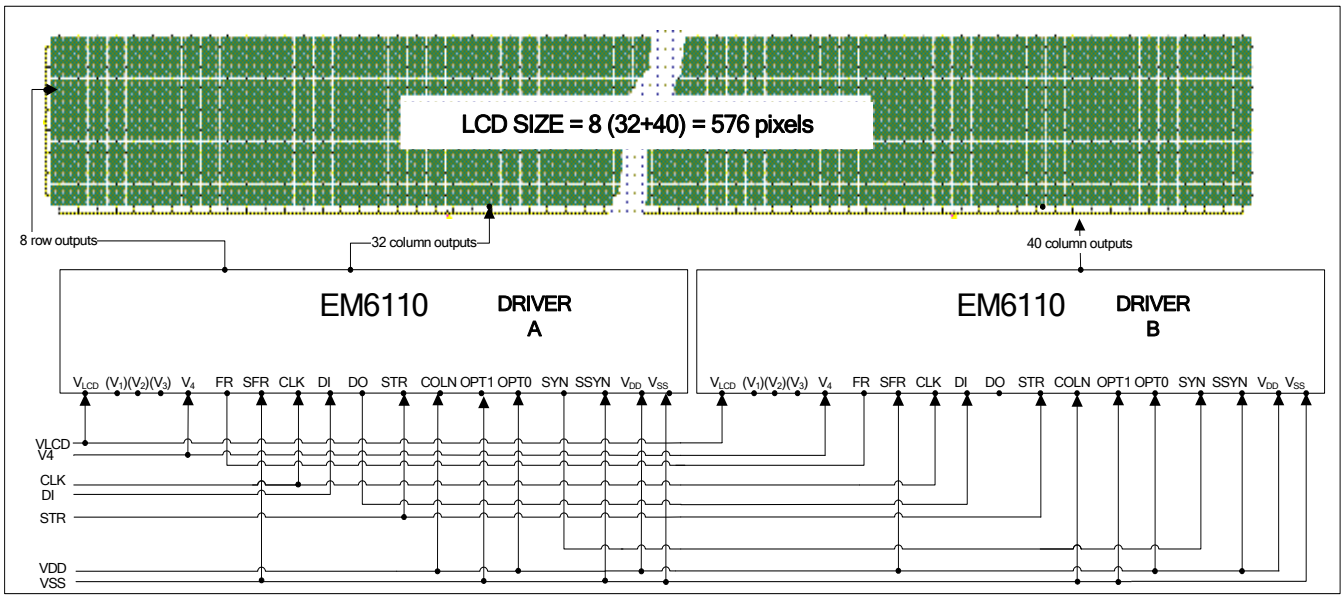


Fig. 47: Example in Mux mode 8

Note1
In a system with several EM6110 cascaded, only one EM6110 with SFR = 0 is allowed. In other case, differences in the frequency of the LCD drivers could create bad synchronisation in the display.

Note2
When cascading EM6110s, only one EM6110 with SSYN = 0 is allowed. Only one driver generates the synchronisation.

Note3
When cascading EM6110s, never cascade one mux mode with another. If e.g. an EM6110 with Mux mode 4 is used to drive the rows, then only EM6110s Mux mode 4 can be cascaded with it.

The data output pin, DO, is used in cascaded applications to transfer the data to the next cascaded chip DI input.

(The data at DO corresponds to the data at DI delayed by 48 clock periods.)

To cascade EM6110 circuits, the DO of one chip must be connected to DI of the following chip. The 48 bit data for the last EM6110 (DO is not connected) must be entered first and the data for the first EM6110 (DI is connected to the µ-processor output) entered last. All STR lines must be tied together.

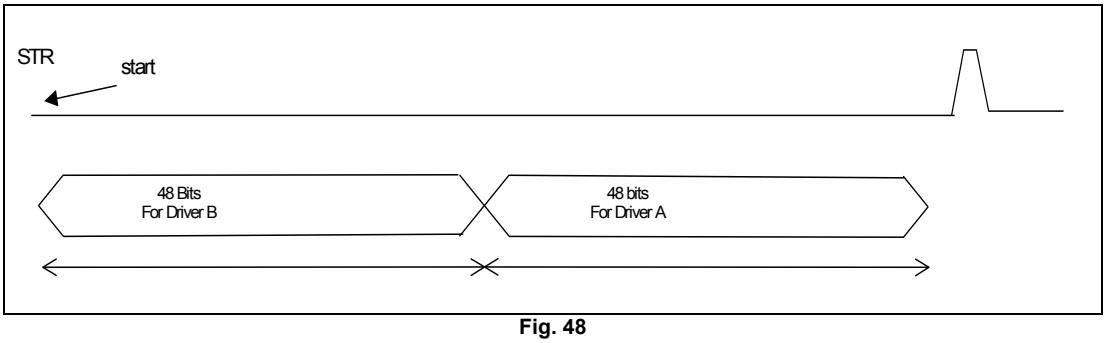


Fig. 48

Note4: For synchronisation see chapter 9.5 Synchronisation

9.5 Synchronisation

Data transfer from µcontroller to an LCD driver should periodically be refreshed to avoid possible malfunction.

In a system with several cascaded EM6110 driving a large display, all EM6110 ICs must be synchronised, so that all outputs row1 are activated simultaneously, because one LCD pixel could be connected to a row driver of one chip and a segment driver of another one.

Two signals are available to synchronise EM6110: SSYN and SYN

SSYN	SYN	
0	output	IC generates the synchronisation signal
1	input	IC receives the synchronisation signal

Table 23

9.5.1.1 Example with Mux 8 / OPT1=0 , OPT0 =1

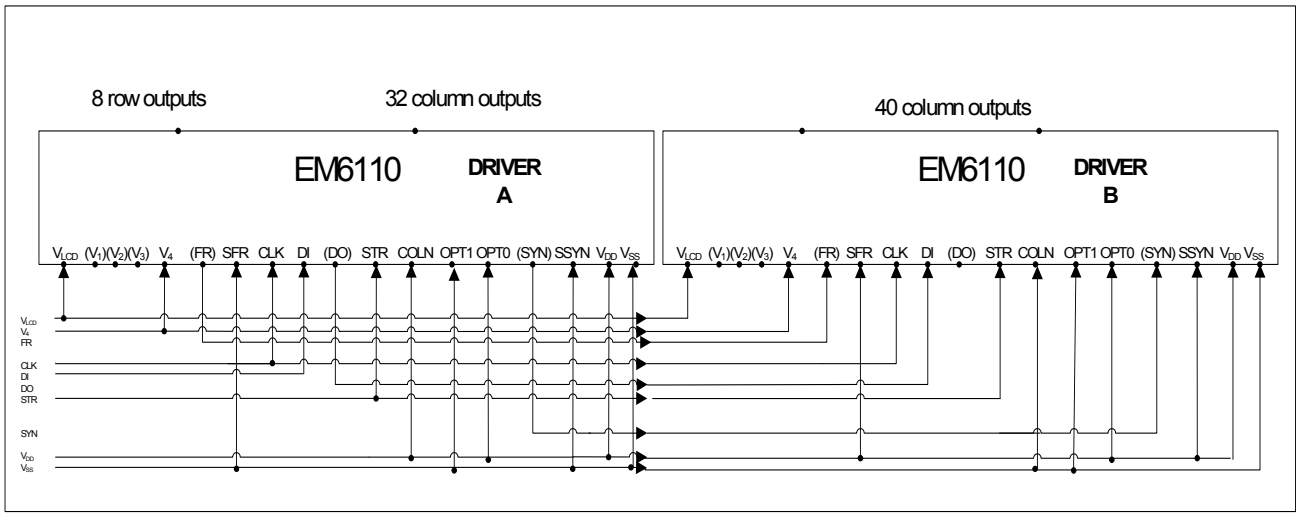


Fig. 49

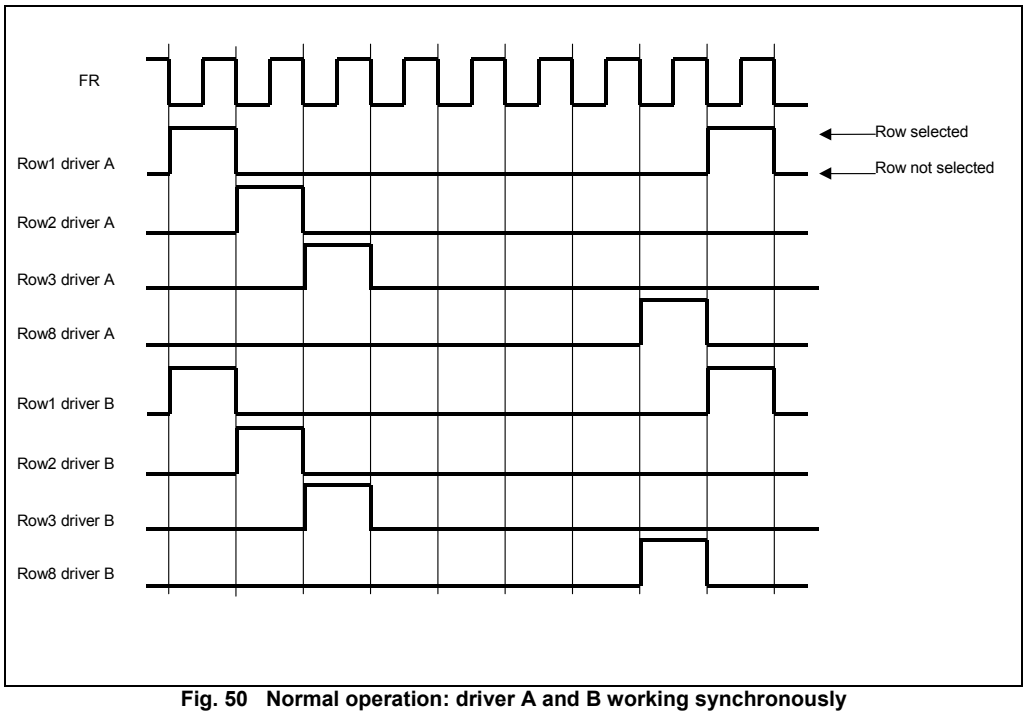


Fig. 50 Normal operation: driver A and B working synchronously

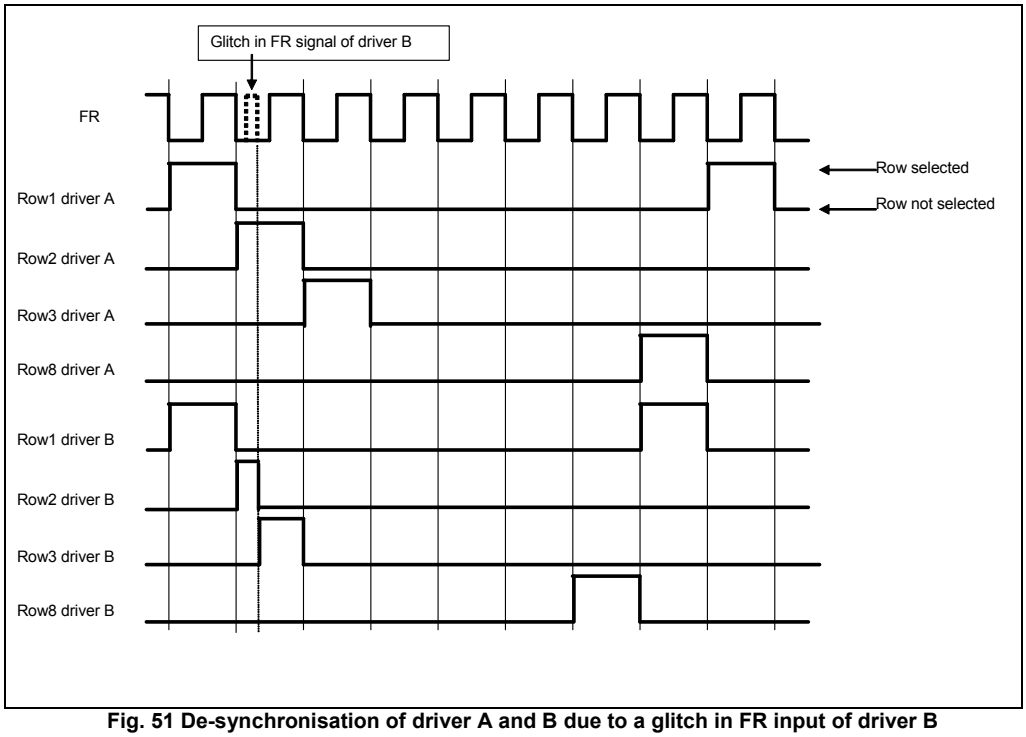


Fig. 51 De-synchronisation of driver A and B due to a glitch in FR input of driver B

In order to synchronise EM6110s in a system with several drivers, the signal SYN is generated by the driver which has its SSYN input set to 0. The output SYN of this driver is connected to the SYN inputs of all other drivers (their inputs SSYN set to logic 1).

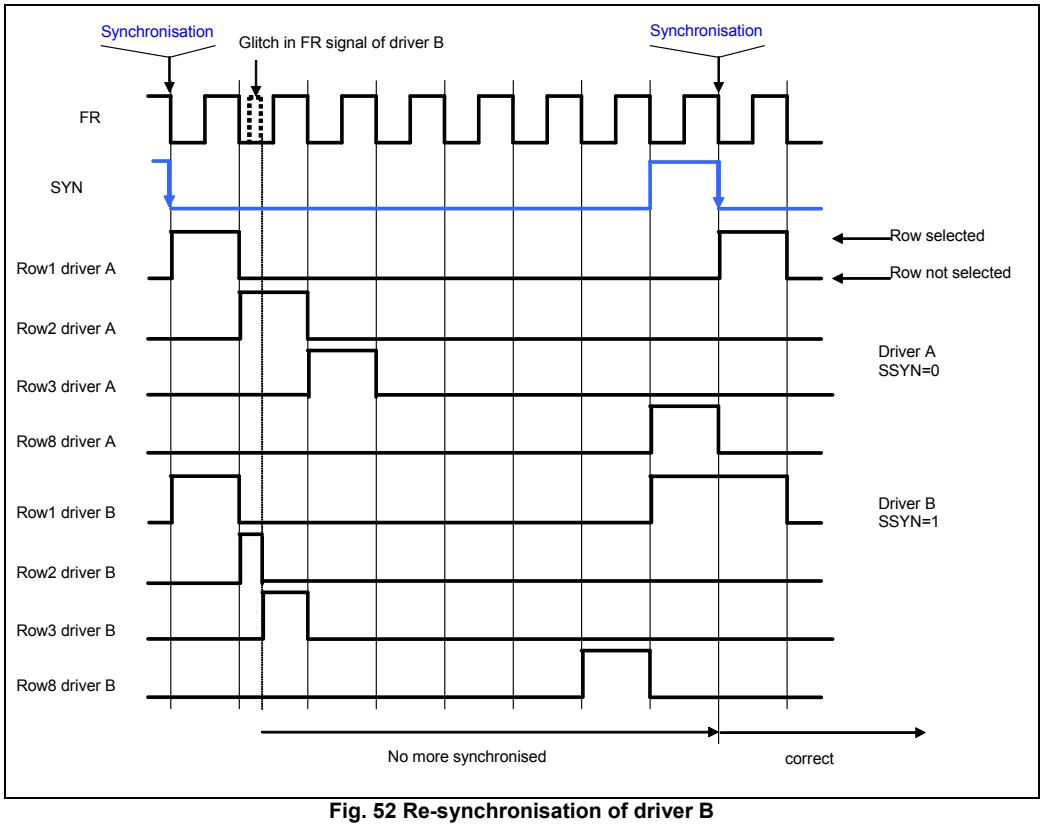


Fig. 52 Re-synchronisation of driver B

The synchronisation takes place when the display is refreshed, that means at the end of each FR-period when the last row of the selected mux rate is driven.

9.5.1.2 External Synchronisation

Synchronisation can be done also externally, by generating the signal SYN externally according to Fig. 52.

The synchronisation can also be applied at lower frequency, if the number of FR falling edges between two synchronisation sequences = n (integer) × multiplex rate

Number of cycles of FR needed to complete a display refresh:

Mux	
8	8
4	4
3	3
2	2

Table 24

9.5.1.3 Synchronisation in Shift Register configuration

If the Shift Register mode is selected (OPT0=0 and OPT1=0), the synchronisation is not needed, in this case the signals SSYN and SYN are configured as shown in the table 25 below:

SSYN	SYN function	Connect SYN
V_{SS}	Output	Open
VDD	Input	V_{SS} or VDD

Table 25

9.6 Frame frequency

The FR signal controls the segment output frequency generation (see §11: LCD Waveforms). To avoid a DC component on the resulting display voltage, the FR signal must have a 50% duty cycle. The LCD pixel voltage changes polarity with the FR signal. The frequency of the FR signal must be n times the intended display refresh rate, where n is the EM6110 Mux mode (1, 2, 3, 4 or 8), e.g., if the desired refresh rate is 64Hz, the FR signal frequency must be 256Hz at Mux mode 4.. A selected row (ON) is in phase with the FR signal (see LCD Waveforms).

The frame signal is generated internally or can be generated externally. The input SFR selects if FR is input or output.

- SFR = 0: FR is internally generated, the pad FR is output
- SFR = 1: FR is externally generated, the pad FR is input

If SFR=0, then EM6110 generates the frame frequency at output FR. An internal oscillator creates the frame frequency with a typical value of 64 Hz. The internal row frequency depends on the number of rows (Freq row = 64 x n, where n = 1, 2, 3, 4, 8).

10 LCD Voltage Bias Levels

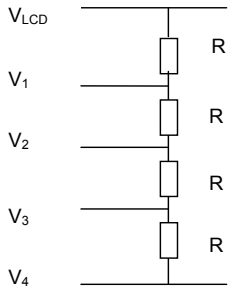
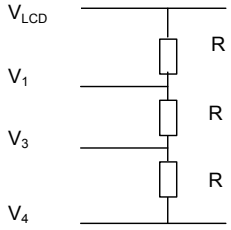
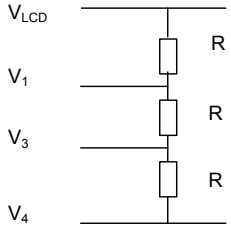
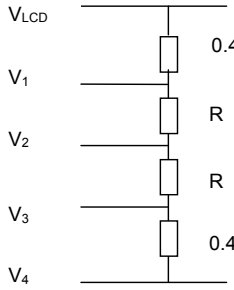
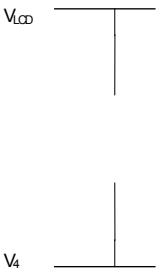
	MUX (n)	LCD Bias Configuration	$\frac{V_{LCD}}{(V_{OFF})_{RMS}}$	$\frac{(V_{ON})_{RMS}}{(V_{OFF})_{RMS}}$	V_{LCD} = 1, V4 = 0		
					V1	V2	V3
	8	4Bias 5 levels	3.4	1.446	0.75	0.5	0.25
	4	3 Bias 4 levels	3	1.73	0.667		0.333
	3	3 Bias 4 levels	3	1.73	0.667		0.333
	2	5 levels	3.69	2.41	0.85	0.5	0.15
	Mux 1 = Static						

Table 26

11 LCD Waveforms

11.1 Row and Column Multiplexing Waveform (Mux2)

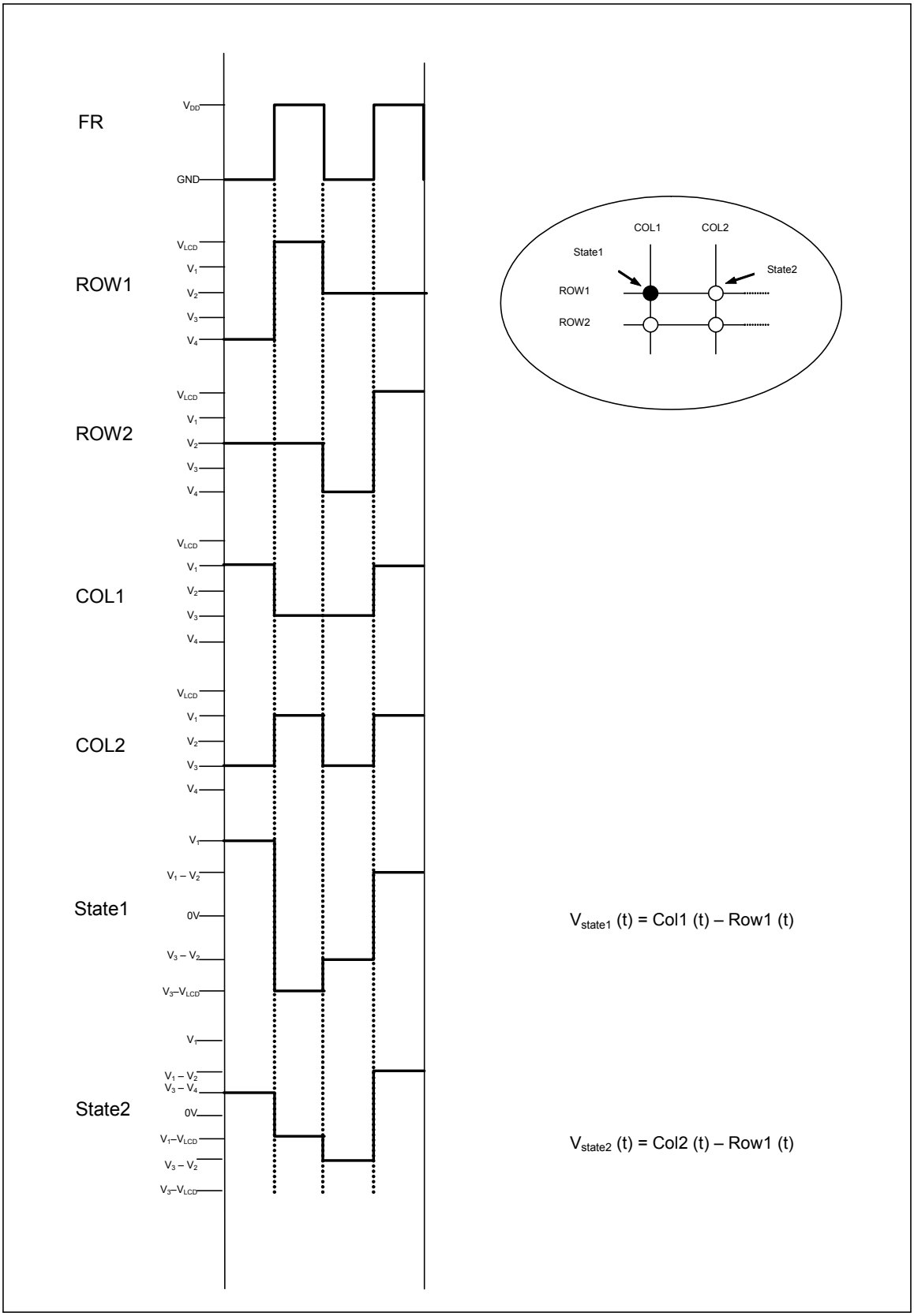


Fig. 53

11.2 Row and Column Multiplexing Waveform (Mux3)

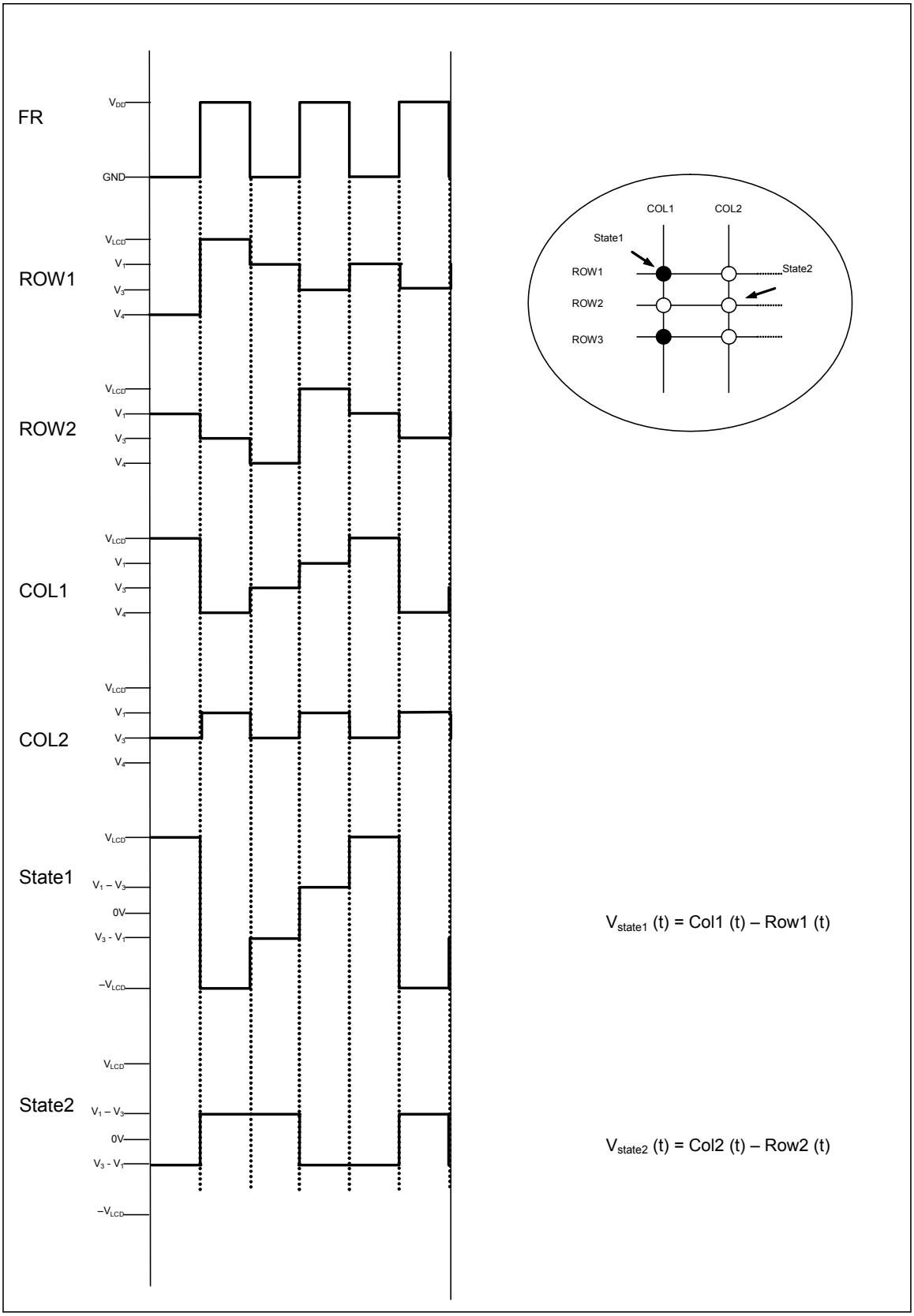


Fig. 54

11.3 Row and Column Multiplexing Waveform (Mux4)

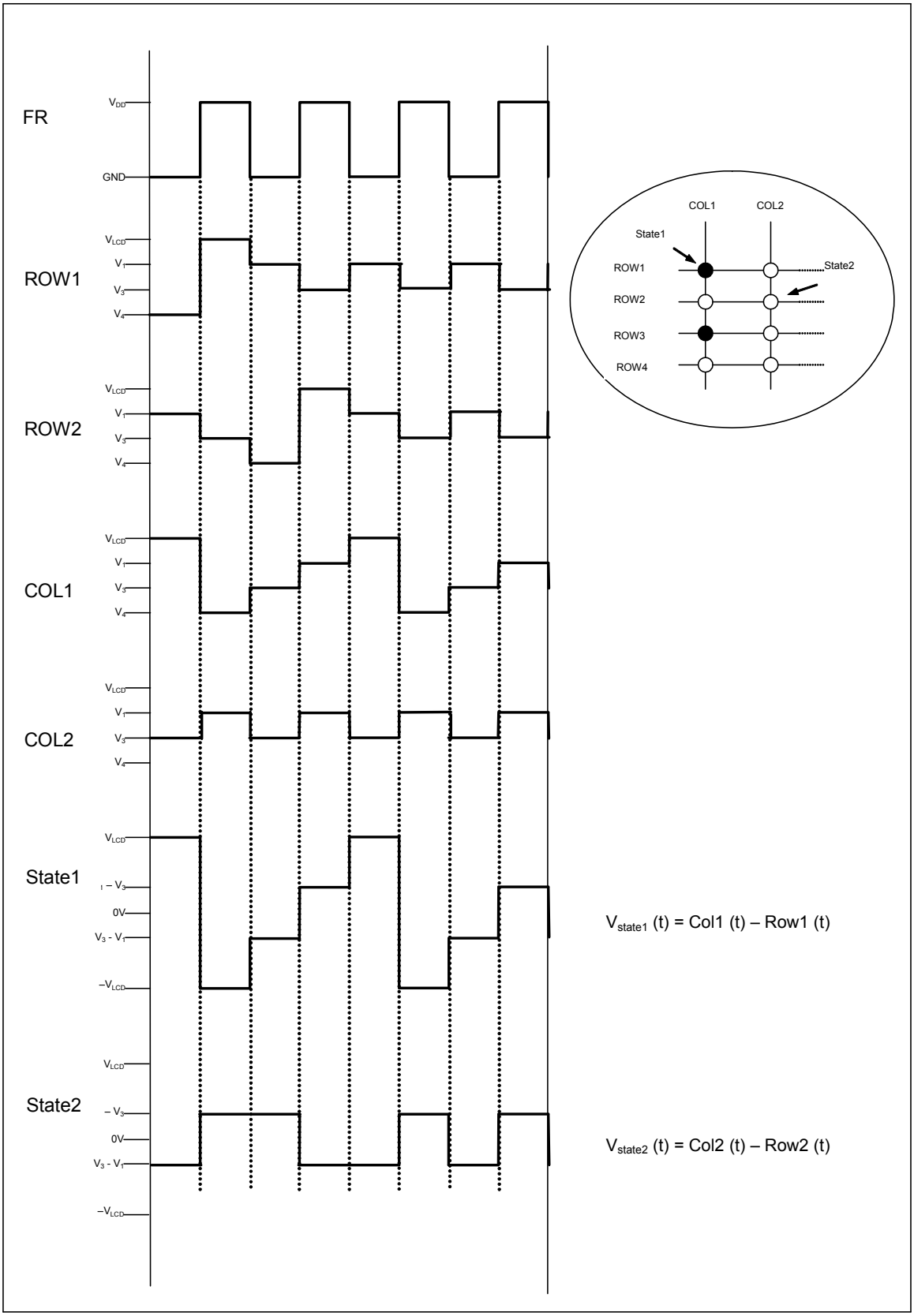


Fig. 55

11.4 Row and Column Multiplexing Waveform (Mux8)

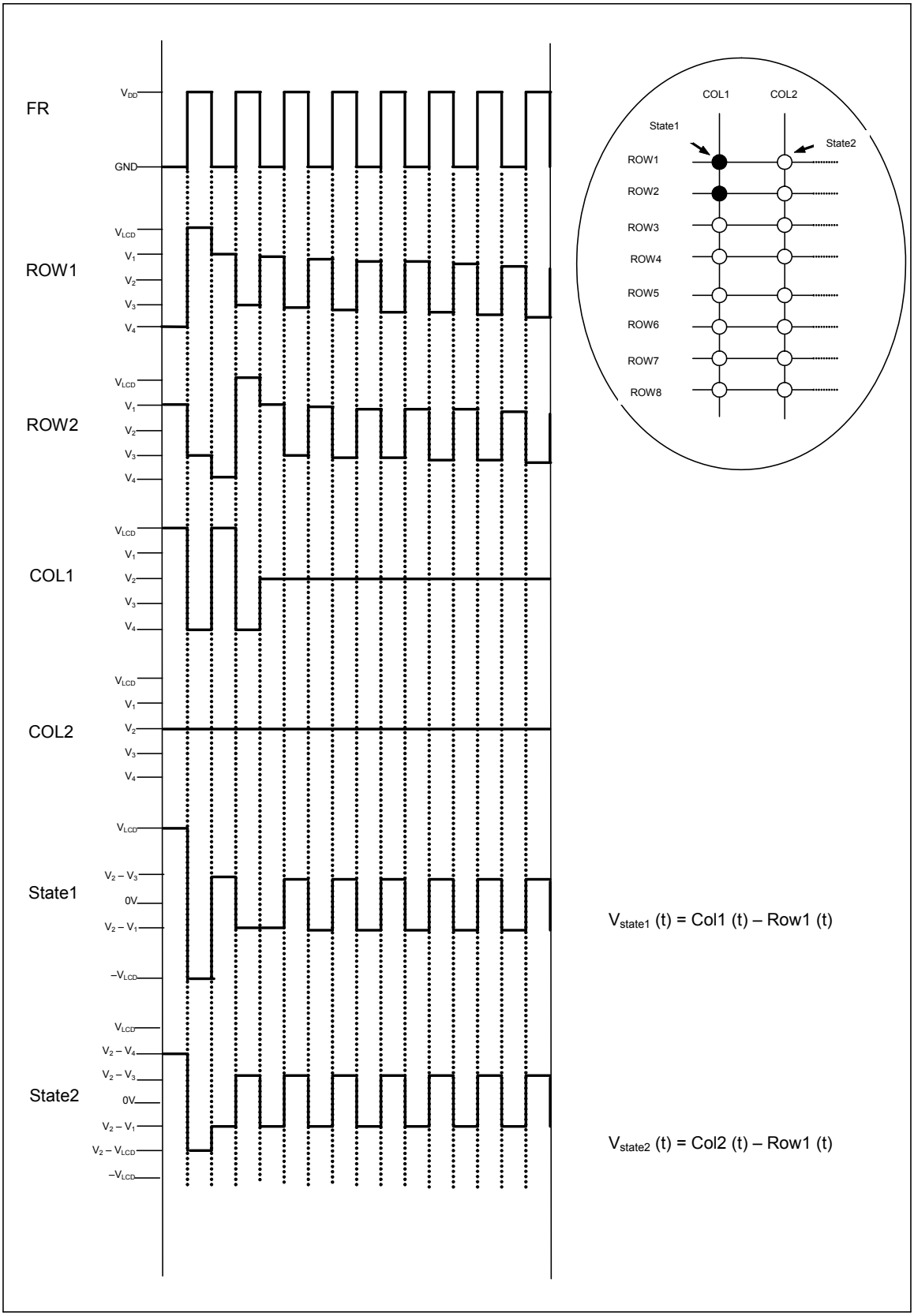


Fig. 56

11.5 Mux 1 = Static Waveform

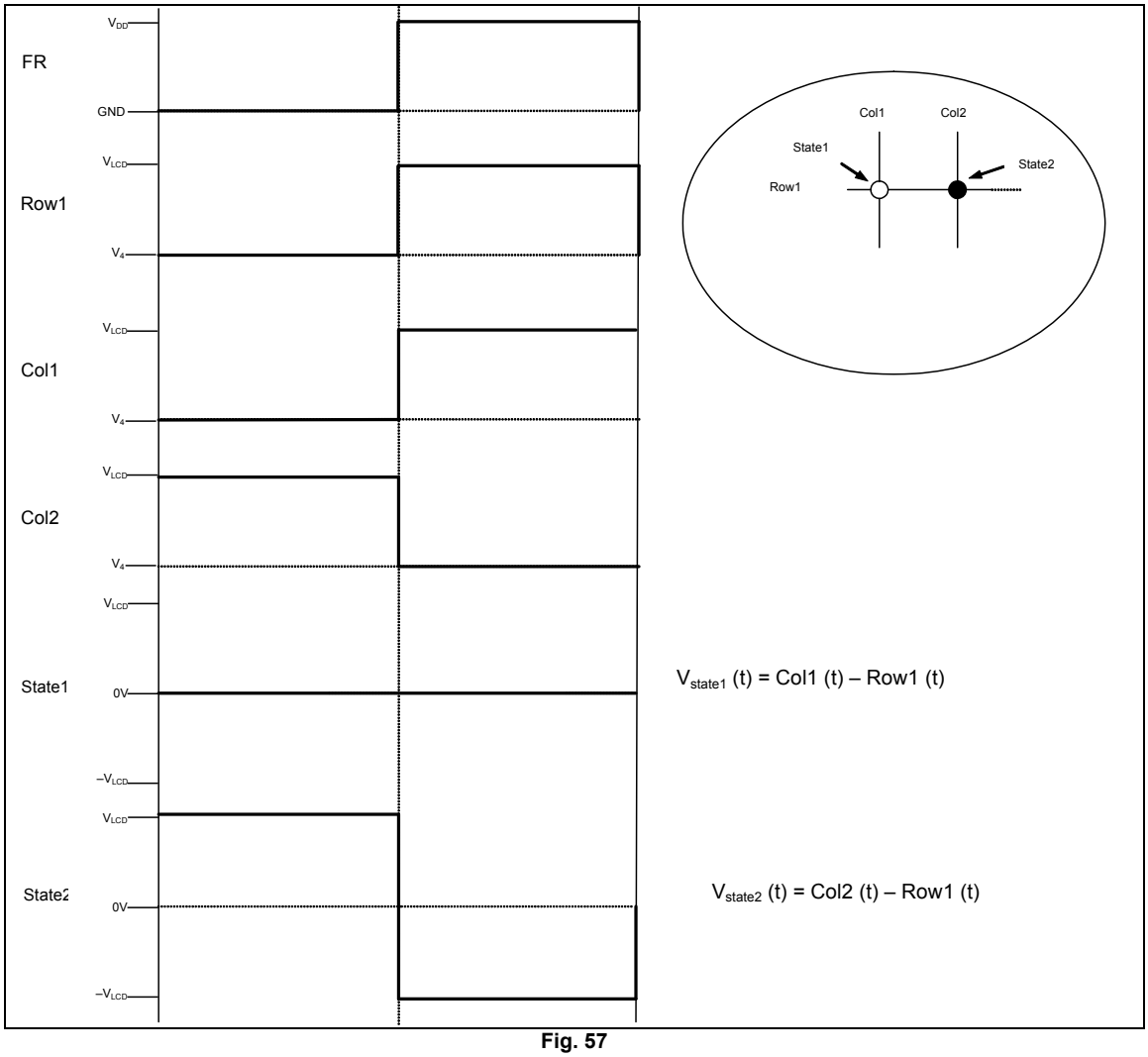


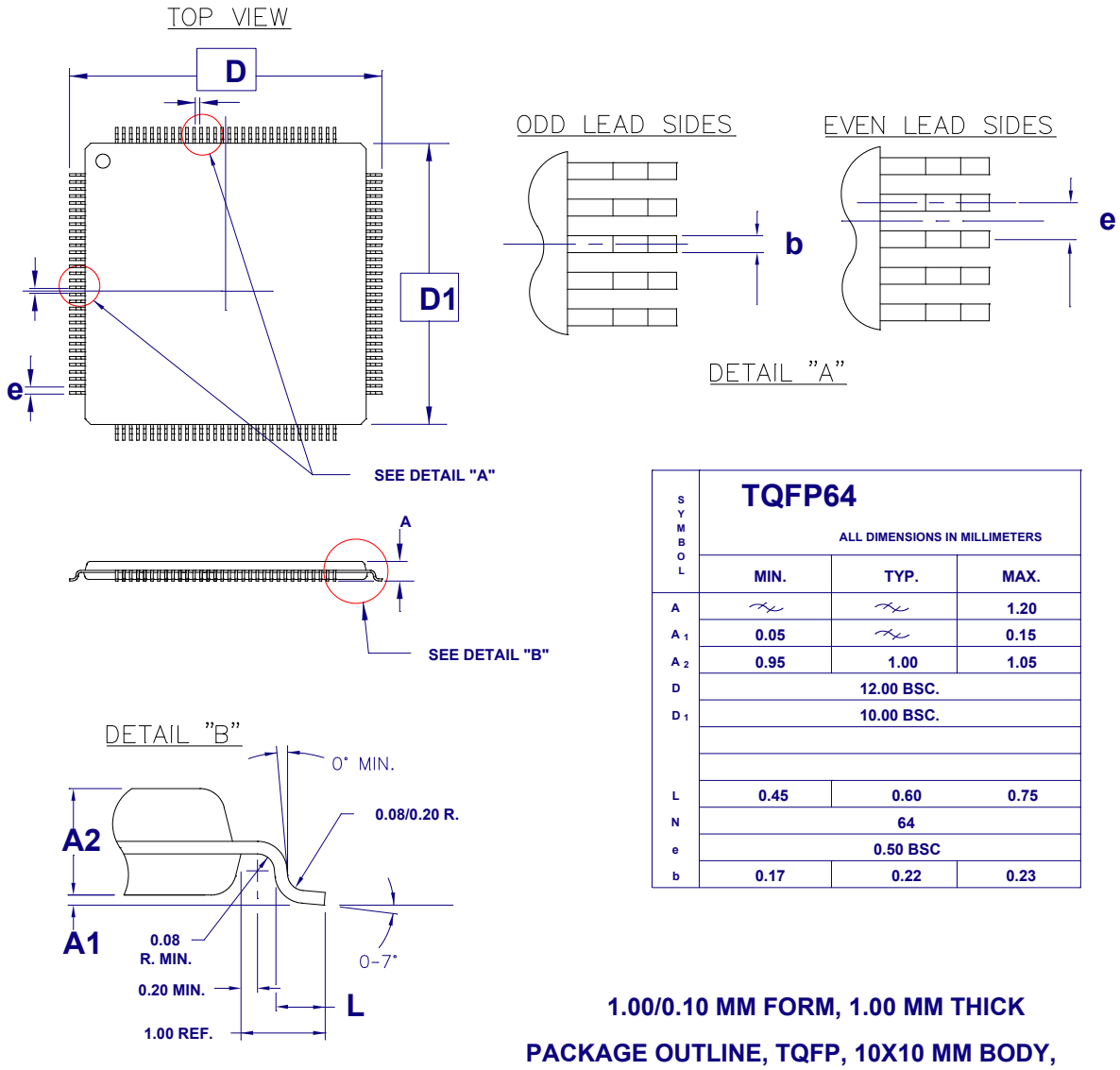
Fig. 57

Segment Switching Table:

Display data in RAM	Signal FR	Segment Voltage
0	0	V_4
0	1	V_{LCD}
1	0	V_{LCD}
1	1	V_4

Table 27

12 TQFP64 Mechanical Dimension



SYMBOL	TQFP64 ALL DIMENSIONS IN MILLIMETERS		
	MIN.	TYP.	MAX.
A			1.20
A_1	0.05		0.15
A_2	0.95	1.00	1.05
D		12.00 BSC.	
D_1		10.00 BSC.	
L	0.45	0.60	0.75
N		64	
e		0.50 BSC	
b	0.17	0.22	0.23

1.00/0.10 MM FORM, 1.00 MM THICK

PACKAGE OUTLINE, TQFP, 10X10 MM BODY,

13 Pad location

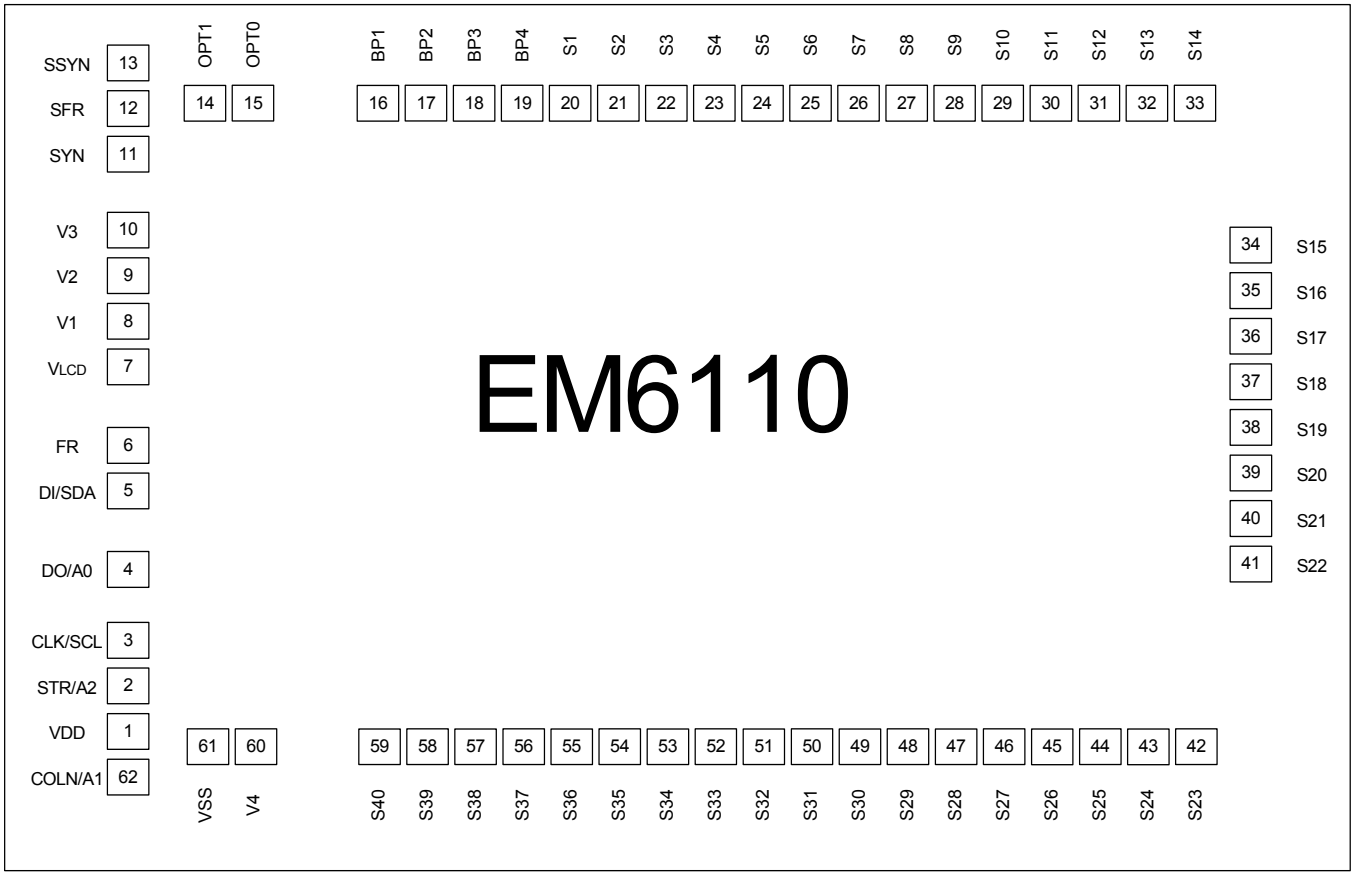


Fig. 58

* The IC substrate should be connected to VSS

13.1 Pad coordinates (Unit: µm)

N°	Pad	Coordinates	
1	VDD	X= 0.00	Y= 80.00
2	STR/A2	X= 0.00	Y= 160.00
3	CLK/SCL	X= 0.00	Y= 240.00
4	DO/A0	X= 0.00	Y= 360.20
5	DI/SDA	X= 0.00	Y= 531.30
6	FR	X= 0.00	Y= 618.90
7	V_{LCD}	X= 0.00	Y= 754.70
8	V1	X= 0.00	Y= 834.70
9	V2	X= 0.00	Y= 914.70
10	V3	X= 0.00	Y= 994.70
11	SYN	X= 0.00	Y= 1171.00
12	SFR	X= 0.00	Y= 1254.80
13	SSYN	X= 0.00	Y= 1334.80
14	OPT1	X= 151.60	Y= 1298.20
15	OPT0	X= 231.60	Y= 1298.20
16	BP1	X= 549.40	Y= 1298.20
17	BP2	X= 629.40	Y= 1298.20
18	BP3	X= 709.40	Y= 1298.20
19	BP4	X= 789.40	Y= 1298.20
20	S1	X= 869.40	Y= 1298.20
21	S2	X= 949.40	Y= 1298.20
22	S3	X= 1029.40	Y= 1298.20
23	S4	X= 1109.40	Y= 1298.20
24	S5	X= 1189.40	Y= 1298.20
25	S6	X= 1269.40	Y= 1298.20
26	S7	X= 1349.40	Y= 1298.20
27	S8	X= 1429.40	Y= 1298.20
28	S9	X= 1509.40	Y= 1298.20
29	S10	X= 1589.40	Y= 1298.20
30	S11	X= 1669.40	Y= 1298.20
31	S12	X= 1749.40	Y= 1298.20
32	S13	X= 1829.40	Y= 1298.20

N°	Pad	Coordinates	
33	S14	X= 1909.40	Y= 1298.20
34	S15	X= 1921.10	Y= 951.50
35	S16	X= 1921.10	Y= 871.50
36	S17	X= 1921.10	Y= 791.50
37	S18	X= 1921.10	Y= 711.50
38	S19	X= 1921.10	Y= 631.50
39	S20	X= 1921.10	Y= 551.50
40	S21	X= 1921.10	Y= 471.50
41	S22	X= 1921.10	Y= 391.50
42	S23	X= 1909.40	Y= 44.80
43	S24	X= 1829.40	Y= 44.80
44	S25	X= 1749.40	Y= 44.80
45	S26	X= 1669.40	Y= 44.80
46	S27	X= 1589.40	Y= 44.80
47	S28	X= 1509.40	Y= 44.80
48	S29	X= 1429.40	Y= 44.80
49	S30	X= 1349.40	Y= 44.80
50	S31	X= 1269.40	Y= 44.80
51	S32	X= 1189.40	Y= 44.80
52	S33	X= 1109.40	Y= 44.80
53	S34	X= 1029.40	Y= 44.80
54	S35	X= 949.40	Y= 44.80
55	S36	X= 869.40	Y= 44.80
56	S37	X= 789.40	Y= 44.80
57	S38	X= 709.40	Y= 44.80
58	S39	X= 629.40	Y= 44.80
59	S40	X= 549.40	Y= 44.80
60	V4	X= 241.70	Y= 44.80
61	VSS	X= 161.70	Y= 44.80
62	COLN/A1	X= 0.00	Y= 0.00

Table 28

13.2 Die Mechanical Dimensions

	Typical value	Unit
Number of Pads	62	
Minimum pad pitch	80	µm
Pad opening size for pads from BP_1 to BP_4 and S_1 to S_{40}	44 x 54	µm
Pad opening size for interface pads	44 x 54	µm
Bump size for pads from BP_1 to BP_4 and S_1 to S_{40}	60 x 70	µm
Bump size interface pads	60 x 70	µm
Bump hardness	50 (Soft)	Vickers
Bump height	17.5	µm
Wafer thickness	15	mils
Chip Size	2271 x 1560	µm

Fig. 59

14 Ordering Information

When ordering, please specify the complete part number and package.

Part Number	Version	MASK SET Versions Features	Die Form & Thickness & Package	Bumping	Conditioning	Marking
EM6110V1WS11	001	Internal bias generation	Sawn wafer, 11mils	Without gold bumps	Cadre	Not applicable
EM6110V1WP11	001	Internal bias generation	Waffle pack, 11mils	Without gold bumps	Not applicable	Not applicable
EM6110V1WP15E	001	Internal bias generation	Waffle pack, 15mils	With gold bumps	Not applicable	Not applicable
EM6110V1WP15	001	Internal bias generation	Waffle pack, 15mils	Without gold bumps	Not applicable	Not applicable
EM6110V1QF64D+	001	Internal bias generation	TQFP64	Not applicable	Tray	EM6110 001

Other delivery form might be available upon request and for a minimum order quantity. Please contact EM sales.