128K x 16 Low Power SRAM

Preliminary, Rev 1.0 07/2001

Features

- Single power supply voltage of 2.7V to 3.6V
- Power down features using CE1# and CE2
- Low operating current : 30mA(max for 55 ns)
- Maximum Standby current : 10μA at 3.6 V
- Data retention supply voltage: 1.5V to 3.6V
- Direct TTL compatibility for all input and output
- Wide operating temperature range: -40°C to 85°C
- Package type: 48-ball TFBGA, 6x8mm

Ordering Information

Part Number	Speed	I_{DDS2}	Package
EM562161BC-55	55 ns	10 μA	6x8 BGA
EM562161BC-70	70 ns	10 μA	6x8 BGA

Pin Description

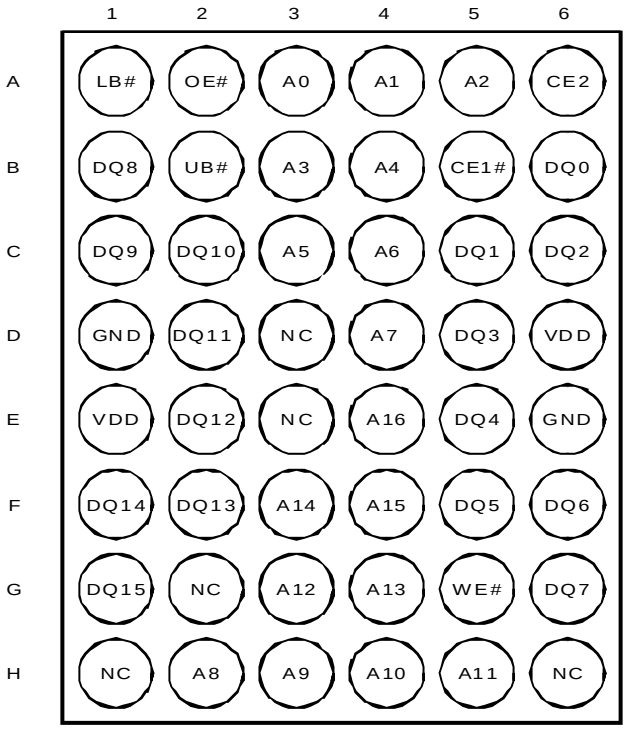
Symbol	Function
A0 - A16	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
CE1#, CE2	Chip Enable Inputs
OE#	Output Enable
WE#	Read / Write Control Input
LB#, UB#	Data Byte Control Inputs
GND	Ground
VDD	Power Supply
NC	No Connection

Overview

The EM562161 is a 2,097,152-bit SRAM organized as 131,072 words by 16 bits. It is designed with advanced CMOS technology. This Device operates from a single 2.7V to 3.6V power supply. Advanced circuit technology provides both high speed and low power. It is automatically placed in low-power mode when chip enable (CE1#) is asserted high or (CE2) is asserted low. There are three control inputs. CE1# and CE2 are used to select the device and for data retention control, and output enable (OE#) provides fast memory access. Data byte control pin (LB#,UB#) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range from -40°C to 85°C, the EM562161 can be used in environments exhibiting extreme temperature conditions.

Pin Configuration

48-Ball BGA (CSP), Top View



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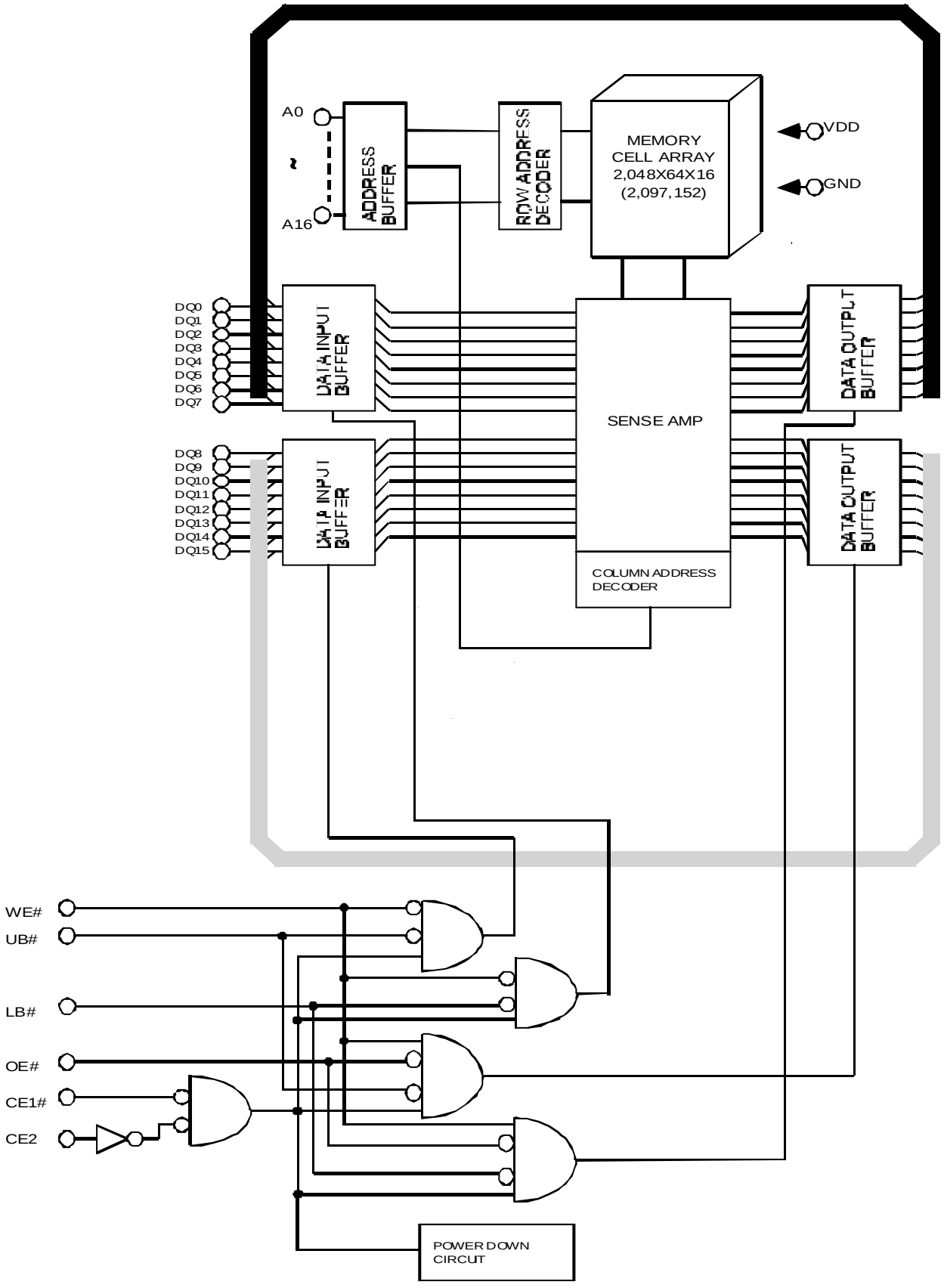
Block Diagram



Operating Mode

Mode	CE1#	CE2	OE#	WE#	LB#	UB#	DQ0~DQ7	DQ8~DQ15	Power
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	Active
					H	L	High-Z	D_{OUT}	Active
					L	H	D_{OUT}	High-Z	Active
Write	L	H	X	L	L	L	D_{IN}	D_{IN}	Active
					H	L	High-Z	D_{IN}	Active
					L	H	D_{IN}	High-Z	Active
Output Deselect	L	H	H	H	X	X	High-Z	High-Z	Active
Standby	H	X	X	X	X	X	High-Z	High-Z	Standby
	X	L	X	X	X	X			
	L	H	X	X	H	H			

Note: X = don't care. H=logic high. L=logic low.

Absolute Maximum Ratings

Supply voltage, V_{DD}	-0.3 to +4.6V
Input voltages, V_{IN}	-0.3 to +4.6V
Input and output voltages, $V_{I/O}$	-0.5 to V_{DD} +0.5V
Operating temperature, T_{OPR}	-40 to +85°C
Storage temperature, T_{STRG}	-55 to +150°C
Soldering Temperature (10s), T_{SOLDER}	240°C
Power dissipation, P_D	0.6 W

DC Recommended Operating Conditions (Ta=-40° C to 85° C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage	2.7	–	3.6	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3(1)	V
V_{IL}	Input Low Voltage	-0.3(2)	–	0.6	V
V_{DR}	Data Retention Supply Voltage	1.5	–	3.6	V

Note:
(1) Overshoot : VDD +2.0V in case of pulse width ≤ 20ns
(2) Undershoot : -2.0V in case of pulse width ≤ 20ns

DC Characteristics (Ta = -40° C to 85° C, V_{DD} = 2.7V to 3.6V)

Parameter	Symbol	Test Conditions			Min	Typ*	Max	Unit
Input low current	I_{IL}	I_{IN} = 0V to V_{DD}			- 1	–	1	µA
Output low voltage	V_{OL}	I_{OL} = 2.1 mA			-	–	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0 mA			2.2	–	–	V
Operating current	I_{DD1}	V_{DD} = 3.6 V , CE1# = V_{IL} and CE2 = V_{IH} and I_{OUT} = 0mA Other Input = V_{IH} / V_{IL}	Cycle time = min	55 ns	–	15	30	mA
				70 ns	–	10	25	
	I_{DD2}		Cycle time = 1µs		–	–	4	
Standby current	I_{DDS1}	CE1# = V_{IH} or CE2 = V_{IL}			–	–	0.5	mA
	I_{DDS2}** (Note)	CE1# ≥ V_{DD} – 0.2V or CE2 ≤ 0.2V, or LB# = UB# ≥ V_{DD} – 0.2V			–	1	10	µA

Notes:

* Typical value are measured at T_a = 25°C, and not 100% tested.

** In standby mode with CE1# ≥ V_{DD} - 0.2V, these limits are assured for the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

Capacitance (Ta = 25° C; f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}	–	–	10	pF	V_{IN} = GND
Output capacitance	C_{OUT}	–	–	10	pF	V_{OUT} = GND

Notes: This parameter is periodically sampled and is not 100% tested.

AC Characteristics and Operating Conditions (Ta = -40° C to 85° C, V_{DD} = 2.7V to 3.6V)

Read Cycle

Symbol	Parameter	EM562161				Unit
		-55		-70		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	55	–	70	–	ns
t_{AA}	Address access time	–	55	–	70	
t_{CO1}	Chip Enable (CE1#) Access Time	–	55	–	70	
t_{CO2}	Chip Enable (CE2) Access Time	–	55	–	70	
t_{OE}	Output enable access time	–	25	–	35	
t_{BA}	Data Byte Control Access Time	–	55	–	70	
t_{LZ}	Chip Enable Low to Output in Low-Z	10	–	10	–	
t_{OLZ}	Output enable Low to Output in Low-Z	3	–	3	–	
t_{BLZ}	Data Byte Control Low to Output in Low-Z	5	–	5	–	
t_{HZ}	Chip Enable High to Output in High-Z	–	20	–	25	
t_{OHZ}	Output Enable High to Output in High-Z	–	20	–	25	
t_{BHZ}	Data Byte Control High to Output in High-Z	–	20	–	25	
t_{OH}	Output Data Hold Time	10	–	10	–	

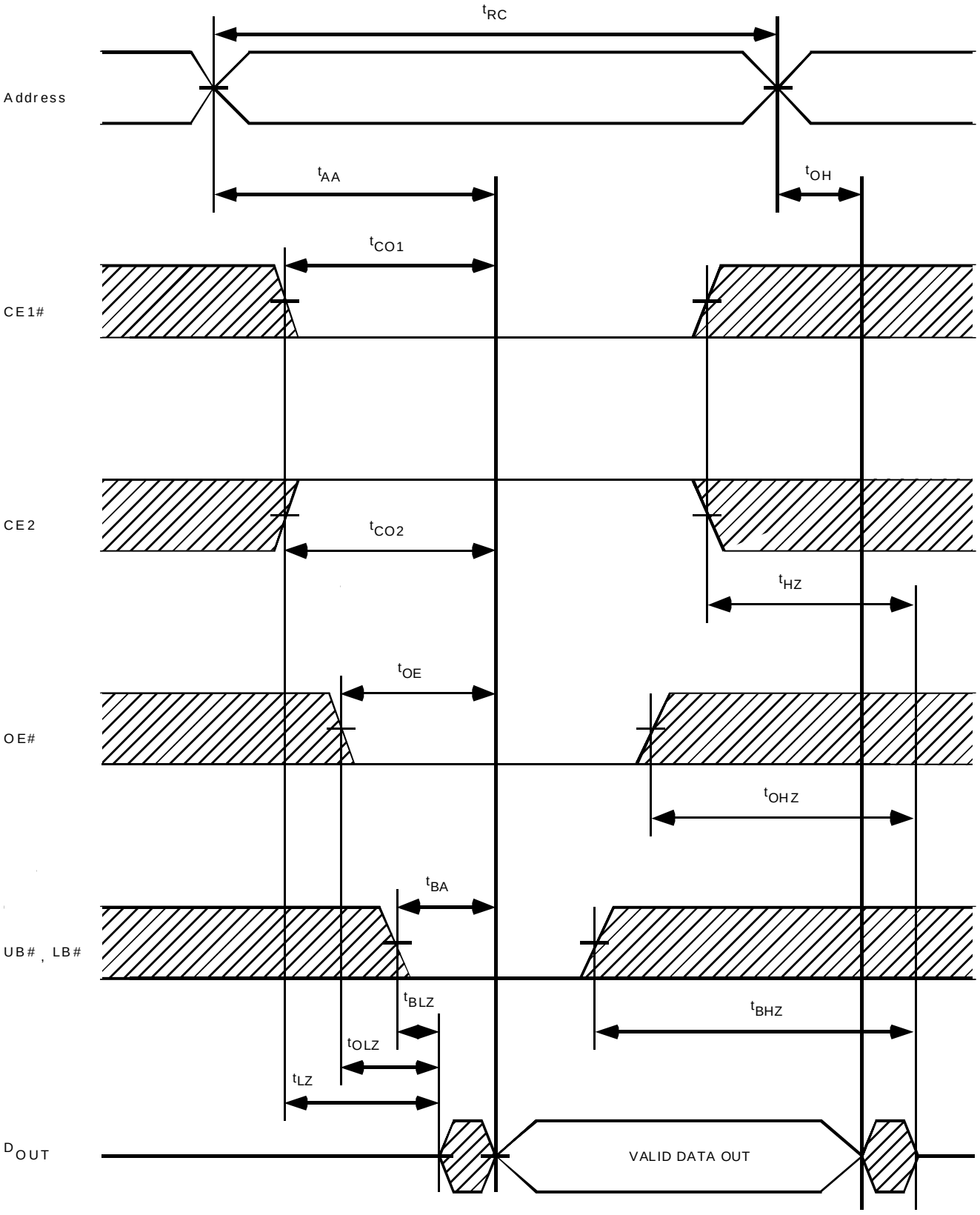
Write Cycle

Symbol	Parameter	EM562161				Unit
		-55		-70		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	55	–	70	–	ns
t_{WP}	Write pulse width	40	–	55	–	
t_{CW}	Chip Enable to end of write	45	–	60	–	
t_{BW}	Data Byte Control to end of Write	45	–	60	–	
t_{AS}	Address setup time	0	–	0	–	
t_{WR}	Write Recovery time	0	–	0	–	
t_{WHZ}	WE# Low to Output in High-Z	–	25	–	30	
t_{OW}	WE# High to Output in Low-Z	5	–	5	–	
t_{DS}	Data Setup Time	25	–	30	–	
t_{DH}	Data Hold Time	0	–	0	–	

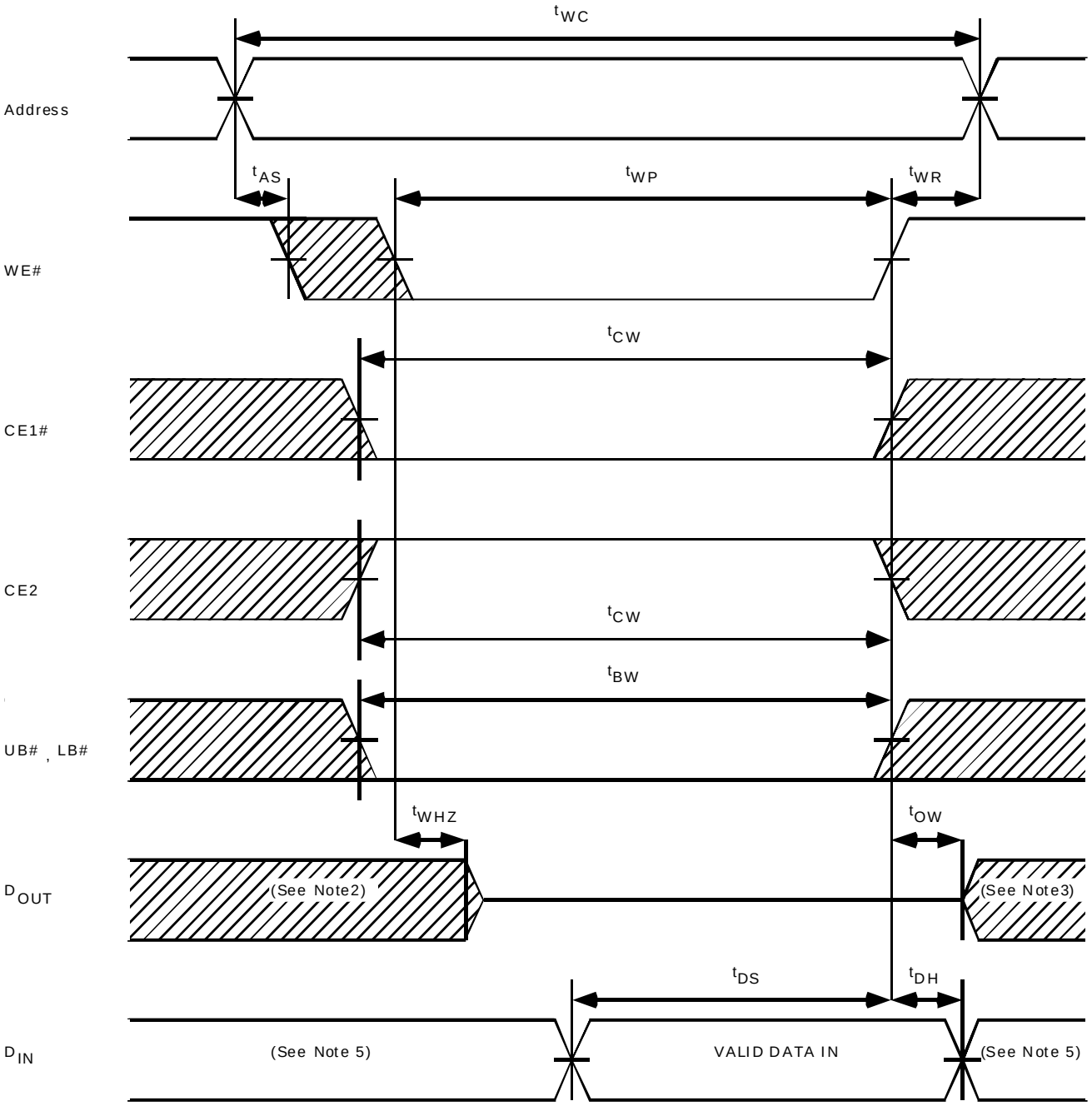
AC Test Condition

- Output load : 50pF + one TTL gate
- Input pulse level : 0.4V, 2.4V
- Timing measurements : 0.5 x V_{DD}
- tR, tF : 5ns

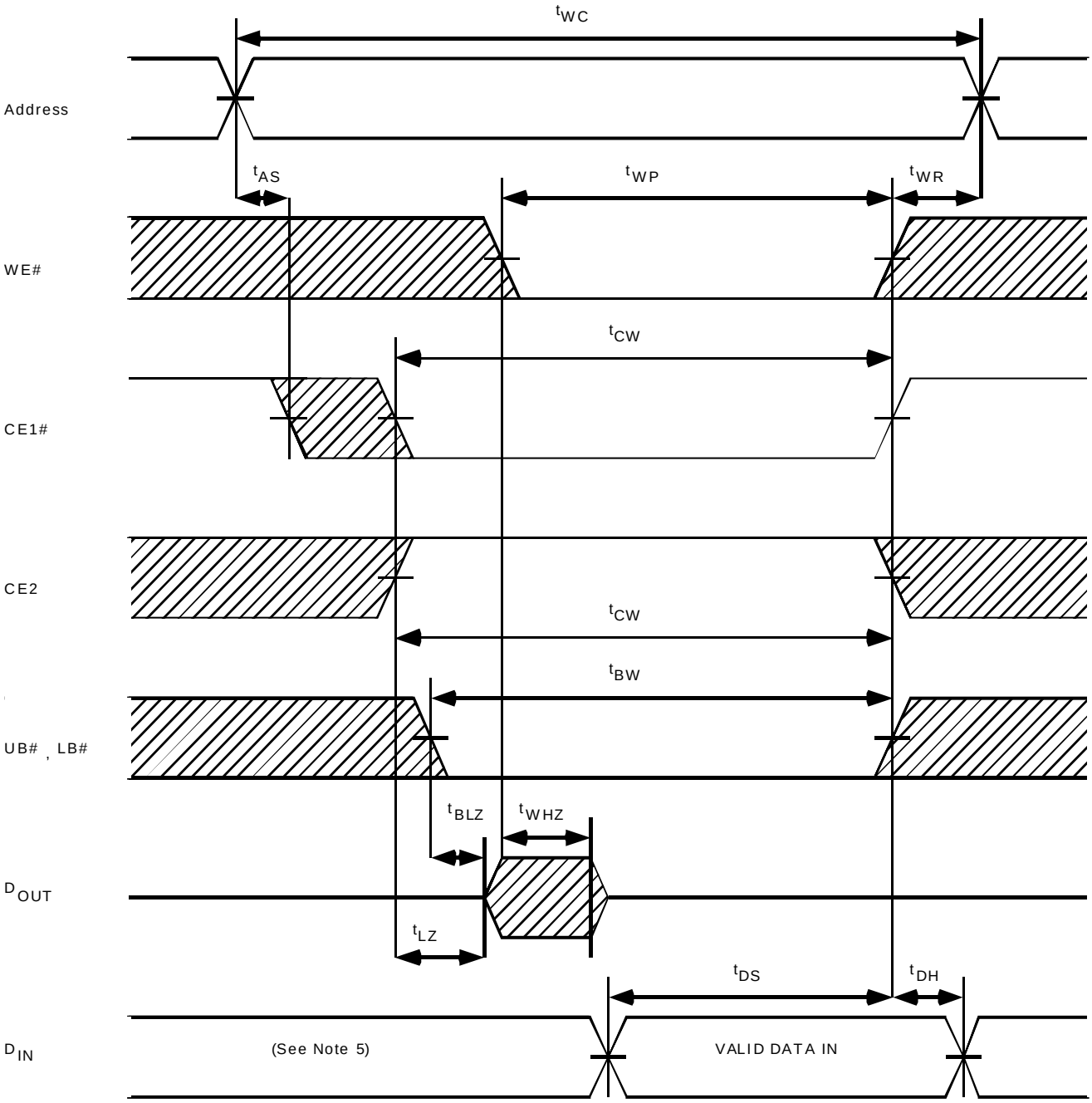
Read Cycle
(See Note 1)



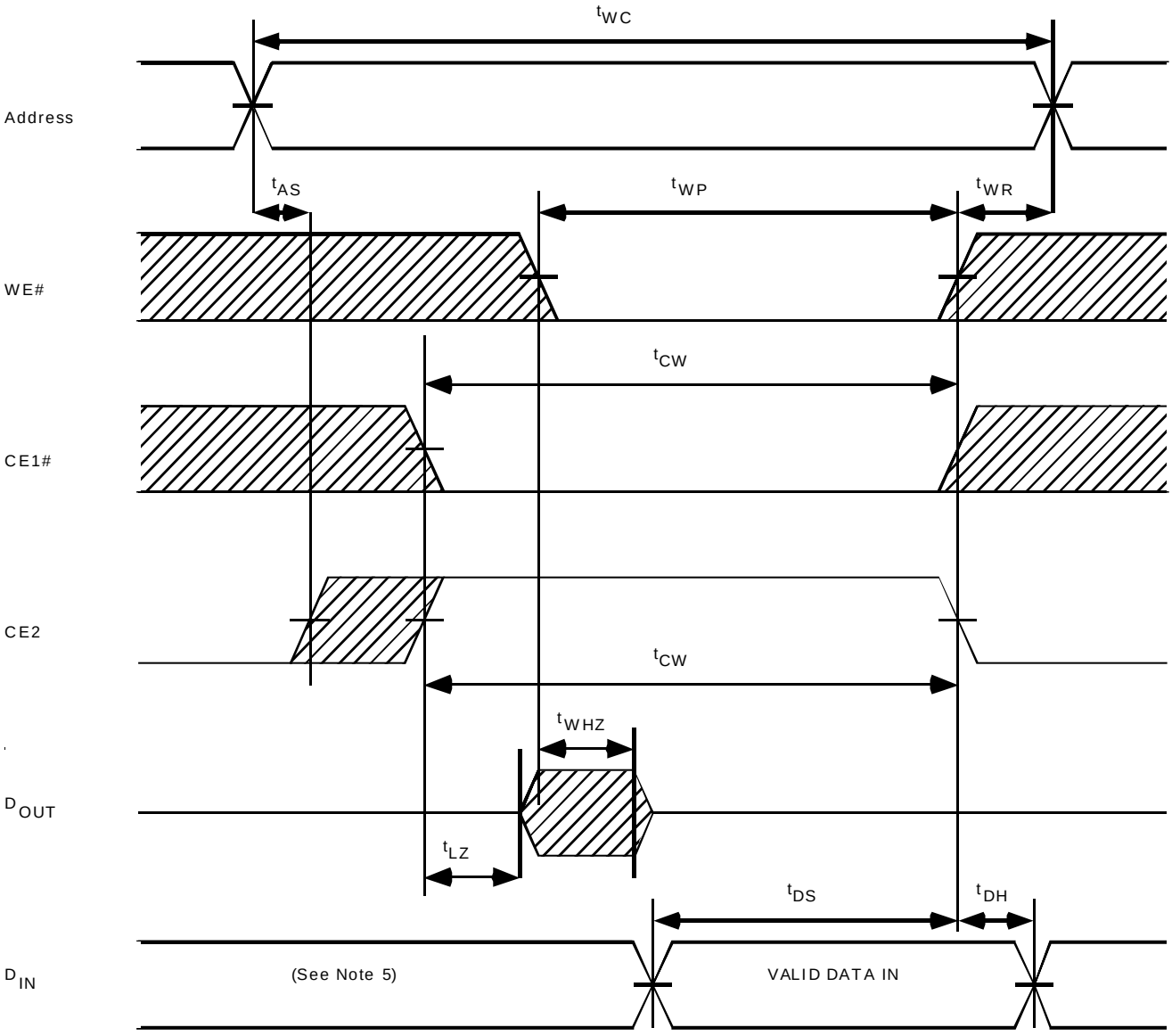
Write Cycle1
(WE# Controlled)(See Note 4)



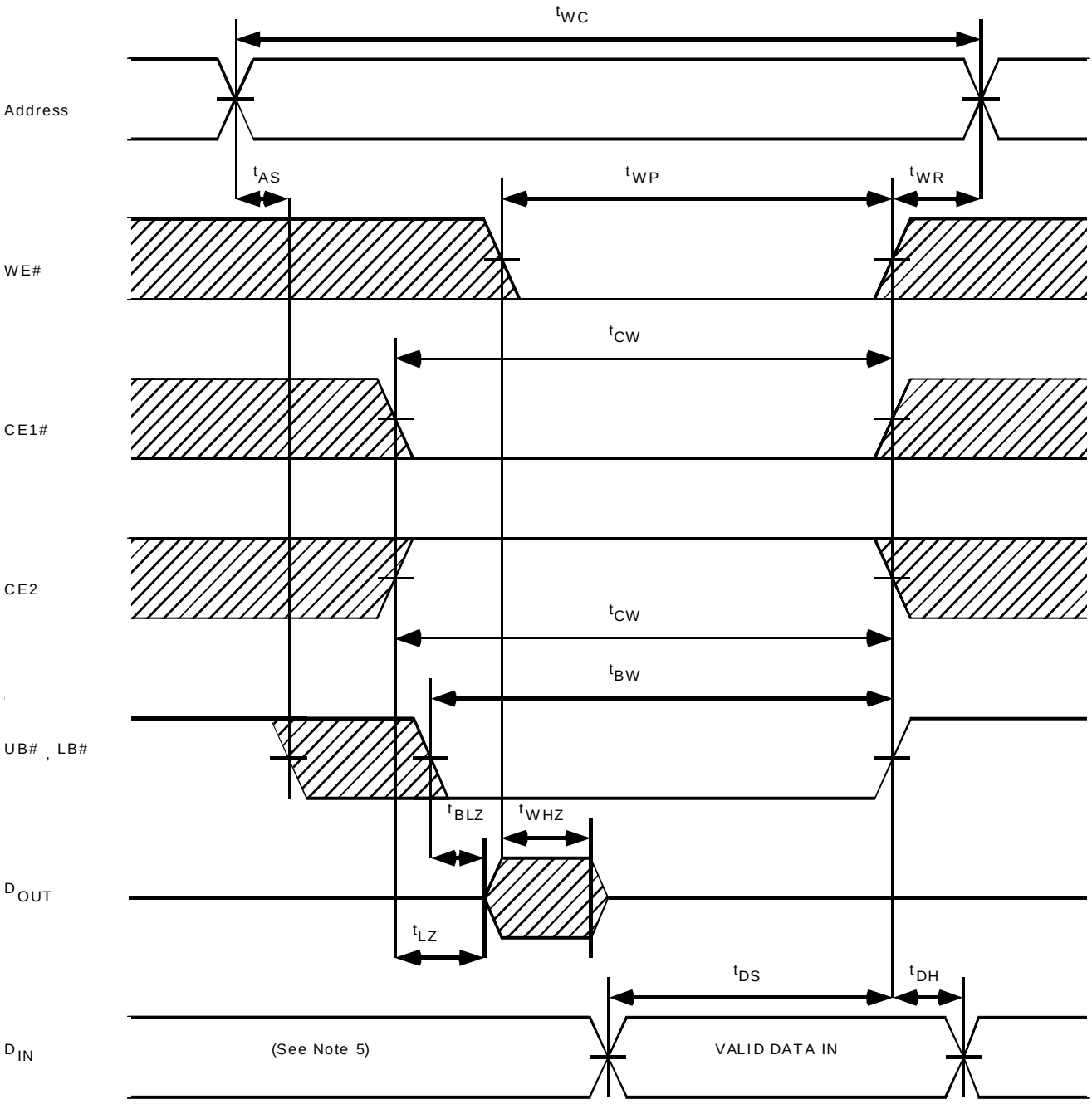
Write Cycle 2
(CE1# Controlled)(See Note 4)



Write Cycle 3
(CE2 Controlled)(See Note 4)



Write Cycle4
(UB#, LB# Controlled)(See Note 4)



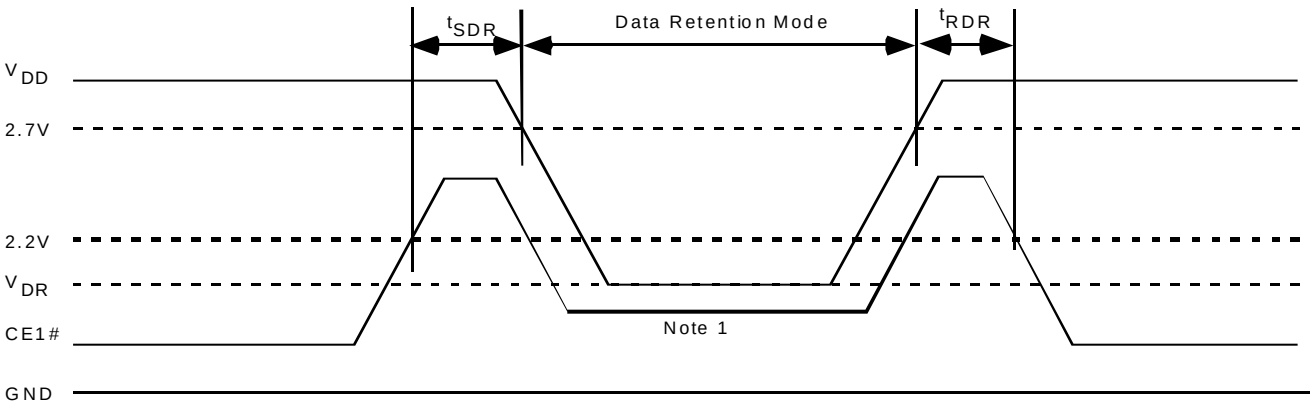
Note:

1. WE# remains HIGH for the read cycle.
2. If CE1# goes LOW (or CE2 goes HIGH) with or after WE# goes LOW, the outputs will remain at high impedance.
3. If CE1# goes HIGH (or CE2 goes LOW) coincident with or before WE# goes HIGH, the outputs will remain at high impedance.
4. If OE# is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

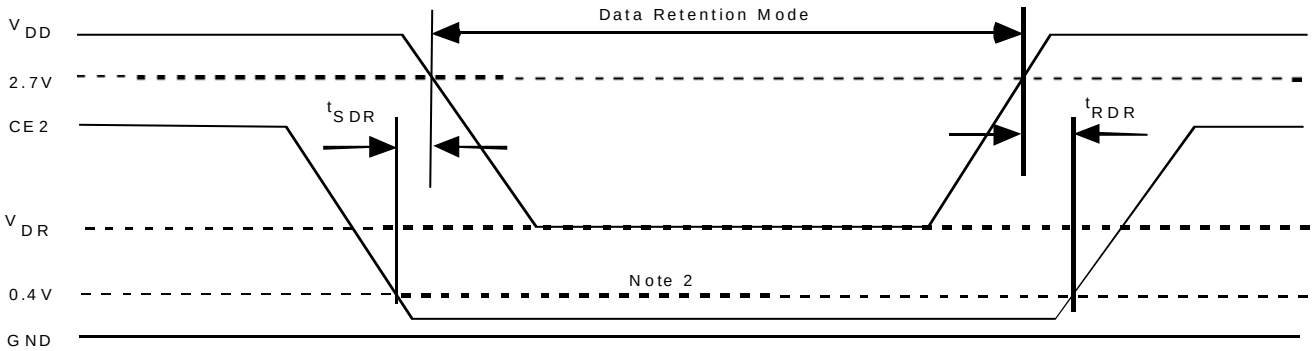
Data Retention Characteristics (Ta = -40° C to 85° C)

Symbol	Parameter		Min	Typ	Max	Unit
V_{DR}	Data Retention Supply Voltage	CE1# ≥ V_{DD} - 0.2V, CE2 ≤ 0.2V, VIN ≥ V_{DD} - 0.2V or VIN ≤ 0.2V	1.5	–	3.6	V
I_{DR}	Data Retention Current	VDD = 1.5V, CE1# ≥ V_{DD} - 0.2V, CE2 ≤ 0.2V, VIN ≥ V_{DD} - 0.2V or VIN ≤ 0.2V	–	0.5	3.0	µA
t_{SDR}	Chip Deselect to Data Retention Mode Time		0	–	–	ns
t_{RDR}	Recovery Time		t_{RC}	–	–	ns

CE1# Controlled Data Retention Mode



CE2 Controlled Data Retention Mode



Note:

1. CE1# ≥ V_{DD} – 0.2V or UB# = LB# ≥ V_{DD} – 0.2V
2. CE2 ≤ 0.2V

Package Diagrams

48-Ball (6mm x 8mm) BGA

Units in mm