



GENERAL DESCRIPTION

EM55M450/EM55Q450 series is a tiny-controller-based voice synthesizer IC which contains all the function of EM55000 series and has an MTP/QTP ROM inside.

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FEATURES

	EM55M450/EM55Q450
RAM (nibbles)	128
PROGRAM	32K*10
ROM(bits)	204Kx 10
I/O ports	4 I + 12 I/O
D/A	Green/Traditional DAC by option
OSC	Ring or Resonator type by option
Reset Pin	Yes

- Single power supply 2.4V~5.1V, suitable for 3 batteries application.
- Port1 and Port2 with wake-up function, Port3.2 with programmable IR (38KHz carry) communication function
- Power down mode for saving power consumption
- Single ROM for voice and program data
- Readable ROM code data
- One 6-bit timer overflow control
- Two stacks for subroutine calling
- 5-bit ASPCM /7-bit PCM voice synthesizer
- Multiple playing speeds in 1KHz ~22KHz for voice playback
- Multiple levels of volume control
- Traditional fixed current D/A output to drive external connected transistor for speaker or direct drive output to speaker.
- Package type:
EM55M450 COB: COB type



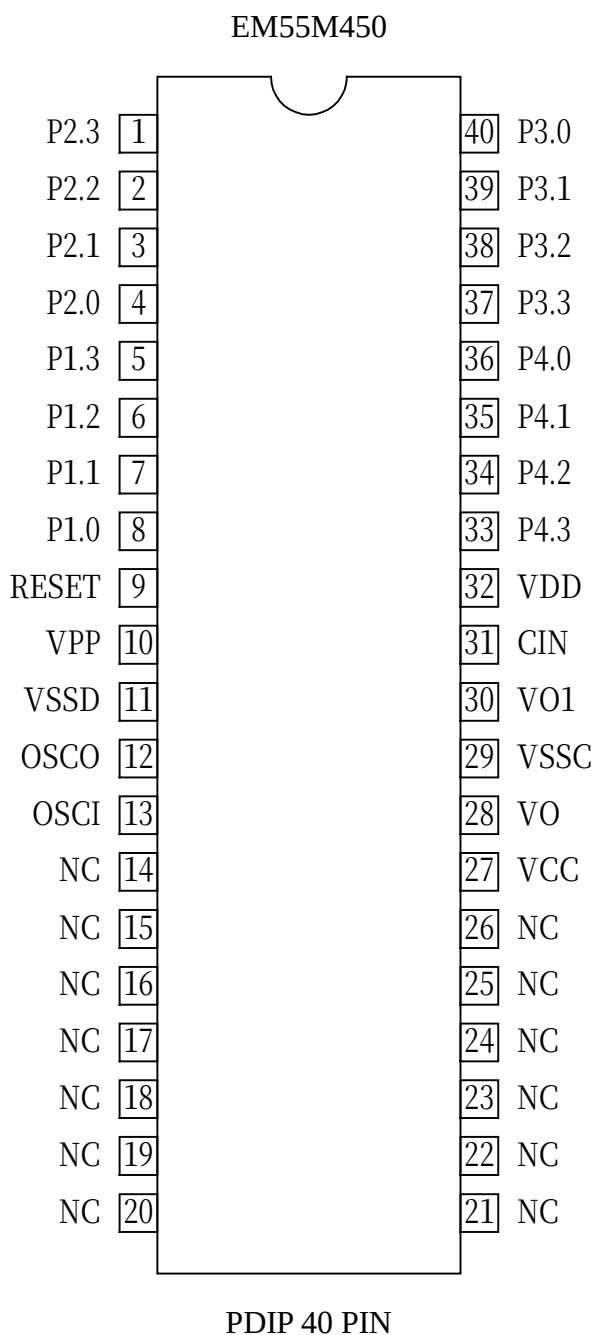
EM55M450 H: dice type

EM55M450 P: 40 PDIP package

EM55Q450 H: dice type

PIN ASSIGNMENT

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PIN DESCRIPTIONS

Symbol	I/O	Function
P1.0	I	Bit 0 of Port 1
P1.1	I	Bit 1 of Port 1
P1.2	I	Bit 2 of Port 1
P1.3	I	Bit 3 of Port 1
P2.0/ PD0	I/O	Bit 0 of Port 2 / Program data pin for parallel data bit 0,4
P2.1/ PD1	I/O	Bit 1 of Port 2 / Program data pin for parallel data bit 1,5
P2.2/ PD2	I/O	Bit 2 of Port 2 / Program data pin for parallel data bit 2,6
P2.3/ PD3	I/O	Bit 3 of Port 2 / Program data pin for parallel data bit 3,7
P3.0/ RDYB	I/O	Bit 0 of Port 3 / Program Ready signal
P3.1 / WEB	I/O	Bit 1 of Port 3 / programming write enable
P3.2 / OEB	I/O	Bit 2 of Port 3 / programming output enable
P3.3/ ACLK	I/O	Bit 3 of Port 3 / programming address increase
P4.0	I/O	Bit 0 of Port 4
P4.1	I/O	Bit 1 of Port 4
P4.2	I/O	Bit 2 of Port 4
P4.3	I/O	Bit 3 of Port 4
TEST / VPP(MTP power)	I	Test / Programming power source
VDD	I	Positive power supply
VSSD	I	Power ground
VCC	I	Analog positive power supply
VSSC	I	Analog power ground
Cin	I	Regulator capacitor
OSCI / CLK	I	Oscillation component pin / Program clock
OSCO	I	Oscillation component pin
RESET	I	RESET pin (active high)
VO1	O	Push Pull voice output
VO	O	Constant current output / Push Pull voice output

ABSOLUTE MAXIMUM RATING

Items	Symbol	Min	Max	Unit
Supply Voltage	$V_{DD}-V_{SS}$	-0.3	6.0	V
Input Voltage	V_{IN}	$V_{GND}-0.3$	$V_{DD}+0.3$	V
Operating Temperature	T_{OP}	0.0	+70.0	$^{\circ}C$
Storage Temperature	T_{STG}	-25.0	+125.0	$^{\circ}C$

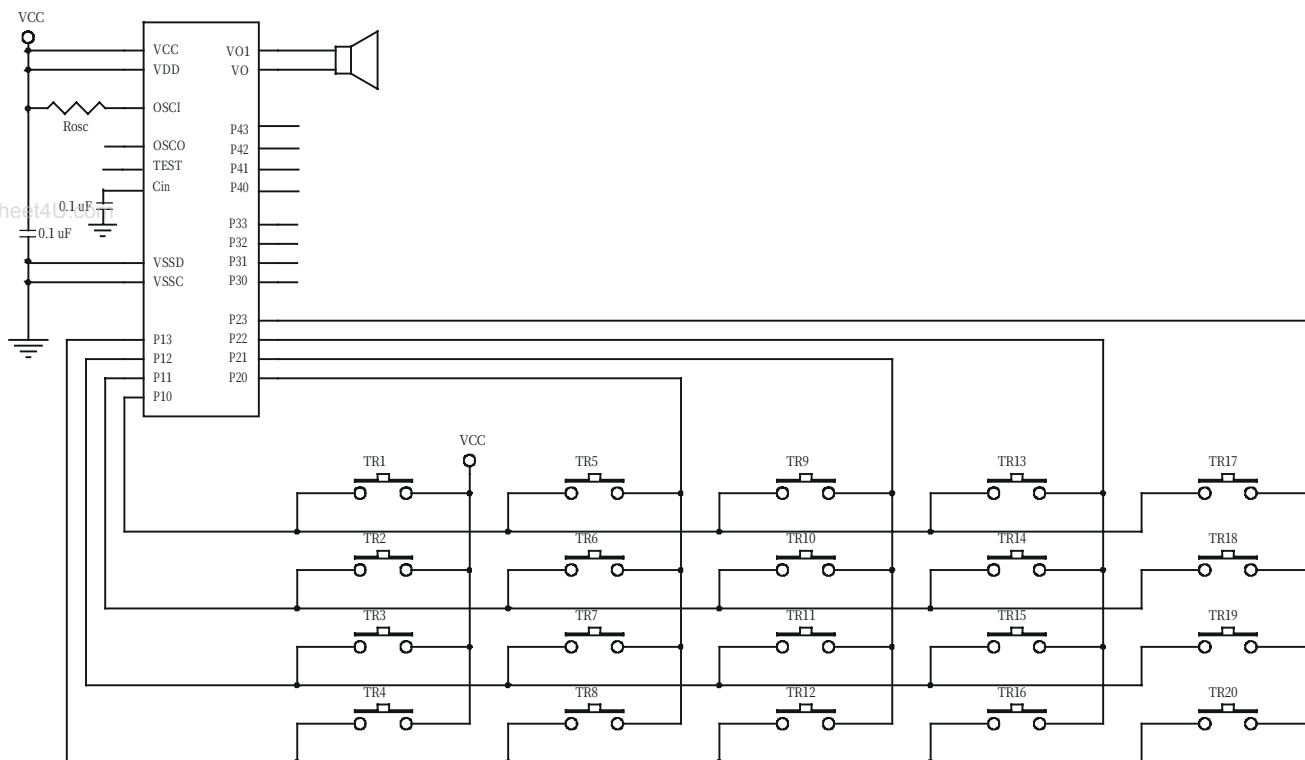
**ELECTRICAL CHARACTERISTICS** ($V_{DD}=3V$, $25^{\circ}C$ unless otherwise specified)

Items	Sym.	Min	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	5.1	V	
Standby current	I_{DDs}	-	-	2	μA	no load
operating current	I_{DDO}	-	1.8	3.5	mA	no load, traditional D/A operate
operating current	I_{DDO}	-	3	6	mA	no load, Green voice D/A operate
Drive current of P2,P3, P4	I_{OD}	2.0	3.0	-	mA	$V_O=2.4V$
Sink current of P2 (before KEYB)	I_{OS}	-	3.0	10.0	μA	$V_O=3V$
Sink current of P2 (after KEYB)	I_{OS}	2.3	3.5	-	mA	$V_O=0.4V$
Sink current of P3,P4	I_{OS}	2.3	3.5	-	mA	$V_O=0.4V$
Input current of P1	I_{IH}	-	3.0	10.0	μA	$V_O=3V$
Output current of VO	I_{VO}	4.0	5.0	6	mA	$V_O=0.7V$, traditional D/A operate
Output sink current of VO1, VO	I_{VO}	120	150.		mA	$V_O=V_{O1}=1.5V$, Green voice D/A operate
Oscillation resistor	R	-	100	-	$K\Omega$	
Oscillation freq.	F_{OSC}	1.08	1.20	1.32	MHz	osc=100 $K\Omega$

DC PROGRAMMING CHARACTERISTICS:

Items	Sym.	Min.	Typ.	Max.	Unit	Test Conditions
VDD programming voltage	VDD	4.7	5.0	5.3	V	
VDD erase voltage	VDD	4.7	5.0	5.3	V	
VPP voltage(programming process)	VPP	11.3	12	12.7	V	
Input current	I_{IN}	-	-	7	μA	$V_{DD} = 5V$, $V_{IN} = 0 \sim V_{DD}$
Output high voltage	V_{OH}	2.4	2.4	-	V	$I_{OH} = 400\mu A$
Output low voltage	V_{OL}	-	-	0.4	V	$I_{OL} = 2.1mA$
VDD supply current	I_{DD}	-	-	100	mA	$V_{DD}=5V$
VPP supply current	I_{PP}	-	-	50	mA	$V_{PP}=12V$

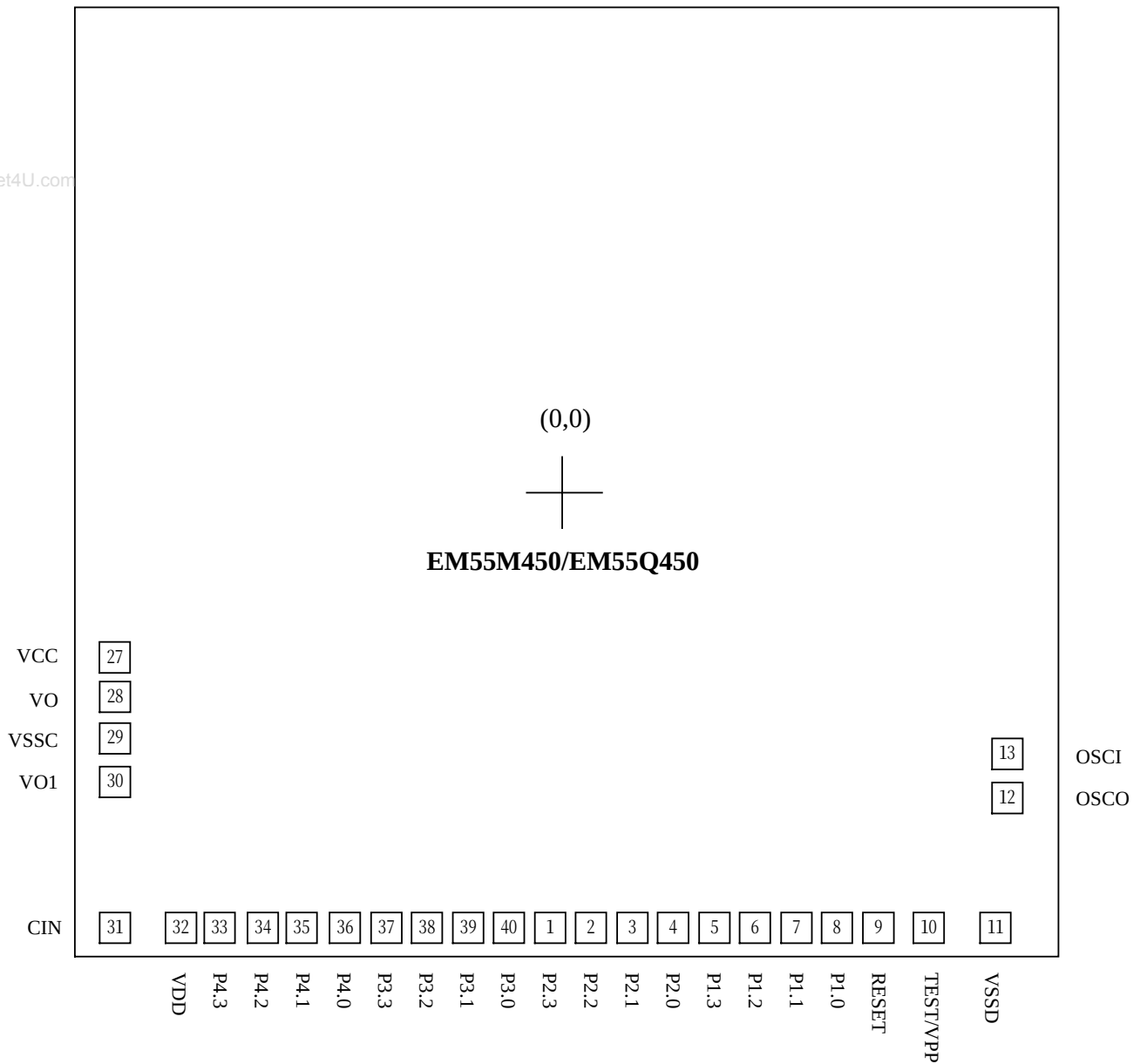
APPLICATION CIRCUIT



Note : It should add a 0.1 uF ceramic capacitor between Cin and ground.
It is suggested to add a 0.1 uF ceramic capacitor between VDD and VSS.



PAD DIAGRAM





Pin NO.	Symbol	X	Y	Pin NO.	Symbol	X	Y
1	P2.3	-2.0	-1356.0	21	NC		
2	P2.2	118.1	-1356.0	22	NC		
3	P2.1	238.1	-1356.0	23	NC		
4	P2.0	358.0	-1356.0	24	NC		
5	P1.3	478.1	-1356.0	25	NC		
6	P1.2	598.0	-1356.0	26	NC		
7	P1.1	718.1	-1356.0	27	VCC	-1311.0	-616.0
8	P1.0	838.0	-1356.0	28	VO	-1311.0	-736.0
9	RESET	958.0	-1356.0	29	VSSC	-1311.0	-856.0
10	TEST/VPP	1101.5	-1356.0	30	VO1	-1311.0	-976.0
11	VSSD	1276.0	-1356.0	31	CIN	-1282.7	-1356.0
12	OSCO	1304.0	-1013.4	32	VDD	-1082.0	-1356.0
13	OSCI	1304.0	-893.4	33	P4.3	-962.0	-1356.0
14	NC			34	P4.2	-842.0	-1356.0
15	NC			35	P4.1	-722.0	-1356.0
16	NC			36	P4.0	-602.0	-1356.0
17	NC			37	P3.3	-481.9	-1356.0
18	NC			38	P3.2	-362.0	-1356.0
19	NC			39	P3.1	-242.0	-1356.0
20	NC			40	P3.0	-122.0	-1356.0

Chip size : 2920*3020 um

For PCB layout, IC substrate must be connected to VSSD.