1A Low Dropout LDO

General Description

EM5105 is a 1A low dropout linear regulator designed for low dropout and high current applications. This device works with dual supplies, a control input for the control circuitry and a power input as low as 1.1V for providing current to output. It features 1A output current and ultra-low-drop output voltage as well as full protection functions. V_{OUT} can be as low as 0.8V.

The other features include soft start, under voltage protection, current limit protection, Power-On-Reset function, and over temperature protection. The EM5105 is available in DFN3x3-10L package.

Ordering Information

Part Number	Package	Remark
EM5105VT	DFN3x3-10L Lead-Free	

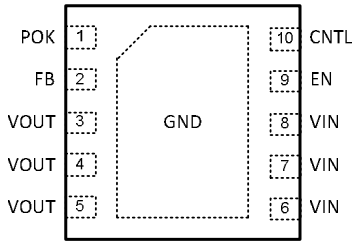
Features

- V_{IN} Range 1.1V to 6.0V
- V_{OUT} is Adjustable (0.8V Min)
- Excellent Line Regulation
- Excellent Load Regulation
- 1A Guaranteed Output Current
- 300mV @ 1A Dropout Voltage
- Very Low On-Resistance
- Enable & Power good Signal
- VOUT Under Voltage Protection
- Current Limit Protection
- Over Temperature Protection
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

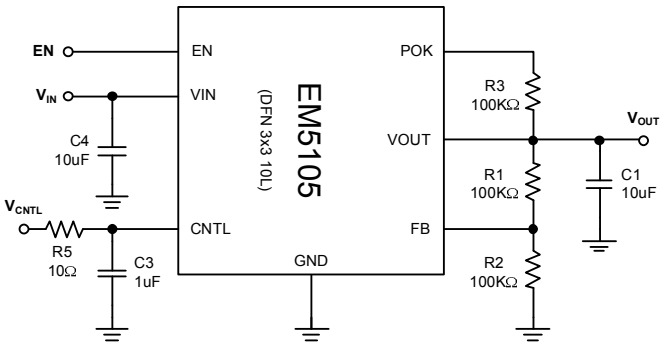
- Notebook & Netbook
- Graphic Cards & MB
- Low Voltage Logic Supplies
- Chipset Supplies
- Server System
- SMPS Post Regulators

Pin Configuration



DFN3x3-10L

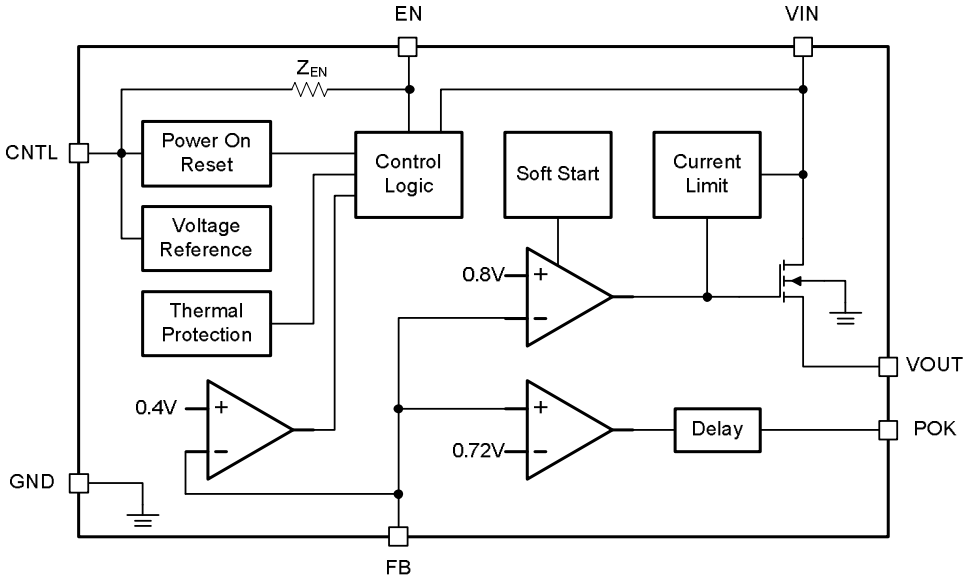
Typical Application Circuit



Pin Assignment

Pin Name	Pin No.	Pin Function
POK	1	**Power OK Indication.** POK is an open-drain output. An external pull high resistor connected to this pin is required.
FB	2	**Feedback Voltage.** FB is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage as V_{OUT} = (1 + R1/R2) x 0.8V (V). This pin has high impedance and should be kept from noisy source to guarantee stable operation.
VOUT	3~5	**Output Voltage.** V_{OUT} is power output pin. An internal pull low resistance exists when the device is disabled. Minimum 10uF low ESR ceramic holding capacitor is required at this pin for stabilizing V_{OUT} voltage.
VIN	6~8	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. Minimum 10uF low ESR ceramic capacitor is recommended at this pin.
EN	9	**Enable Input.** Pulling the pin below 0.3V turns the regulator off
CNTL	10	**Supply Input for Control Circuit.** CNTL provides supply voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the V_{CNTL}.
GND	Exposed Pad	**Ground.**

Function Block Diagram



Absolute Maximum Ratings (Note1)

- V_{IN} ---------- -0.3V to +6.0V
- V_{CNTL} ---------- -0.3V to +6.0V
- Other Pins---------- -0.3V to (V_{CNTL}+0.3V)
- Package Thermal Resistance,θ_{JA}, DFN3X3-10L ---------- 60°C/W
- Power Dissipation, PD @ TA = 25°C, DFN3X3-10L ---------- 1.67W
- Junction Temperature---------- 150°C
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Storage Temperature ---------- –65°C to 150°C
- ESD susceptibility (Note3)
  HBM (Human Body Mode)---------- 2KV
  MM (Machine Mode)---------- 200V

Recommended Operating Conditions (Note4)

- Control Voltage, V_{CNTL} ---------- +3.0V to +6V
- Supply Input Voltage, V_{IN} ---------- +1.1V to V_{CNTL}
- Junction Temperature ---------- –40°C to 125°C
- Ambient Temperature ---------- –40°C to 85°C

Electrical Characteristics

V_{CNTL}=5V, T_A=25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Section						
Control Input Voltage	V_{CNTL}	V_{OUT}= V_{REF}	3.0	-	6	V
POR Threshold	$V_{CNTLRTH}$		2.5	-	2.9	V
POR Hysteresis	$V_{CNTLHYS}$		-	0.4	-	V
Power Input Voltage	V_{IN}	V_{OUT}=V_{REF}	1.1	-	V_{CNTL}	V
VIN POR Threshold	V_{VINTH}		0.8	-	1.0	V
VIN POR Hysteresis	V_{VINHYS}		0.2	-	0.5	V
VN POR Deglitch Time			-	100	-	us
Control Input Current in Shutdown	I_{CNTL_SD}	V_{IN}=V_{CNTL}=5V, I_{OUT}=0A,V_{EN}=0V	-	10	30	uA
Quiescent Current	I_Q	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A	-	1.0	1.5	mA
Feedback						
Reference Voltage	V_{REF}	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	0.792	0.8	0.808	V
V_{IN} Line Regulation	$V_{REF(LINE)}$	1.1V<V_{IN}<5V, V_{CNTL}=V_{EN}=5V	-	0.01	0.1	%/V
Load Regulation (Note 5)	$V_{REF(LOAD)}$	0<I_{OUT}<1A, V_{IN}=V_{CNTL}=V_{EN}=5V	-	0.1	0.5	%/A
Dropout Voltage (Note 6)	V_{DROP}	I_{OUT}=1A, V_{CNTL}=V_{EN}=5V, V_{OUT}=1.2V	-	300	400	mV
V_{OUT} Pull Low Resistance		V_{EN}=0V, sinking current=5mA	-	-	150	Ω
Enable						
Enable High Level	V_{EN}		1.1	-	-	V
Disable Low Level	V_{SD}		-	-	0.3	V
Enable Source Current	I_{EN}	V_{CNTL}=5V, V_{EN}=0V	-	5	10	µA
Enable Input Impedance	Z_{EN}		500	-	-	KΩ
Output Voltage Ramp Up Time			0.6	1	2	ms

PWROK						
POK Threshold	V_{POKTH_R}	VFB Rising	90	-	94	%
	V_{POKTH_F}	VFB Falling	80	-	84	%
POK Sinking Voltage	V_{POK}	sinking current= 5mA	-	-	0.4	V
POK Delay Time		From V_{OUT}>92% to POK rising	1	2	4	ms
Protection						
OCP Threshold Level	I_{OCP}		1.2	1.8	-	A
Under Voltage Threshold	V_{UVP}	VFB Falling	-	0.4	-	V
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}		-	170	-	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		-	40	-	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A=25°C on a 4-layers high effective thermal conductivity test board with minimum copper area of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

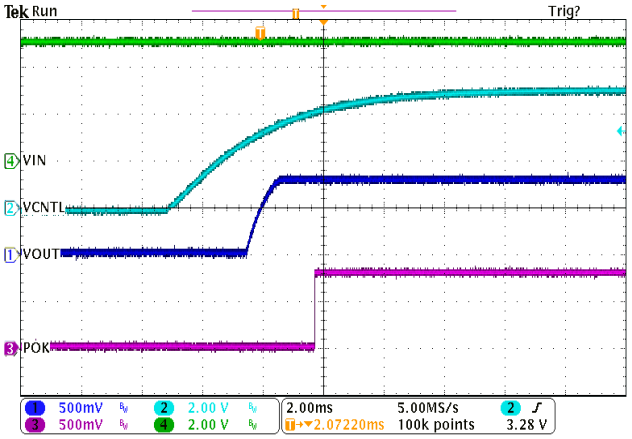
Note 5. Load regulation is measured by a current pulse with 50Hz frequency and 10% duty cycle.

Note 6. The dropout voltage is defined as (V_{IN}-V_{OUT}), which is measured when V_{OUT} equal to ($V_{OUT,(NORMAL)}$-100mV).

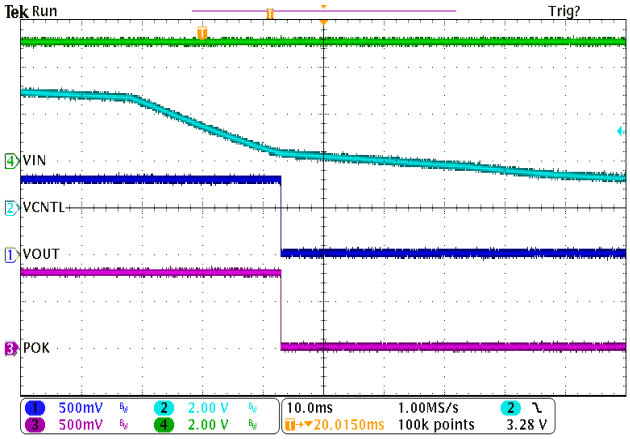
Typical Operating Characteristics

V_{IN}=5V；V_{CNTL}= V_{EN}=5V；V_{OUT}=0.8V；C_{IN}=10uF；C_{OUT}=10uF

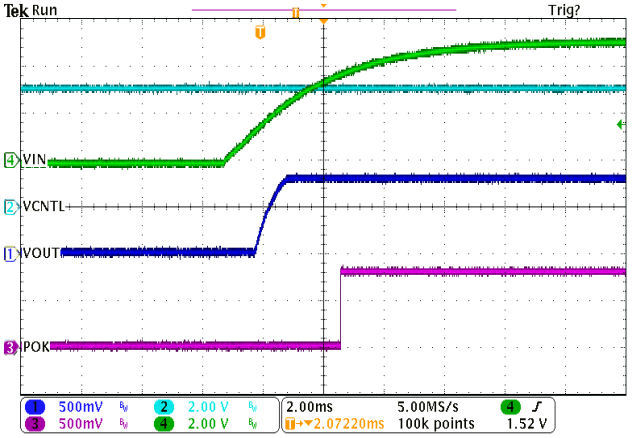
Power On from V_{CNTL}
No Load



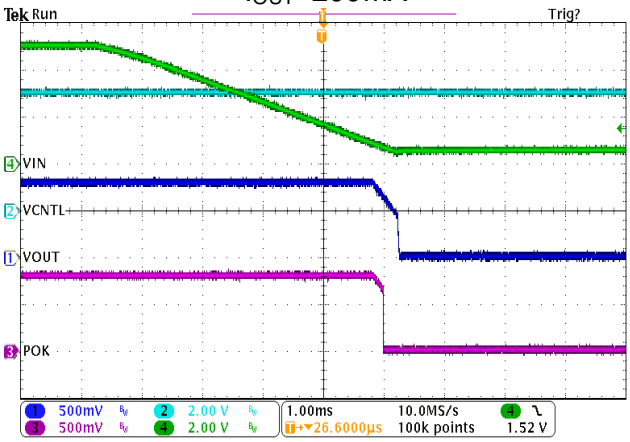
Power Off from V_{CNTL}
I_{OUT}=200mA



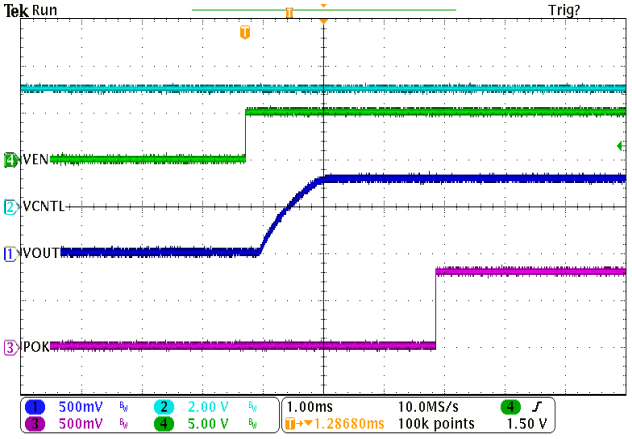
Power On from V_{IN}
No Load



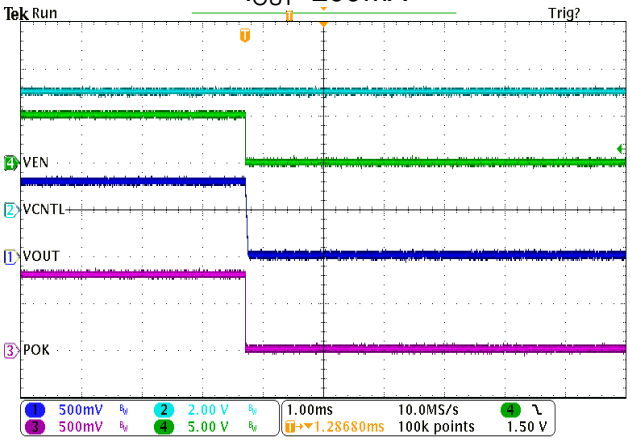
Power Off from V_{IN}
I_{OUT}=200mA



Power On from V_{EN}
No Load

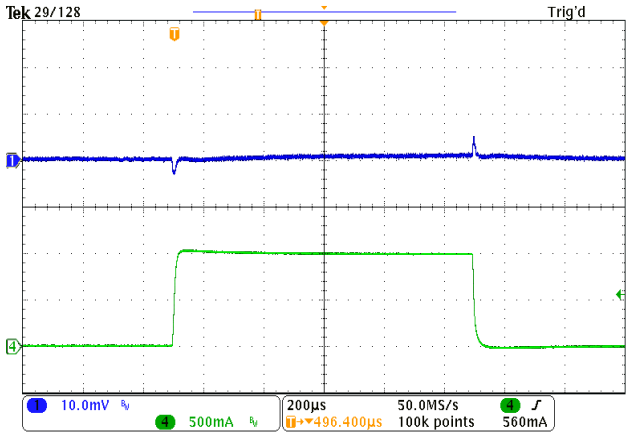


Power Off from V_{EN}
I_{OUT}=200mA



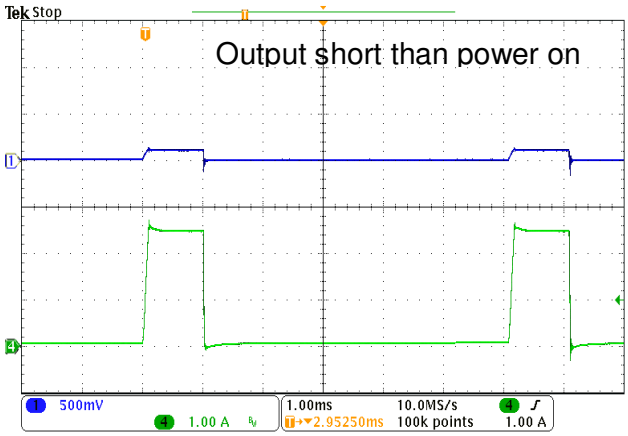
Load Transient Response

I_{OUT}=0 to 1A；Rise＝0.25A/us



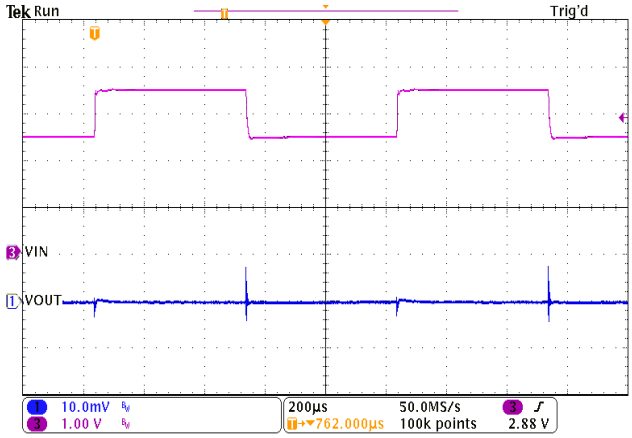
OCP Test

V_{IN}=5V；V_{CNTL}= V_{EN}=5V



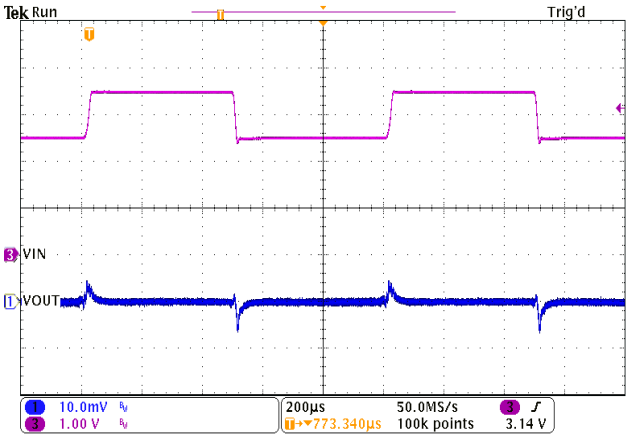
V_{IN} Line Transient Response

V_{IN}=2.5 to 3.5V；I_{OUT}=0A

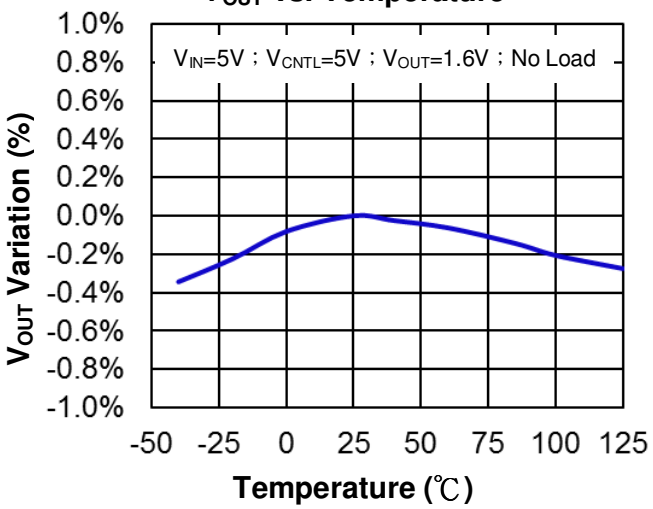


V_{IN} Line Transient Response

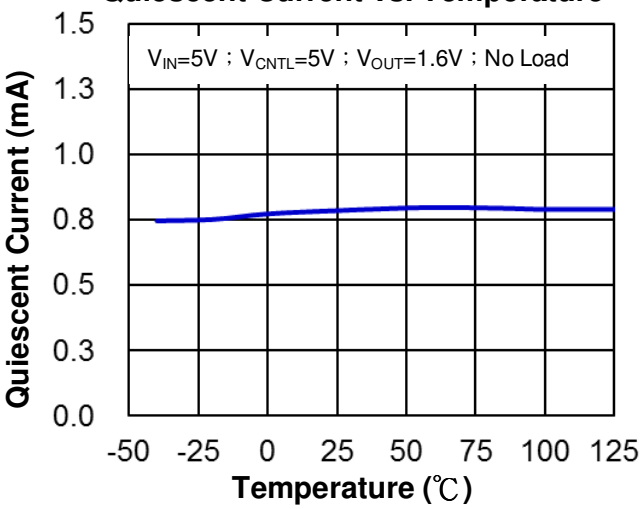
V_{IN}=2.5 to 3.5V；I_{OUT}=1A



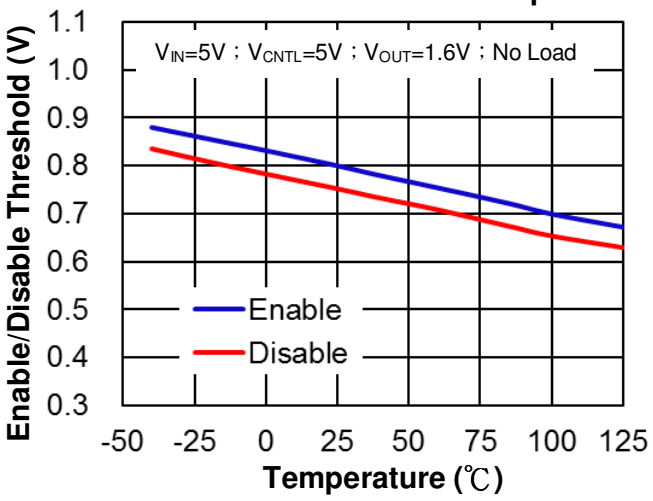
V_{OUT} vs. Temperature



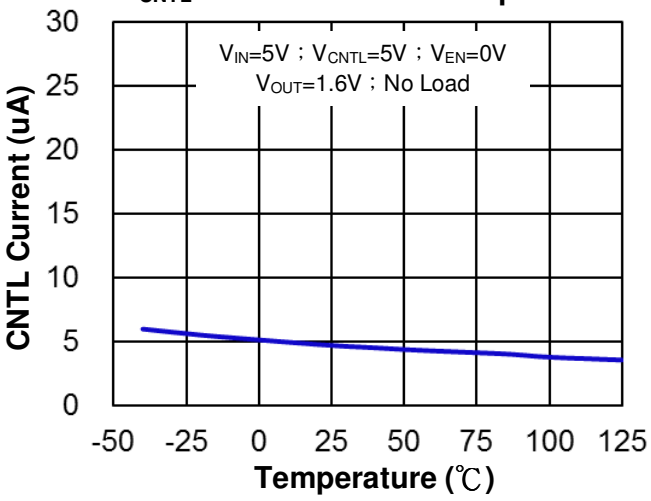
Quiescent Current vs. Temperature



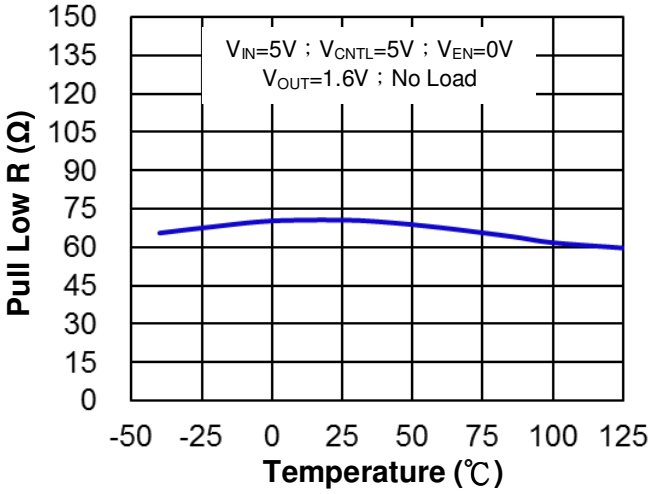
En/Disable Threshold vs. Temperature



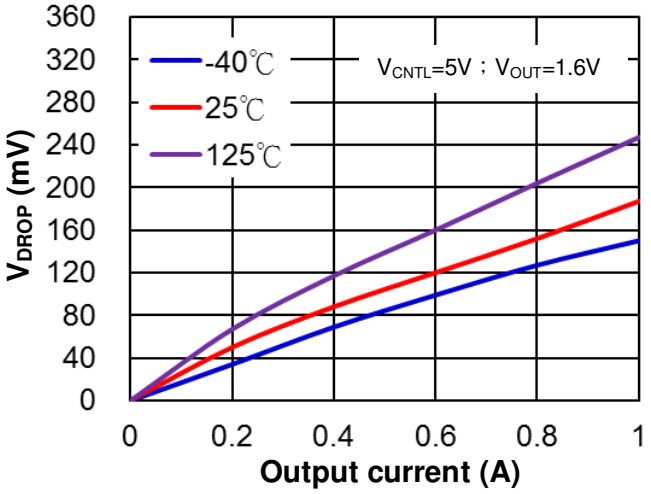
I_{CNTL} in Shutdown vs. Temperature



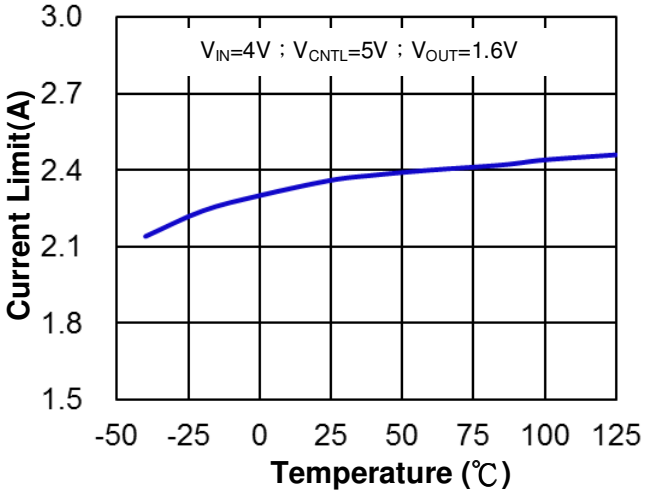
Pull low Resistance vs. Temperature



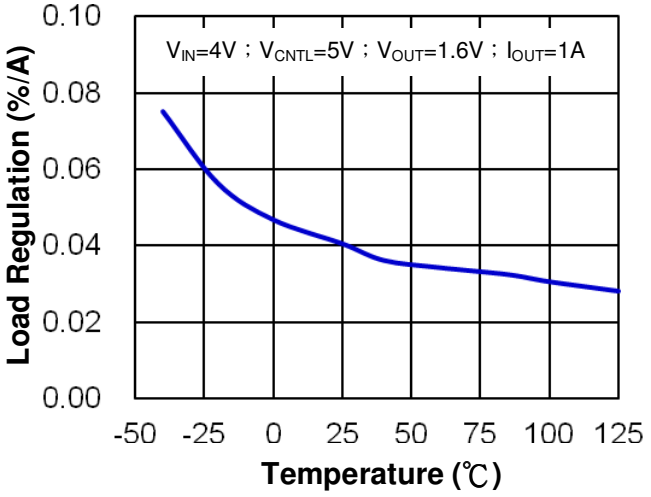
V_{DROP} vs. Temperature

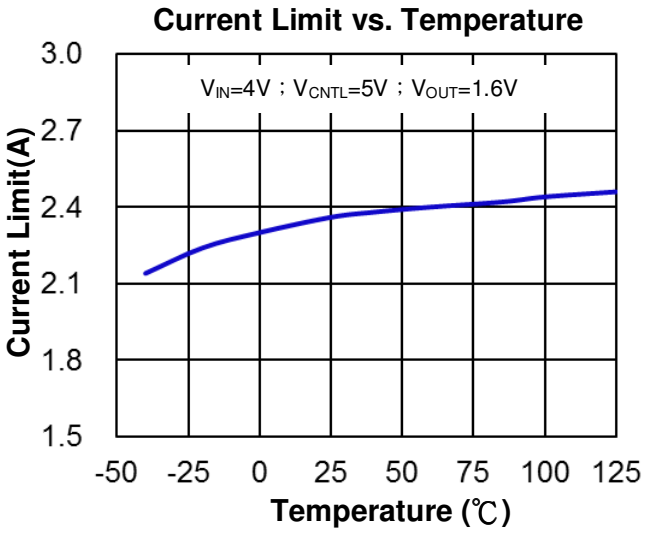


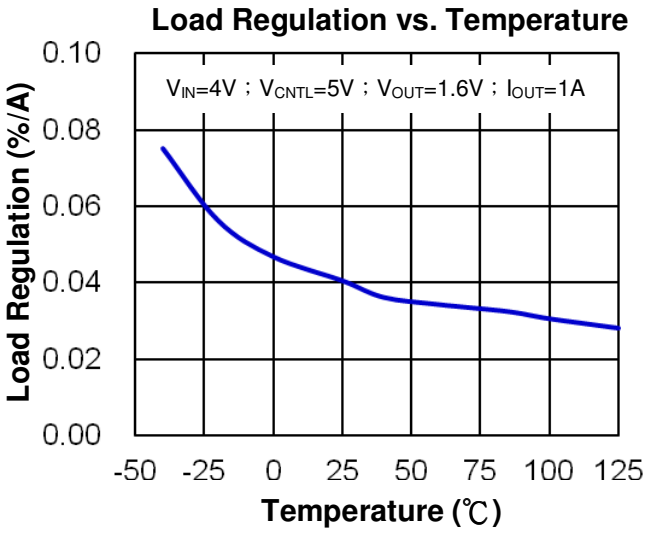
Current Limit vs. Temperature

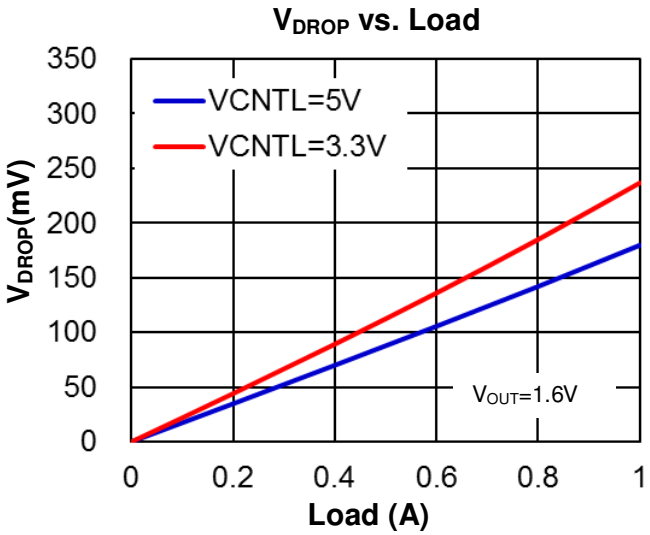


Load Regulation vs. Temperature




Current Limit vs. Temperature
VIN=4V；VCNTL=5V；VOUT=1.6V
Current Limit(A)
3.0
2.7
2.4
2.1
1.8
1.5
-50 -25 0 25 50 75 100 125
Temperature (℃)


Load Regulation vs. Temperature
VIN=4V；VCNTL=5V；VOUT=1.6V；IOUT=1A
Load Regulation (%/A)
0.10
0.08
0.06
0.04
0.02
0.00
-50 -25 0 25 50 75 100 125
Temperature (℃)


VDROP vs. Load
VCNTL=5V
VCNTL=3.3V
VOUT=1.6V
VDROP(mV)
350
300
250
200
150
100
50
0
0 0.2 0.4 0.6 0.8 1
Load (A)

Functional Description

Enable Function

EM5105 is enabled if the voltage of the EN pin is greater than 1.1V. If the voltage of the EN pin is less than 0.3V, the IC will be disabled. The quiescent current can be decreased to be less than 10uA typically.

POR – Power ON Reset

To let EM5105 start to operation, CNTL voltage must be higher than its POR voltage even when EN voltage is pulled higher than enable high voltage. Typical POR voltage is 2.7V.

VOUT Voltage Adjustment

The VOUT voltage of EM5105 can be adjusted by external voltage divider. Refer to typical application circuit, VOUT voltage is calculated by the following equation,

V_{OUT} = (1 + R1/R2) x 0.8V

Over Current Limit Function

EM5105 features over current limiting function which can limit its output current to 1.8A. When current limit lasts over one millisecond, IC turns-off the power device for few milliseconds and then re-starts.

Input and Output Capacitor Selection

For CNTL pin, a 1uF ceramic capacitor is enough for bypass the supply of CNTL to GND. For VIN pin, 10uF or larger ceramic capacitor is required to provide bypass path in transient current demand. VOUT pin is also recommended to have 10uF or larger ceramic capacitor to be stable and reduce the VOUT voltage dip when fast loading transient is happened. A feed-forward capacitor can be placed between VOUT and FB pin to speed up the transient response, optionally.

Power Dissipation

The max power depends on some conditions, including of thermal impedance, PCB layout, airflow, and so on. The max power dissipation can be calculated by the formula as below

$P_{D(max)}=(T_{J(max)}-T_A) / \theta_{JA}$

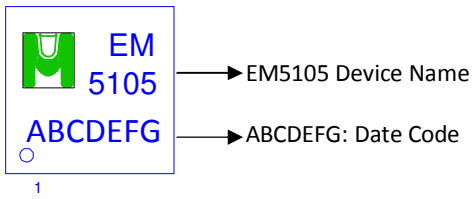
$T_{J(max)}$ is the max junction temperature; θ_{JA} is the thermal impedance from junction to ambient. The thermal impedance θ_{JA} of DFN3x3-10L is package design and PCB design dependent. The thermal impedance can be reduced by increasing the copper area under the exposed pad of the DFN3x3-10L package. So, to let the copper area as large as possible is helpful for the thermal performance of the DFN3x3-10L package.

For recommended specification of EM5105, the max junction temperature is 125 degree C. The θ_{JA} of DFN3x3-10L is 60°C/W on the standard JEDEC 51-7(4 layers, 2S2P, copper 2 oz) thermal test board. The max power dissipation (at 25°C ambient, on the min exposed pad layout) can be calculated as below:

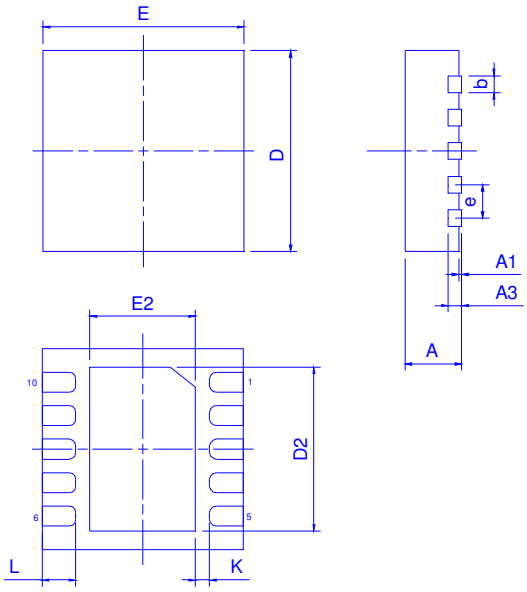
$P_{D(max\ at\ 25°C)}$=(125°C–25°C)/(60°C/W) = 1.67W

Marking Information

Device Name: EM5105VT for DFN3X3-10L



Outline Drawing



Dimension in mm

Dimension	A	A1	A3	b	D	E	D2	E2	e	L	K
Min.	0.7	0.00		0.18			2.20	1.40		0.30	0.20
Typ.	0.75	0.02	0.2	0.25	3.0	3.0			0.50	0.40	
Max.	0.80	0.05		0.30			2.70	1.75		0.50	