ELM73xxxxxA CMOS Voltage detector with delay circuit and Manual Reset function

■General description

ELM73xxxxxA is CMOS voltage detector IC with delay function; delay time is adjustable by external capacitor. It operates with very low current consumption; 260nA(typ.). The type with Manual Reset function is also available in ELM73xxxBxA series; reset condition can be manually asserted at any time. There are two output forms available; N-ch opendrain and CMOS output. The output logic is positive, therefore, the output becomes low level when VDD is lower than detection voltage. The standard detection voltages are 2.2V, 2.7V, 3.0V and 4.0V; ELM73 series can also be made as semi-custom IC within the range of 1.4~5.0V by 0.1V step.

■Features

- Detection voltage range : 1.4V to 5.0V (by 0.1V step)
- Low power operation : Typ.260nA(Vdd=VdetN+1V)
- Accuracy of detection voltage : ±30mV (VdetN<2.5V)
  ±1.2% (VdetN≥2.5V)
- Accuracy of delay time : Typ.15% (ExtC=4.7nF)
- Hysteresis voltage : Typ.VdetN×1.04
- Manual reset input : MR pin (ELM73xxxBxA only, Built-in pull-up resistor)
- Package : SC-82AB(SOT-343), SC-70-5(SOT-353), SOT-25

■Application

- Reset for microcomputers
- Voltage power shortage detectors
- Switch of back up power source
- Battery checkers

■Maximum absolute ratings

Parameter	Symbol	Limit	Unit
Power supply voltage	Vdd	Vss-0.3 to 7.0	V
Apply voltage to OUT pin	Vout	N-ch : Vss-0.3 to 7.0	V
		CMOS : Vss-0.3 to Vdd+0.3	
Apply voltage to ExtC pin	VExtC	Vss-0.3 to Vdd+0.3	V
Apply voltage to MR pin	Vmr	Vss-0.3 to Vdd+0.3	V
Output current	Iout	100	mA
Power dissipation	Pd	250 (SOT-25)	mW
		150 (SC-82AB (SOT-343))	
		150 (SC-70-5 (SOT-353))	
Operating temperature	Top	-40 to +85	°C
Storage temperature	Tstg	-55 to +125	°C

■Selection guide

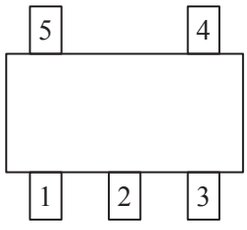
ELM73xxxxxA-x

Symbol		
a, b	Detection voltage	e.g. : 22: VdetN=2.2V, 27: VdetN=2.7V 30: VdetN=3.0V, 40: VdetN=4.0V
c	Output form	N: N-ch open-drain output C: CMOS output
d	Manual reset function	A : Without MR function B : With MR function
e	Package	B: SOT-25 C: SC-82AB(SOT-343), SC-70-5(SOT-353)
f	Product version	A
g	Taping direction	S, N: Refer to PKG file

ELM73 x x x x x A - x
↑ ↑ ↑ ↑ ↑ ↑ ↑
a b c d e f g

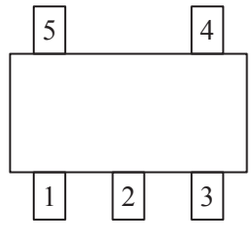
■Pin configuration

SOT-25(TOP VIEW)



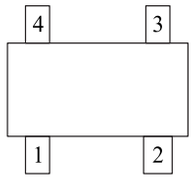
Pin No.	Pin name (73xxxABA)
1	OUT
2	VDD
3	VSS
4	NC
5	ExtC

SOT-25(TOP VIEW)



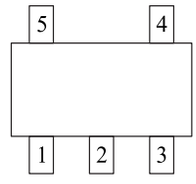
Pin No.	Pin name (73xxxBBA)
1	MR
2	VSS
3	VDD
4	ExtC
5	OUT

SC-82AB(TOP VIEW)



Pin No.	Pin name (73xxxACA)
1	VSS
2	VDD
3	ExtC
4	OUT

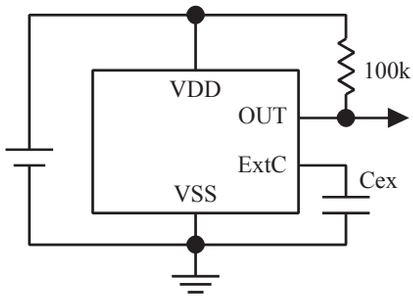
SC-70-5(TOP VIEW)



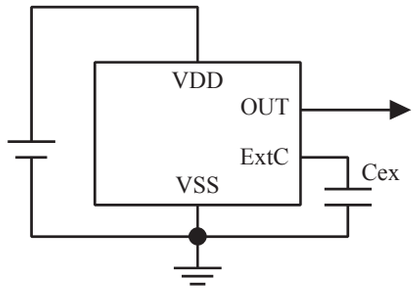
Pin No.	Pin name (73xxxBCA)
1	MR
2	VSS
3	VDD
4	ExtC
5	OUT

■Standard circuit

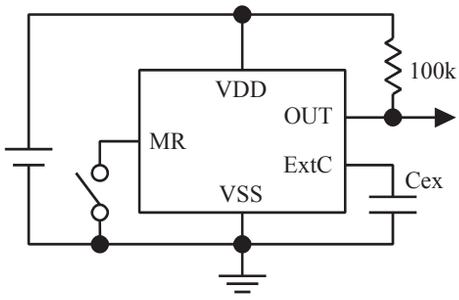
• ELM73xxNAxA



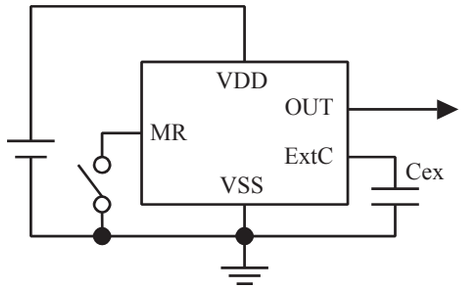
• ELM73xxCAxA



• ELM73xxNBxA



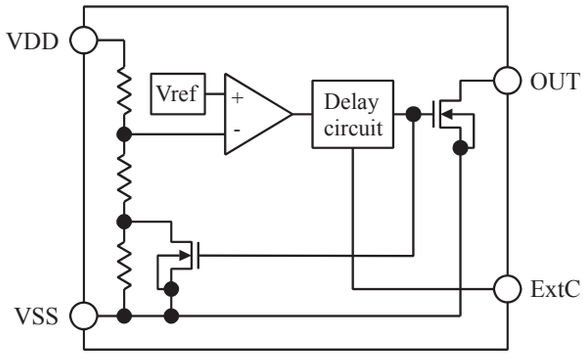
• ELM73xxCBxA



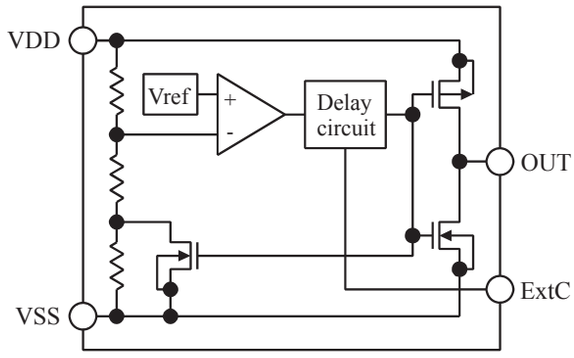
* If delay function is not required, Cex is not necessary.

■Block diagram

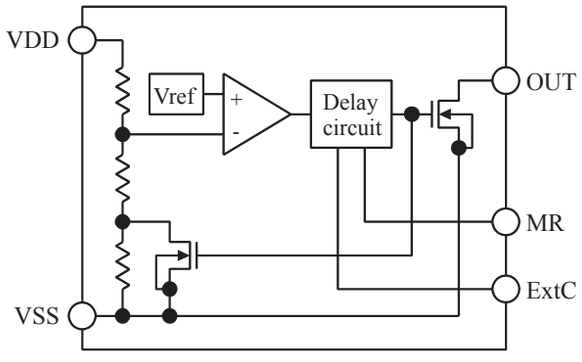
• ELM73xxNAxA



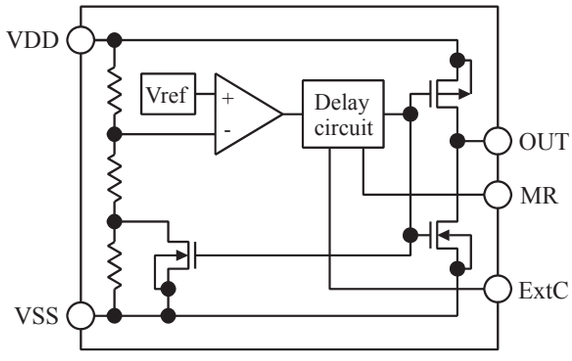
• ELM73xxCAxA



• ELM73xxNBxA

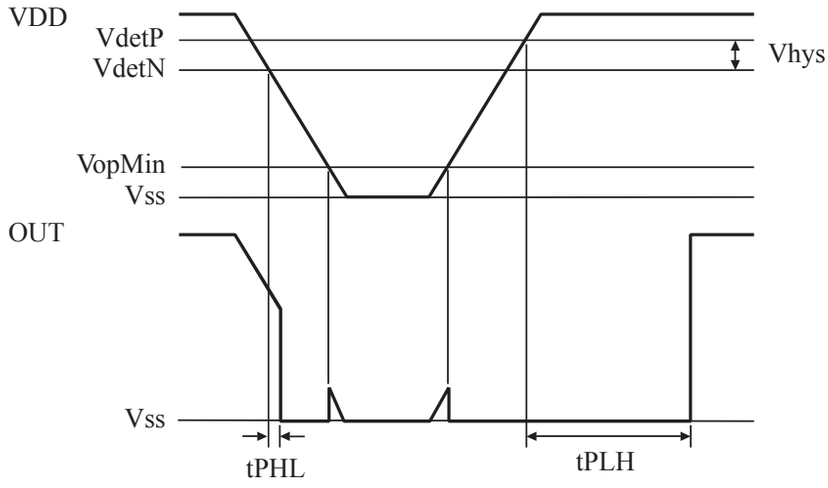


• ELM73xxCBxA

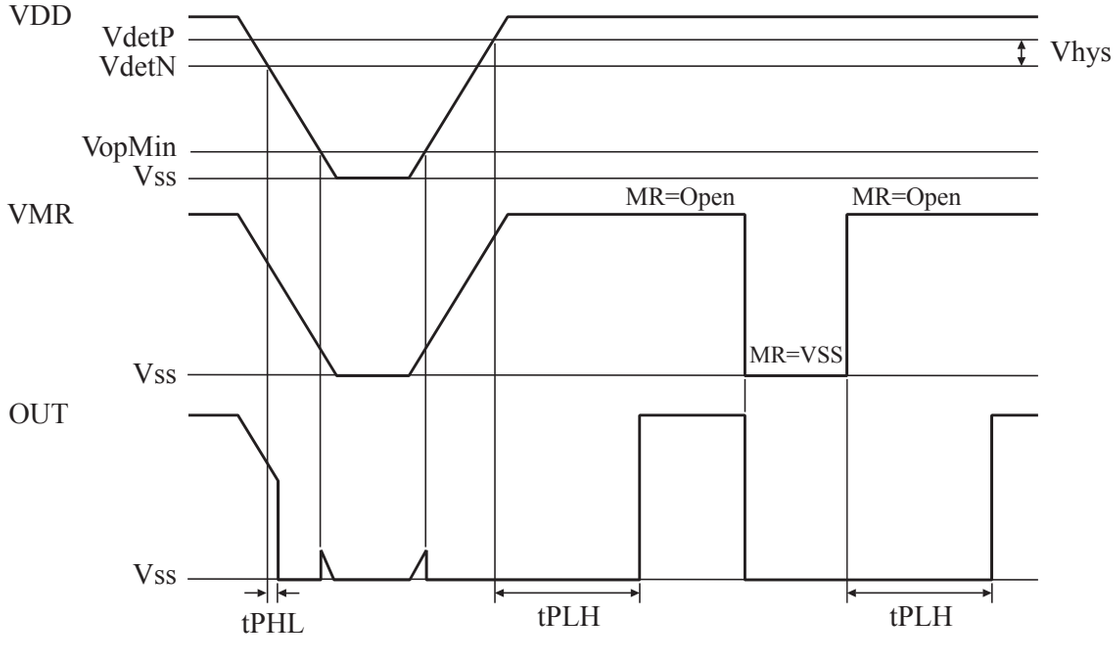


■Timing chart

• ELM73xxxAxA



• ELM73xxxBxA



■Electrical characteristics

ELM7322xxxA Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note*1
Detection voltage	VdetN		2.170	2.200	2.230	V	1
Hysteresis width	Vhys		VdetN× 0.02	VdetN× 0.04	VdetN× 0.08	V	1
Current consumption	Iss	Vdd=3.2V		0.26	0.80	µA	2
Power voltage	Vdd		0.8		6.0	V	1
Output current	IoutN1	Vdd=0.8V, Vds=0.4V	0.01	0.50		mA	3-(1)
	IoutN2	Vdd=1.0V, Vds=0.4V	0.50	2.50			
	IoutP*2	Vdd=3.0V, Vds=0.4V	0.60	1.90		mA	3-(2)
Leakage current	Ileak	Vdd=VLX=6.0V			0.1	µA	4
Delay time	tPLH	Vdd=1.0V to 3.2V, Cex=4.7nF	22.1	26.0*3	29.9	ms	5
	tPHL	Vdd=3.2V to 1.0V		30		µs	
MR voltage High	VmrH	Vdd=6.0V			1.2	V	6
MR voltage Low	VmrL	Vdd=2.7V	0.3				6
MR pull-up resistance	Rmr	Vdd=3.2V	1	3	6	MΩ	7
Temperature characteristic of VdetN	$\frac{\Delta VdetN}{\Delta Top}$			±30		ppm/°C	

∗ 1. Note: test circuit No.,
2. IoutP is only applied to CMOS output products.
3. tPLH(typ.) is derived by using Cex from the following formula: tPLH(typ.)[ms]=5.532×Cex[nF].

ELM7327xxxA Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note*1
Detection voltage	VdetN		2.668	2.700	2.732	V	1
Hysteresis width	Vhys		VdetN× 0.02	VdetN× 0.05	VdetN× 0.08	V	1
Current consumption	Iss	Vdd=3.7V		0.26	0.80	µA	2
Power voltage	Vdd		0.8		6.0	V	1
Output current	IoutN1	Vdd=0.8V, Vds=0.4V	0.01	0.50		mA	3-(1)
	IoutN2	Vdd=1.0V, Vds=0.4V	0.50	2.50			
	IoutP*2	Vdd=4.5V, Vds=0.4V	0.80	2.30		mA	3-(2)
Leakage current	Ileak	Vdd=VLX=6.0V			0.1	µA	4
Delay time	tPLH	Vdd=1.0V to 3.7V, Cex=4.7nF	22.1	26.0*3	29.9	ms	5
	tPHL	Vdd=3.7V to 1.0V		30		µs	
MR voltage High	VmrH	Vdd=6.0V			1.2	V	6
MR voltage Low	VmrL	Vdd=3.2V	0.3				6
MR pull-up resistance	Rmr	Vdd=3.7V	1	3	6	MΩ	7
Temperature characteristic of VdetN	$\frac{\Delta VdetN}{\Delta Top}$			±30		ppm/°C	

∗ 1. Note: test circuit No.,
2. IoutP is only applied to CMOS output products.
3. tPLH(typ.) is derived by using Cex from the following formula: tPLH(typ.)[ms]=5.532×Cex[nF].

ELM7330xxxA Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note*1
Detection voltage	VdetN		2.964	3.000	3.036	V	1
Hysteresis width	Vhys		VdetN× 0.02	VdetN× 0.06	VdetN× 0.08	V	1
Current consumption	Iss	Vdd=4.0V		0.26	0.80	μA	2
Power voltage	Vdd		0.8		6.0	V	1
Output current	IoutN1	Vdd=0.8V, Vds=0.4V	0.01	0.50		mA	3-(1)
	IoutN2	Vdd=1.0V, Vds=0.4V	0.50	2.50			
	IoutP*2	Vdd=4.5V, Vds=0.4V	0.80	2.30		mA	3-(2)
Leakage current	Ileak	Vdd=VLX=6.0V			0.1	μA	4
Delay time	tPLH	Vdd=1.0V to 4.0V, Cex=4.7nF	22.1	26.0*3	29.9	ms	5
	tPHL	Vdd=4.0V to 1.0V		30		μs	
MR voltage High	VmrH	Vdd=6.0V			1.2	V	6
MR voltage Low	VmrL	Vdd=3.5V	0.3				6
MR pull-up resistance	Rmr	Vdd=4.0V	1	3	6	MΩ	7
Temperature characteristic of VdetN	$\frac{\Delta VdetN}{\Delta Top}$			±30		ppm/°C	

∗ 1. Note: test circuit No.,
2. IoutP is only applied to CMOS output products.
3. tPLH(typ.) is derived by using Cex from the following formula: tPLH(typ.)[ms]=5.532×Cex[nF].

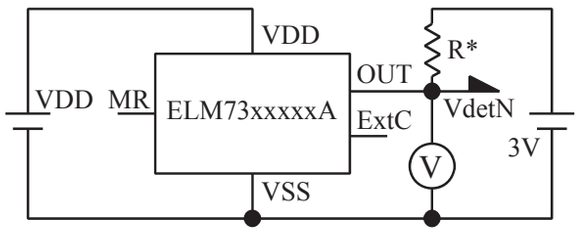
ELM7340xxxA Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note*1
Detection voltage	VdetN		3.952	4.000	4.048	V	1
Hysteresis width	Vhys		VdetN× 0.02	VdetN× 0.06	VdetN× 0.08	V	1
Current consumption	Iss	Vdd=5.0V		0.26	0.80	μA	2
Power voltage	Vdd		0.8		6.0	V	1
Output current	IoutN1	Vdd=0.8V, Vds=0.4V	0.01	0.50		mA	3-(1)
	IoutN2	Vdd=1.0V, Vds=0.4V	0.50	2.50			
	IoutP*2	Vdd=4.5V, Vds=0.4V	0.80	2.30		mA	3-(2)
Leakage current	Ileak	Vdd=VLX=6.0V			0.1	μA	4
Delay time	tPLH	Vdd=1.0V to 5.0V, Cex=4.7nF	22.1	26.0*3	29.9	ms	5
	tPHL	Vdd=5.0V to 1.0V		30		μs	
MR voltage High	VmrH	Vdd=6.0V			1.2	V	6
MR voltage Low	VmrL	Vdd=4.5V	0.3				6
MR pull-up resistance	Rmr	Vdd=5.0V	1	3	6	MΩ	7
Temperature characteristic of VdetN	$\frac{\Delta VdetN}{\Delta Top}$			±30		ppm/°C	

∗ 1. Note: test circuit No.,
2. IoutP is only applied to CMOS output products.
3. tPLH(typ.) is derived by using Cex from the following formula: tPLH(typ.)[ms]=5.532×Cex[nF].

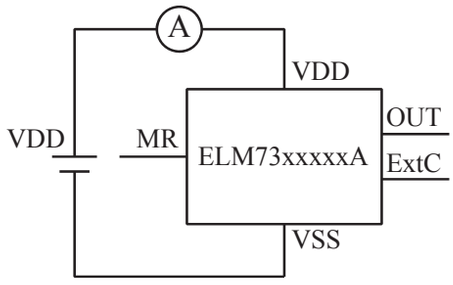
■Test circuits

1) Detection voltage

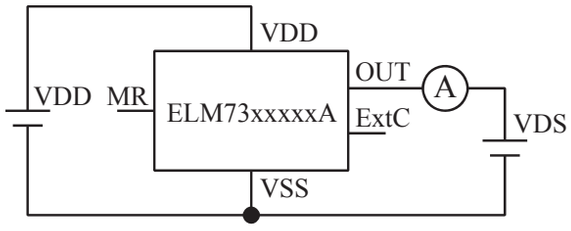


* Pull up circuit is necessary for N-ch output only.
R=100kΩ(R=1MΩ for Vdd min measurement.

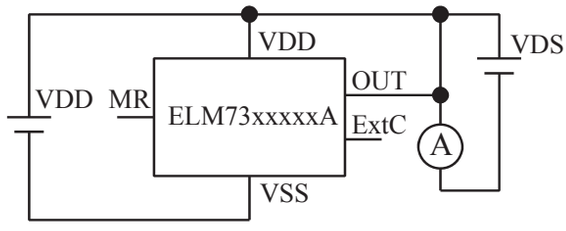
2) Current consumption



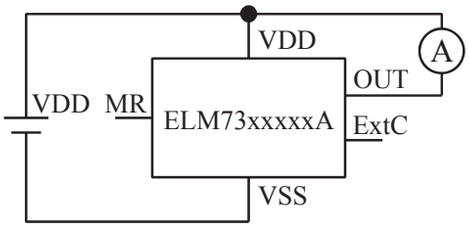
3)-(1) Output current (N-ch)



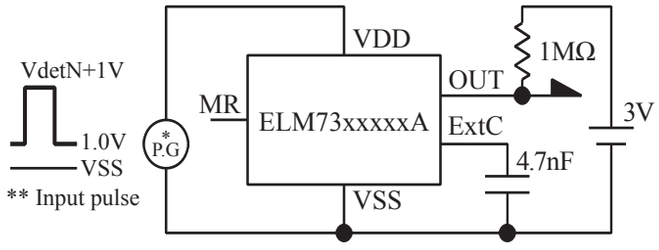
3)-(2) Output current (P-ch)



4) Leakage current

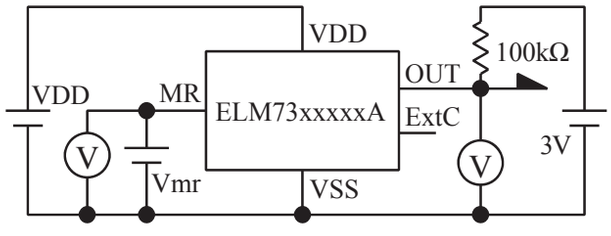


5) Delay time



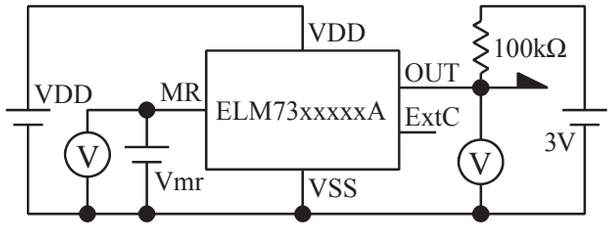
* Pull up circuit is necessary for N-ch output only.

6) MR voltage



* Pull up circuit is necessary for N-ch output only.

7) MR pull-up resistance

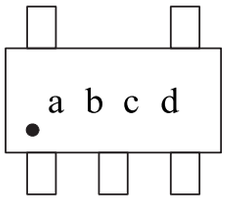


* Pull up circuit is necessary for N-ch output only.

■Marking

- SOT-25 package

SOT-25



a, b : Represents “Output type” , “Manual Reset function” and “Detection voltage range”.

Symbol	Output type	Manual reset function	Vdet range(V)
78	CMOS	Without MR function	1.4 to 3.0
79			3.1 to 5.0
7A		With MR function	1.4 to 3.0
7B			3.1 to 5.0
7C	Nch	Without MR function	1.4 to 3.0
7D			3.1 to 5.0
7E		With MR function	1.4 to 3.0
7F			3.1 to 5.0

c : Represents “Detection voltage”.

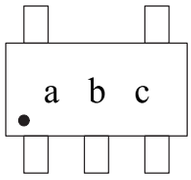
Symbol	Detection voltage(V)		Symbol	Detection voltage(V)	
1		3.1	F	1.6	4.6
2		3.2	G	1.7	4.7
3		3.3	H	1.8	4.8
4		3.4	J	1.9	4.9
5		3.5	K	2.0	5.0
6		3.6	L	2.1	
7		3.7	M	2.2	
8		3.8	N	2.3	
9		3.9	P	2.4	
0		4.0	Q	2.5	
A		4.1	R	2.6	
B		4.2	S	2.7	
C		4.3	T	2.8	
D	1.4	4.4	U	2.9	
E	1.5	4.5	V	3.0	

d : Represents “Assembly lot number”.

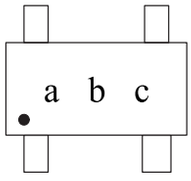
Symbol
1 to 0 and A to Z repeated (I, O, X excepted)

- SC-70-5, SC-82AB package

SC-70-5



SC-82AB



a : Represents “Output type” and “Detection voltage range”.

Symbol	Output type	Vdet range(V)
H	CMOS	1.4 to 3.0
J		3.1 to 5.0
K	Nch	1.4 to 3.0
L		3.1 to 5.0

b : Represents “Detection voltage”.

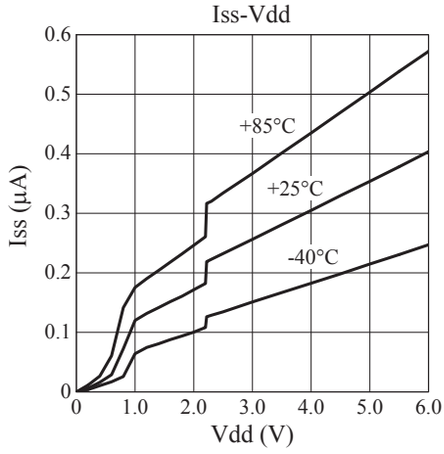
Symbol	Detection voltage(V)		Symbol	Detection voltage(V)	
1		3.1	F	1.6	4.6
2		3.2	G	1.7	4.7
3		3.3	H	1.8	4.8
4		3.4	J	1.9	4.9
5		3.5	K	2.0	5.0
6		3.6	L	2.1	
7		3.7	M	2.2	
8		3.8	N	2.3	
9		3.9	P	2.4	
0		4.0	Q	2.5	
A		4.1	R	2.6	
B		4.2	S	2.7	
C		4.3	T	2.8	
D	1.4	4.4	U	2.9	
E	1.5	4.5	V	3.0	

c : Represents “Assembly lot number”.

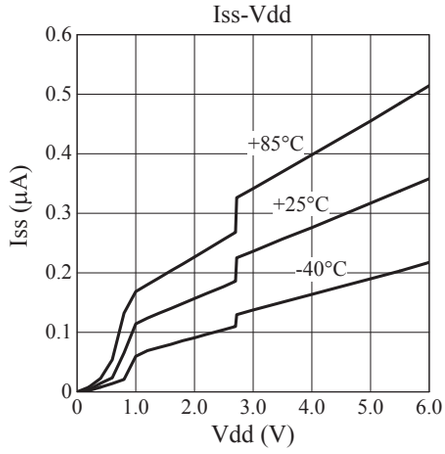
Symbol
1 to 0 and A to Z repeated (I, O, X excepted)

■Current consumption characteristics

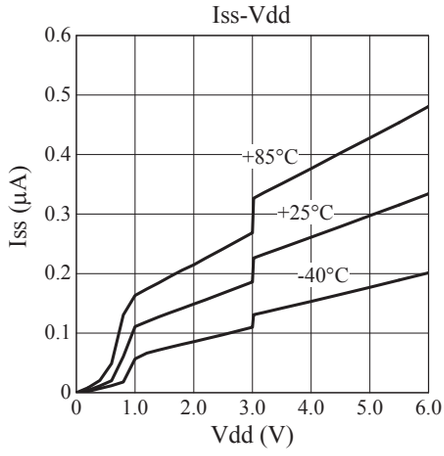
• VdetN=2.2V (ELM7322xxxA)



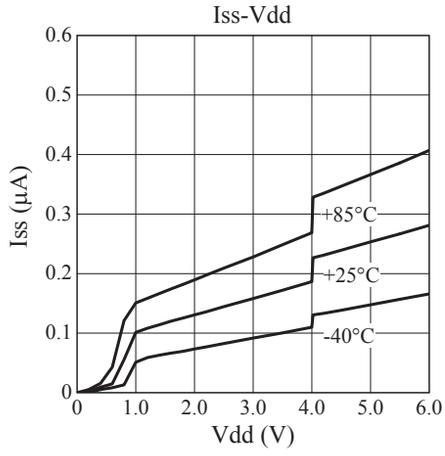
• VdetN=2.7V (ELM7327xxxA)



• VdetN=3.0V (ELM7330xxxA)

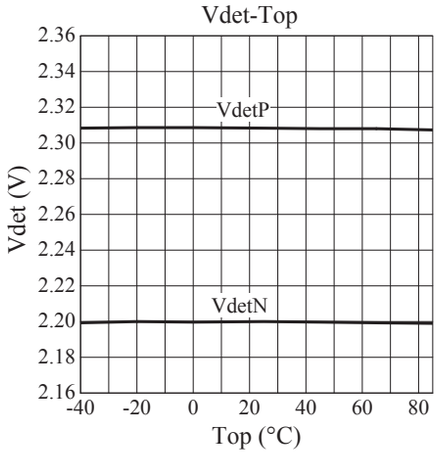


• VdetN=4.0V (ELM7340xxxA)

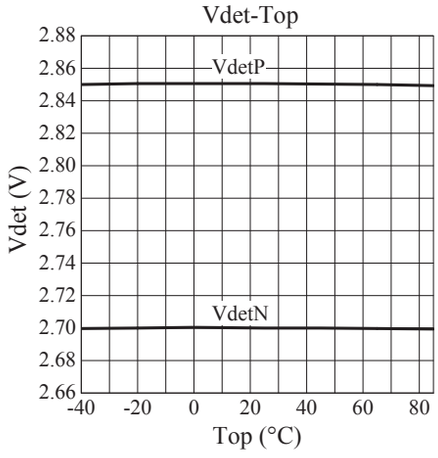


■Detection voltage characteristics

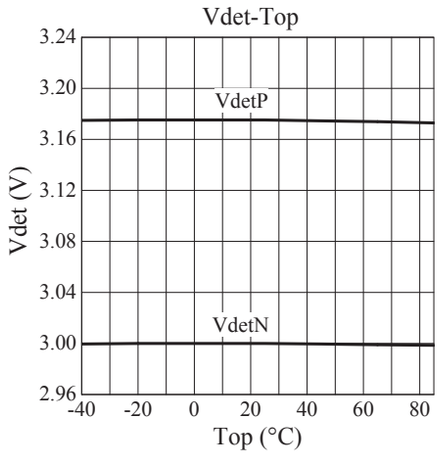
• VdetN=2.2V (ELM7322xxxA)



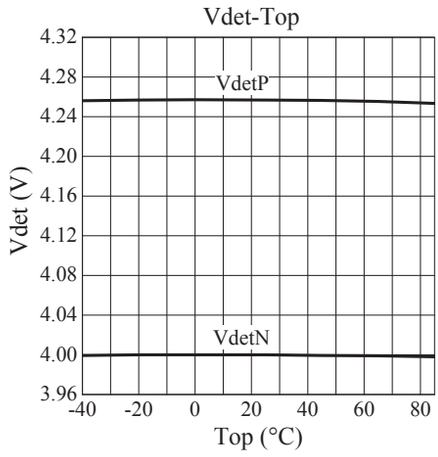
• VdetN=2.7V (ELM7327xxxA)



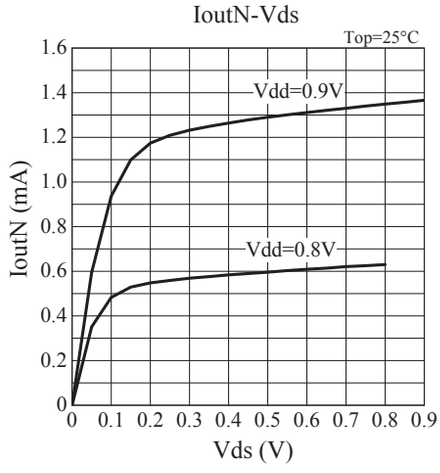
• VdetN=3.0V (ELM7330xxxA)

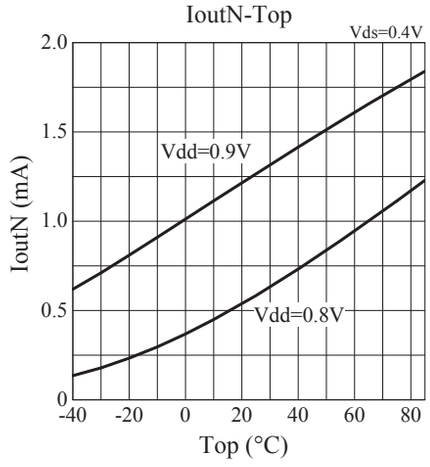


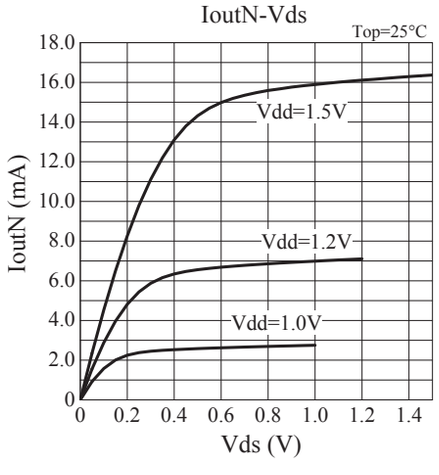
• VdetN=4.0V (ELM7340xxxA)

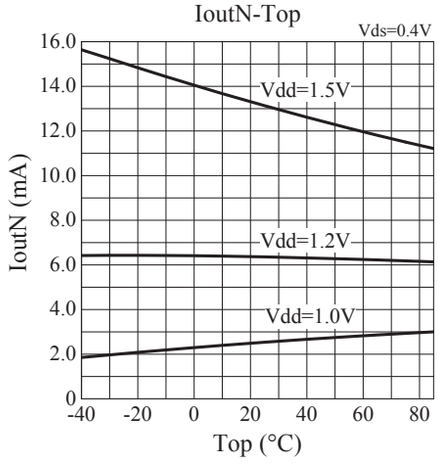


■N-ch output current characteristics

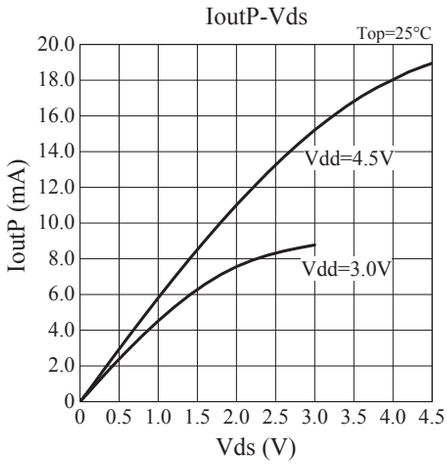


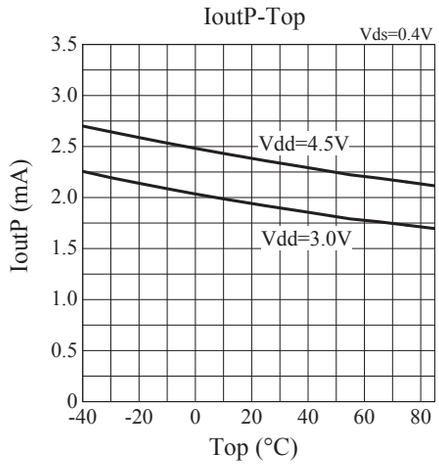






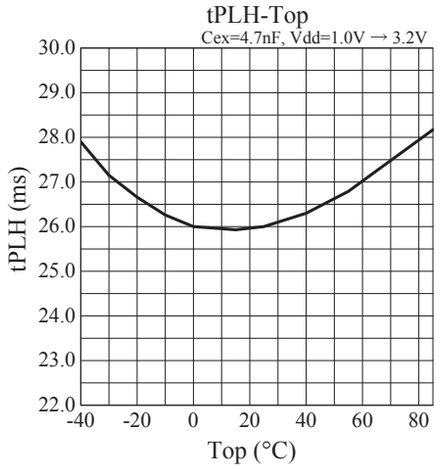
■P-ch output current characteristics (ELM73xxCxxA)

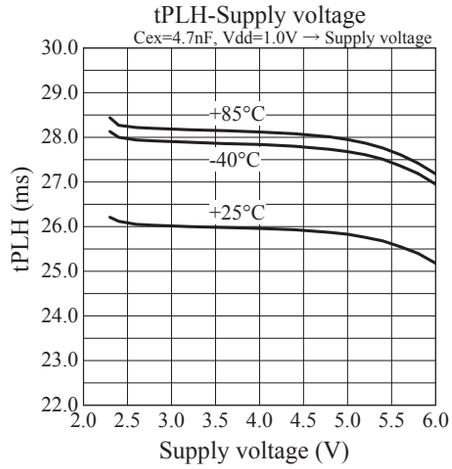


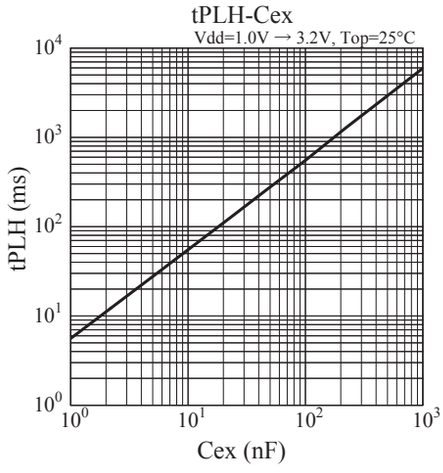


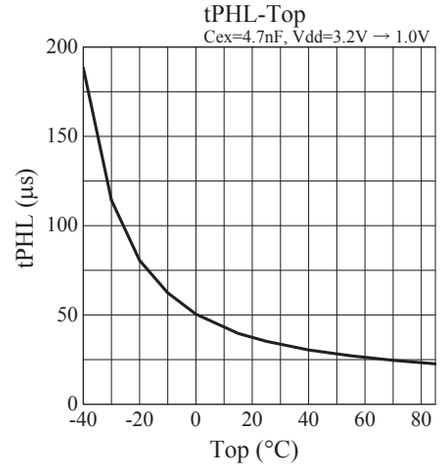
■Delay time characteristics

- VdetN=2.2V (ELM7322xxxA)

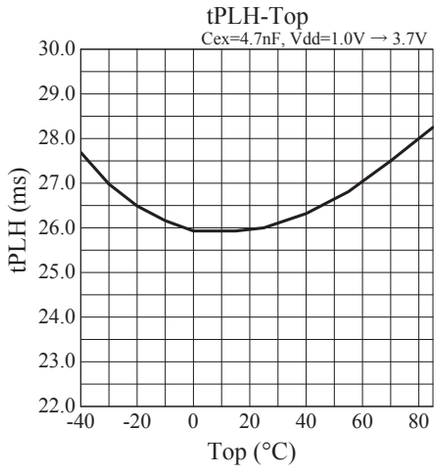


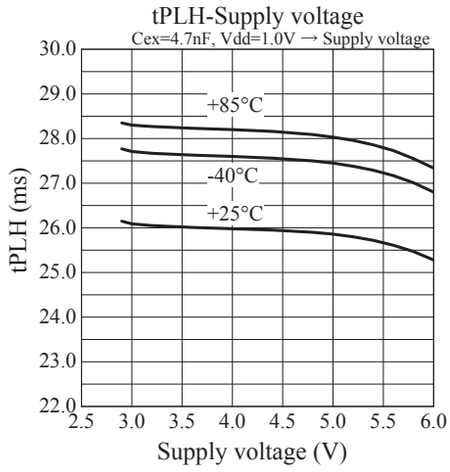


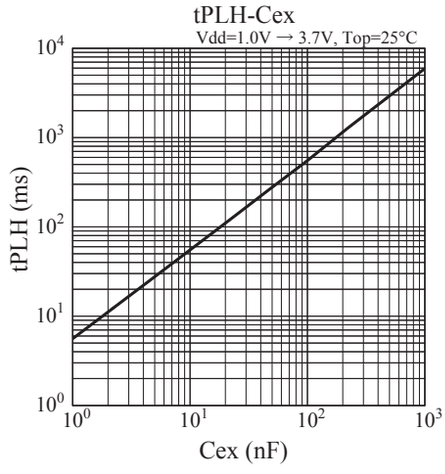


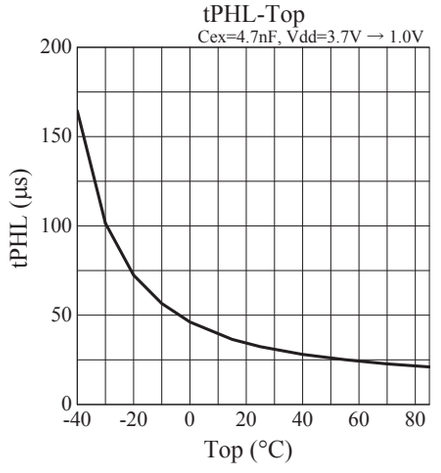


• VdetN=2.7V (ELM7327xxxA)

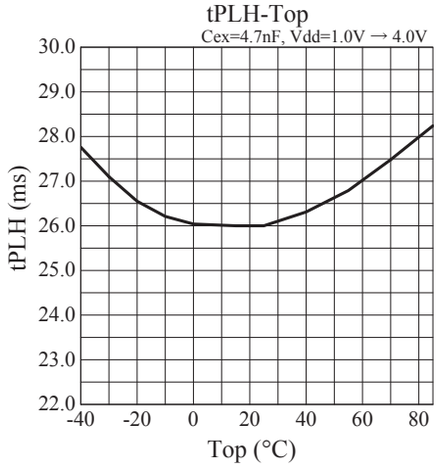


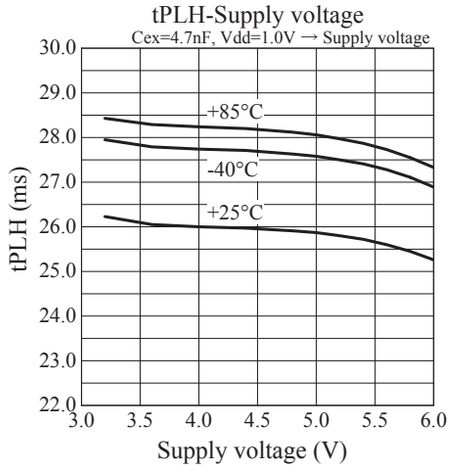


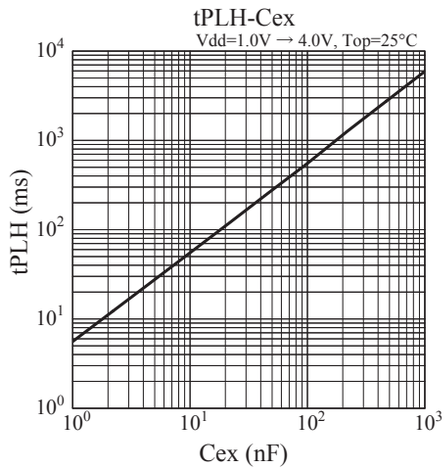


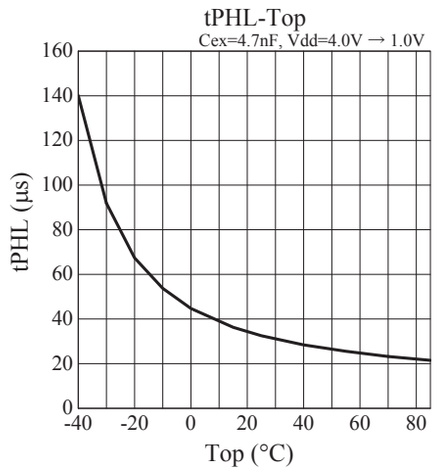


• VdetN=3.0V (ELM7330xxxA)

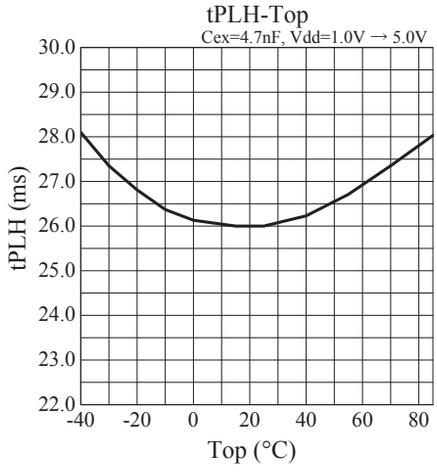


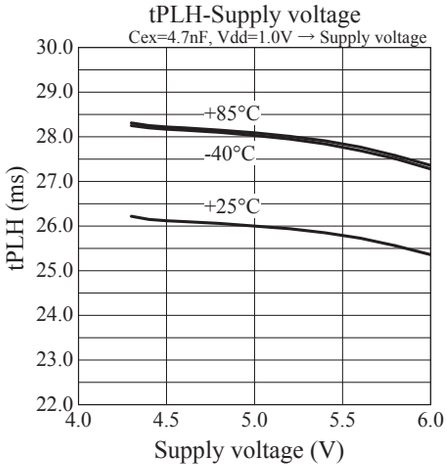


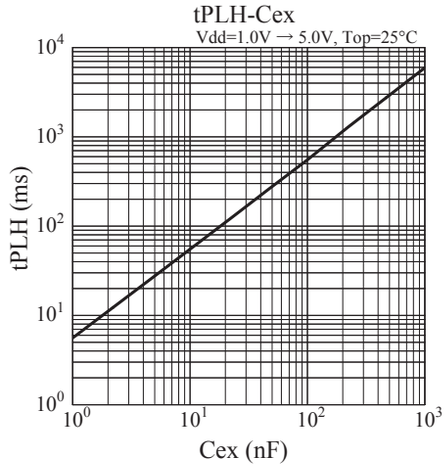


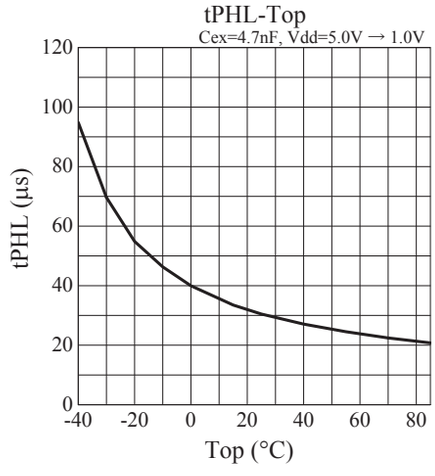


• VdetN=4.0V (ELM7340xxxA)

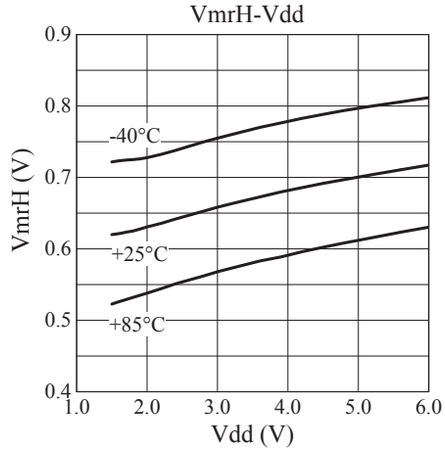


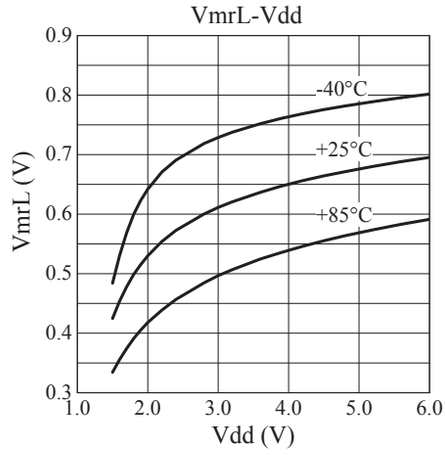


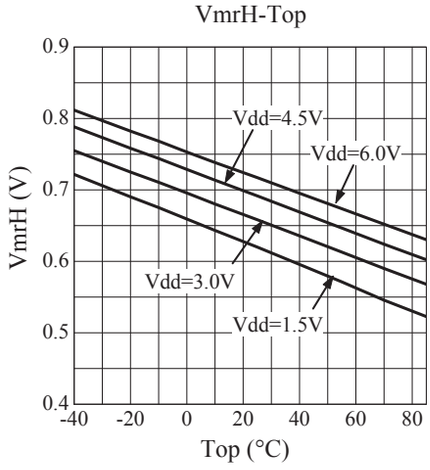


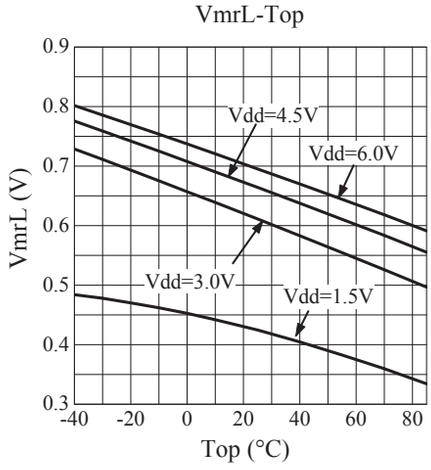


■MR voltage characteristics (ELM73xxxBxA)

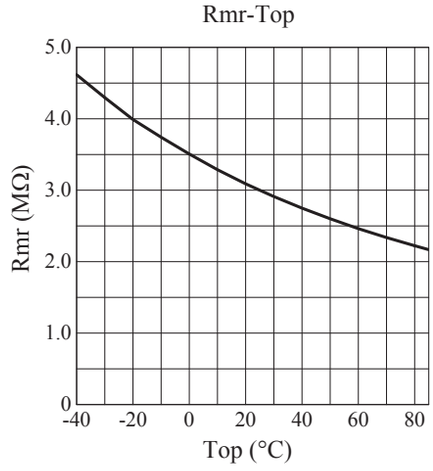








■MR pull-up resistance characteristics (ELM73xxxBxA)



■N-ch output leakage current characteristics (ELM73xxNxxA)