Ver.:1.0

TFT LCD Specification

Model Name: 990001265 (EJ030NA-01B)

Customer Signature
Date

This technical specification is subjected to change without notice

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Record of Revision

Rev	Issue Date	Description
0.1	2011/05/16	New created
0.2	2011/06/03	Update Packing Drawing
0.3	2011/06/09	Updated the EE/ME/DQA design concept after DR confirm
0.4	2011/06/29	Update EE power consumption and Application circuit
0.5	2011/08/01	Update EE SPI timing
1.0	2011/12/05	Final version

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1. FEATURES

The 3.0” LCD module is the active matrix color TFT LCD module applied by a-si TFT(Amorphous silicon TFT) technology. The product is designed for the requirement of the green product, and the specification complies with CMI’s “Green Product Chemical Substance Specification Standard Hand Book”.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	3.0	Inch
Display Type	Transmissive	-
Active Area (HxV)	60.03125 X 45	mm
Number of Dots (HxV)	960 x 480	dot
Dot Pitch (HxV)	62.5 x 93.75	um
Color Arrangement	RGB Delta	-
Outline Dimension (HxVxT) *	70.6 X 51.7 X 2.05	mm
Weight	15.95	g
Panel surface treatment	HC	-

*Exclude FPC and protrusions.

*With WV film

*HC: Hard Coating (3H)

*Gray Scale Inversion (6 o’clock): Outer Lead Bonding at right side

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3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD Panel

Recommend connector:

Compatible with Molex 5025985191

Pin	Symbol	I/O	Description	Remark
1	GND	P	Ground supply for internal circuit	
2	GRB	I	Global reset pin	
3	CS	I	Serial communication chip select	
4	SDIN	I	Serial communication data input	
5	SCLK	I	Serial communication clock input	
6	VDDIO	P	Power supply for digital interface	
7	VDD_18V	C	Power setting capacitor connect pin	
8	DCLK	I	Clock signal, latching data at the rising edge	
9	VS	I	Vertical sync input, negative polarity	
10	HS	I	Horizontal sync input, negative polarity	
11	DY7	I	Data input	
12	DY6	I	Data input	
13	DY5	I	Data input	
14	DY4	I	Data input	
15	DY3	I	Data input	
16	DY2	I	Data input	
17	DY1	I	Data input	
18	DY0	I	Data input	
19	DC7	I	Data input	
20	DC6	I	Data input	
21	DC5	I	Data input	
22	DC4	I	Data input	
23	DC3	I	Data input	
24	DC2	I	Data input	
25	DC1	I	Data input	
26	DC0	I	Data input	
27	VCOMH	C	Power setting capacitor for VCOMH	
28	VCOMH	C	Power setting capacitor for VCOMH	
29	VCOML	C	Power setting capacitor for VCOML	
30	VCOML	C	Power setting capacitor for VCOML	
31	VDD	P	Power supply for internal circuit	

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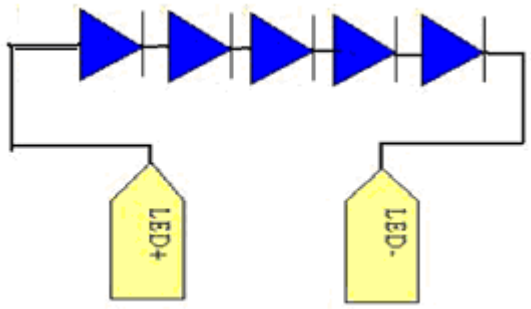
32	VDD	P	Power supply for internal circuit	
33	GND	P	Ground supply for internal circuit	
34	VINT2	C	Power setting capacitor connect pin	
35	V9	C	Power setting capacitor connect pin	
36	V10	C	Power setting capacitor connect pin	
37	VINT1	C	Power setting capacitor connect pin	
38	VINT1	C	Power setting capacitor connect pin	
39	AGND	P	Ground supply for charge pump circuit	
40	V1	C	Power setting capacitor connect pin	
41	V2	C	Power setting capacitor connect pin	
42	V3	C	Power setting capacitor connect pin	
43	V4	C	Power setting capacitor connect pin	
44	V5	C	Power setting capacitor connect pin	
45	V6	C	Power setting capacitor connect pin	
46	VGH	C	Power setting capacitor connect pin	
47	V7	C	Power setting capacitor connect pin	
48	V8	C	Power setting capacitor connect pin	
49	VGL	C	Power setting capacitor connect pin	
50	LED+	P	LED power anode	**Note 2**
51	LED-	P	LED power cathode	**Note 2**

Note 1: I : Input, O : Output, C : Capacitor Pin, P : Power(in)

Note 2: The figure below shows the connection of backlight LED.



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4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Power supply (pump)	VDD	-0.3	+4.0	V
Power supply for IO	VDDIO	-0.3	VDD+0.3	V
Storage temperature	T_{STG}	-30	80	℃
Operating temperature	T_{OPR}	0	60	℃

5. ELECTRICAL CHARACTERISTICS

Driving TFT LCD Panel

GND=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		VDD	3.00	3.30	3.60	V	
Power Supply for IO		VDDIO	1.65	1.8	VDD	V	
Input Signal Voltage	Low Level	V_{IL}	GND	-	0.3x VDDIO	V	VSYNC, HSYNC, DCLK, DG[0:7], DB[0:7], SDIN, SCLK, CS, GRB, Note5-1
	High Level	V_{IH}	0.7x VDDIO	-	VDDIO	V	
Panel Power Consumption		W_P	-	60	-	mW	
Panel Power Consumption (Standby mode)		I_{ST}			35	uA	DCLK stop, Data keep low

Note5-1: Overshoot swing: Low level: -0.3V ~ High level: VDDIO+0.3V

Driving Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	--	25	27	mA	Note 5-2
Forward Current Voltage	V_F	--	16	17.5	V	
Backlight Power Consumption	W_{BL}	--	400	472.5	mW	

Note 5-2: Backlight driving circuit is recommended as the fix current circuit.

* Ta: Ambient Temperature

* High temperature operation: Test current refers the diagram as following

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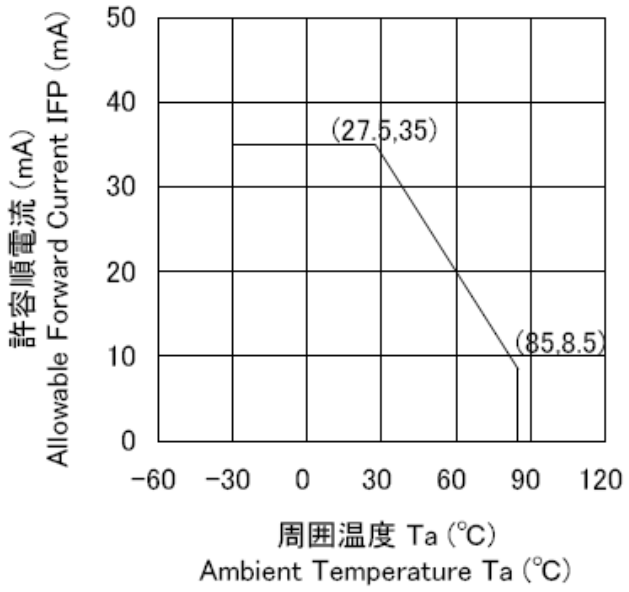

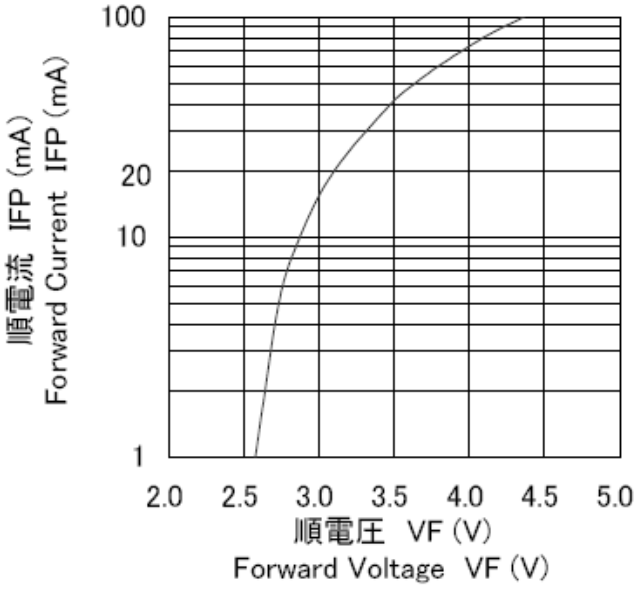

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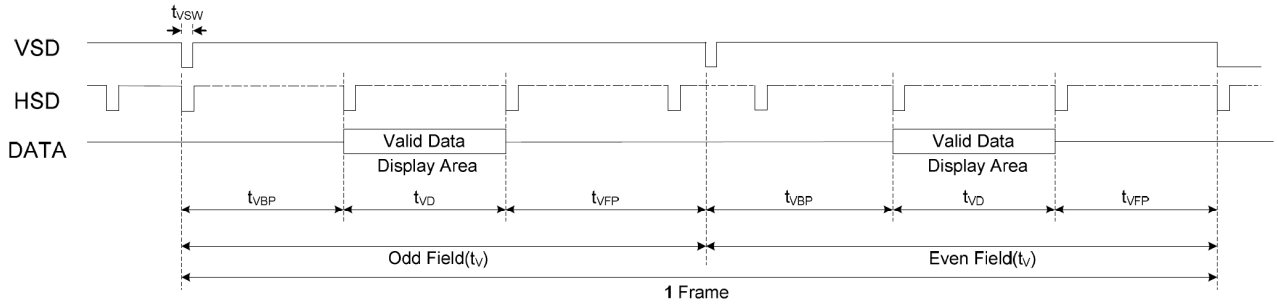
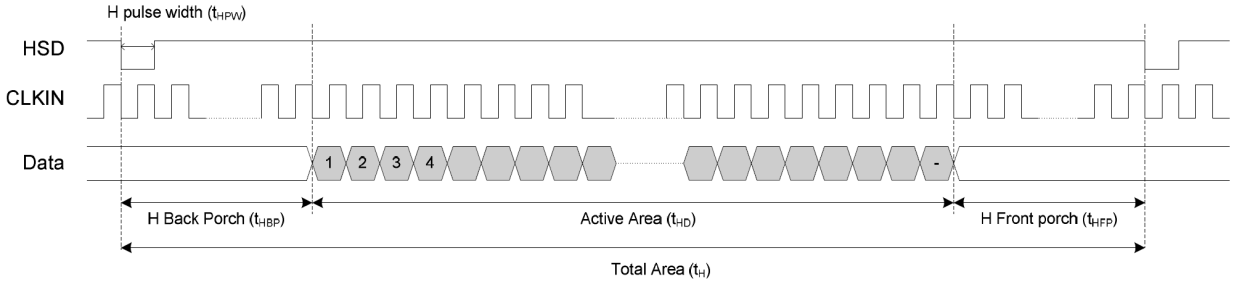
6. TIMING CHART

6.1 YUV720 16-bit Parallel input timing





NTSC

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK frequency			f_{DCLK}	18.6	27	29.7	MHz	
Hsync	Period		t_H	764	858	1920	DCLK	
	Display period		t_{HD}		720		DCLK	
	Back porch		t_{HBP}	10	40	255	DCLK	
	Front porch		t_{HFP}	-	98	-	DCLK	
	Pulse Width		t_{HPW}	1	20	t_{HBP} -1	DCLK	
Vsync	Period		t_V	485.5	524.5	575.5	HS	
	Display period		t_{VD}		480		HS	
	Back porch	Odd field	t_{VBP}	3	27	31	HS	
		Even field		3.5	27.5	31.5		
	Front porch	Odd field	t_{VFP}	-	17.5	-	HS	
		Even field		-	17	-		
	Pulse Width		t_{VSW}	-	1	-	DCLK	
	1 Frame		-	-	1049	-	HS	

PAL

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK frequency			f_{DCLK}	17.8	26.8	29.5	MHz	
Hsync	Period		t_H	764	858	1920	DCLK	
	Display period		t_{HD}		720		DCLK	
	Back porch		t_{HBP}	10	40	255	DCLK	
	Front porch		t_{HFP}	-	98	-	DCLK	
	Pulse Width		t_{HPW}	1	20	t_{HBP} -1	DCLK	
Vsync	Period		t_V	581.5	624.5	680.5	HS	
	Display period		t_{VD}		576		HS	
	Back porch	Odd field	t_{VBP}	3	30	34	HS	
		Even field		3.5	30.5	34.5		
	Front porch	Odd field	t_{VFP}	-	18.5	-	HS	
		Even field		-	18	-		
	Pulse Width		t_{VSW}	-	1	-	DCLK	
	1 Frame		-	-	1249	-	HS	

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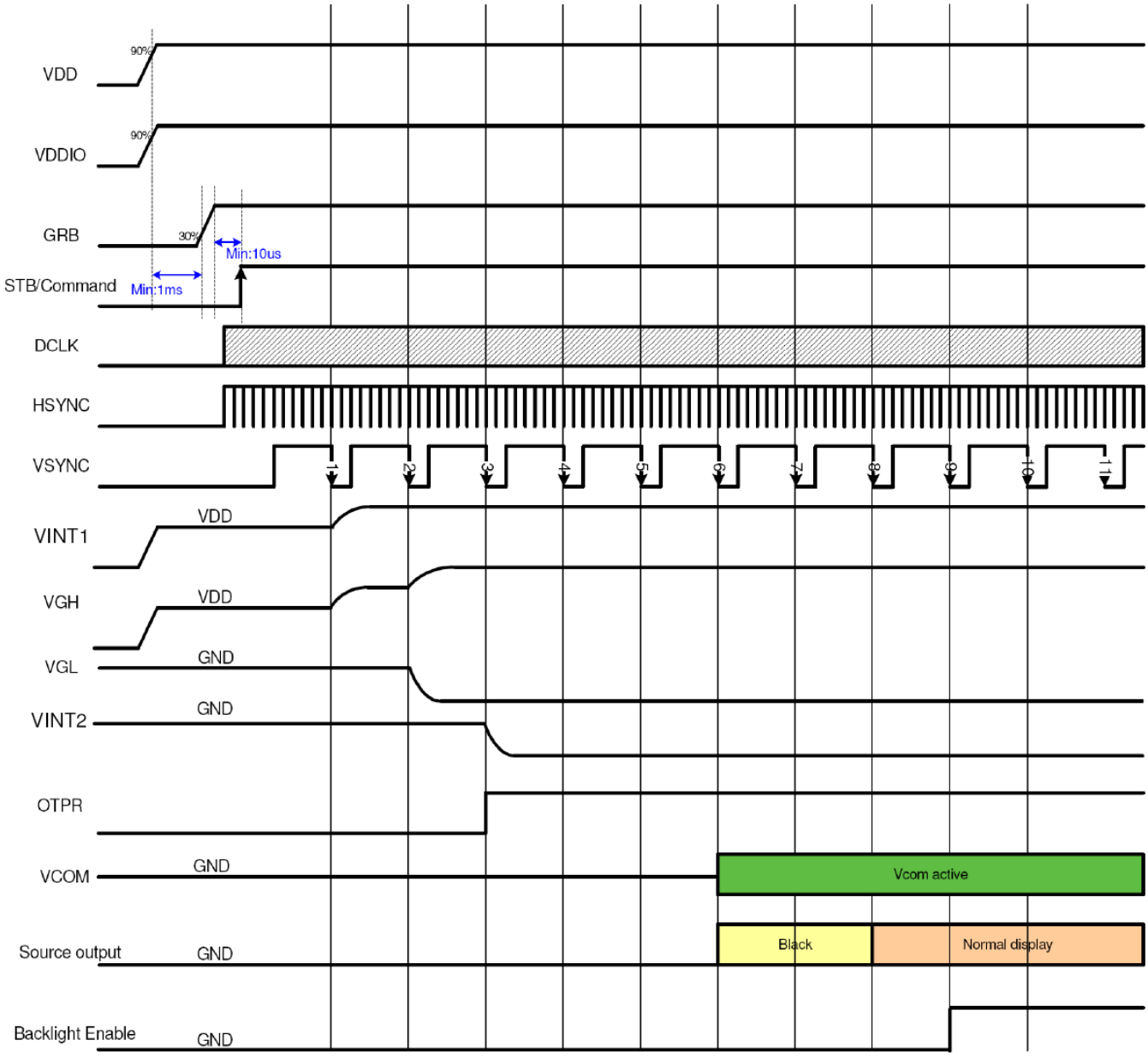
7. POWER SEQUENCE

7.1 Power On Sequence



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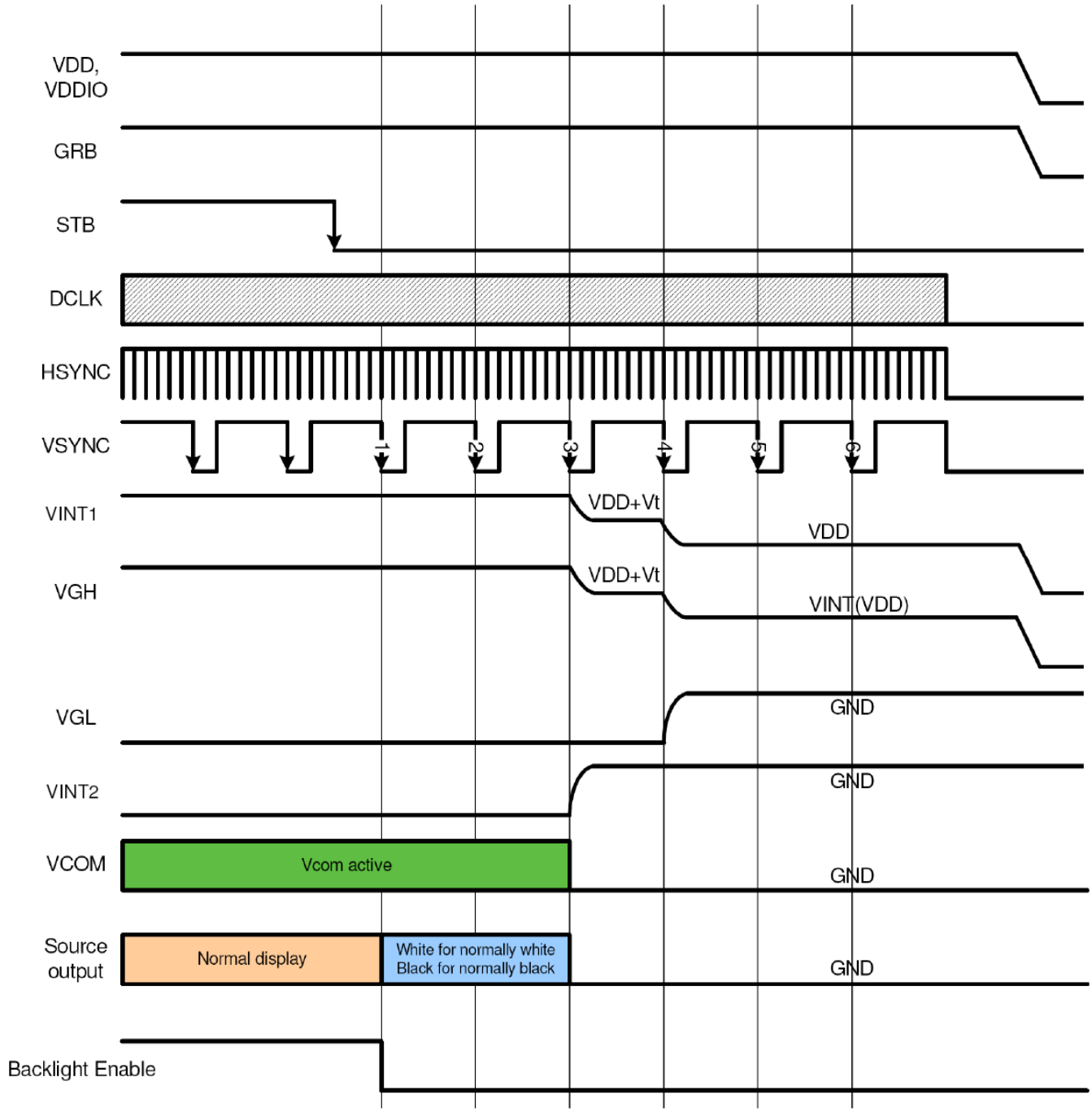
7.2 Power off Sequence



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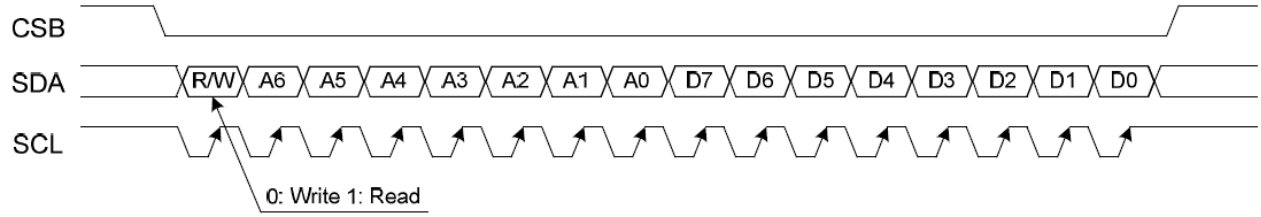
8. SERIAL INTERFACE

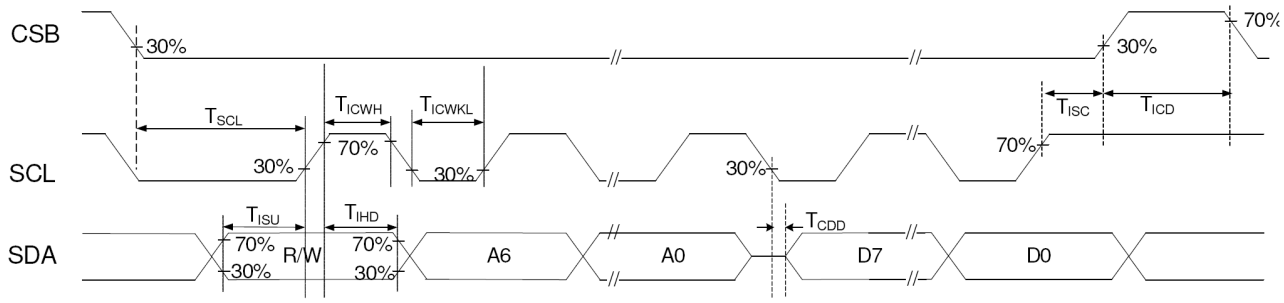
8.1 SPI command format



Note:

- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SCL. Command loading operation starts from the falling edge of CSB and is completed at the next rising edge of CSB.
- The serial control block is operational after power on reset, but commands are established by the VS signal. If command is transferred multiple times for the same register, the last command before the VS signal is valid.
- If less than 16 bits of SCL are input while CSB is low, the transferred data is ignored.
- If longer than 16 bits of SCL are input while CSB is low, the transferred data is ignored.
- Serial commands can be accepted in the stand-by mode.

8.2 SPI timing



(VDD=3.0~3.6V, VDD=VDDIO, GND=AGND= 0V, T_{OPR} = -10℃ to 60℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Write timing						
CSB falling to SCL rising time	T_{SCL}	200	-	-	ns	
SCL pulse high period	T_{ICWH}	100	-	-	ns	
SCL pulse low period	T_{ICWL}	100	-	-	ns	
SDA data input setup time	T_{ISU}	100	-	-	ns	
SDA data input hold time	T_{IHD}	100	-	-	ns	
SCL rising to CSB rising time	T_{ISC}	100	-	-	ns	
CSB rising to falling time	T_{ICD}	400	-	-	ns	

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Read timing						
CSB falling to SCL rising time	T_{SCL}	200	-	-	ns	
SCL pulse high period	T_{ICWH}	500	-	-	ns	
SCL pulse low period	T_{ICWL}	500	-	-	ns	
SDA data input setup time	T_{ISU}	100	-	-	ns	
SDA data input hold time	T_{IHD}	100	-	-	ns	
SCL rising to CSB rising time	T_{ISC}	100	-	-	ns	
SCL falling to SDA output delay time	T_{CDD}	-	-	100	ns	SDA at output mode
CSB rising to falling time	T_{ICD}	400	-	-	ns	

8.3 Input timing

(VDD=3.0~3.6V, VDD=VDDIO, GND=AGND= 0V, T_{OPR} = -10℃ to 60℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
VDD slew rate	T_{POR}	0.1	-	30	ms	From 0V to 90%VDD
GRB active pulse width	T_{GRB}	1	-	-	ms	VDDIO=3.3V
VDD resettle time	T_{RES}	1	-	-	s	
DCLK clock pulse width	T_{DCLK}	-	37	-	ns	16-bit 720 YUV mode
DCLK clock pulse high	T_{CWH}	7	-	-	ns	
DCLK clock pulse low	T_{CWL}	7	-	-	ns	
VS setup time	T_{VSU}	6	-	-	ns	
VS hold time	T_{VHU}	6	-	-	ns	
HS setup time	T_{HSU}	6	-	-	ns	
HS hold time	T_{HHD}	6	-	-	ns	
Data setup time	T_{DSU}	6	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to DCLK
Data hold time	T_{DHD}	6	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to DCLK

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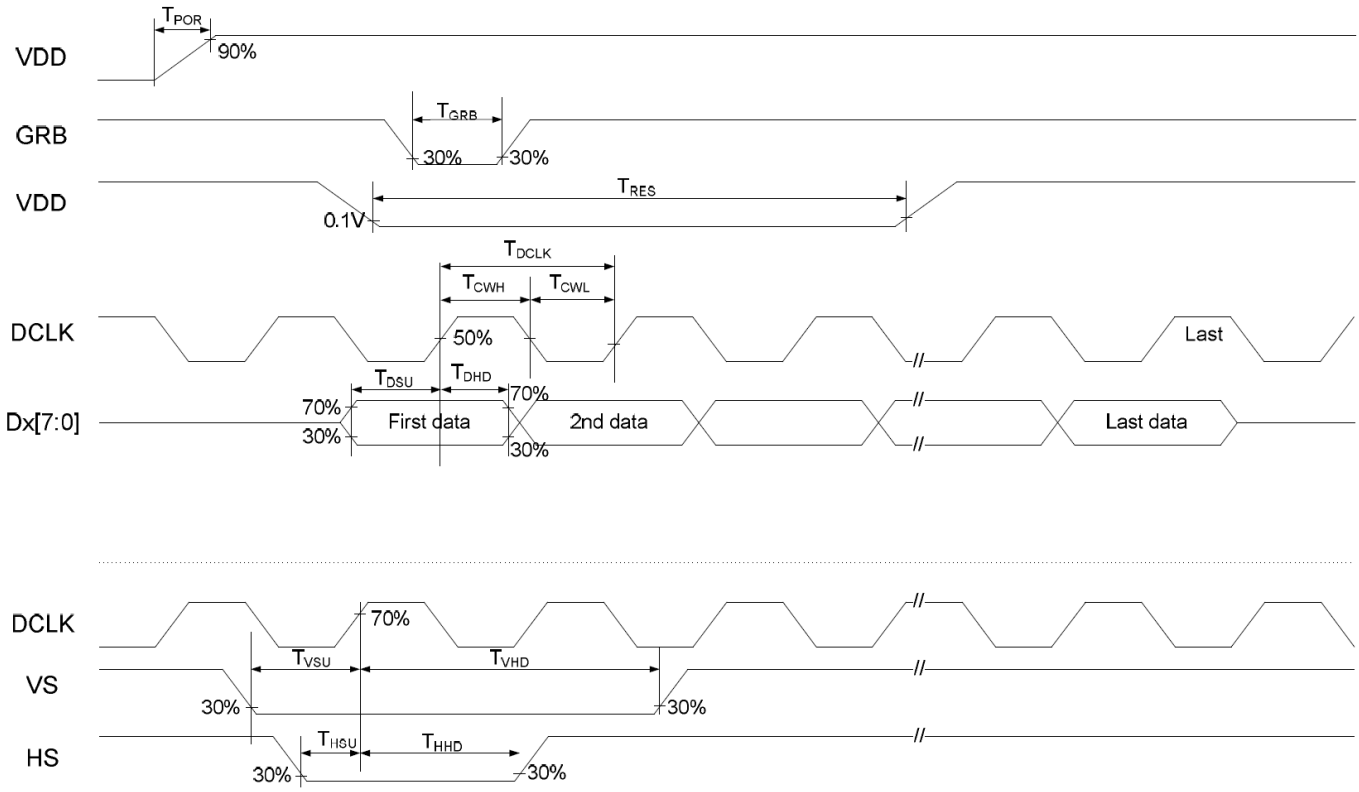
Timing Waveform



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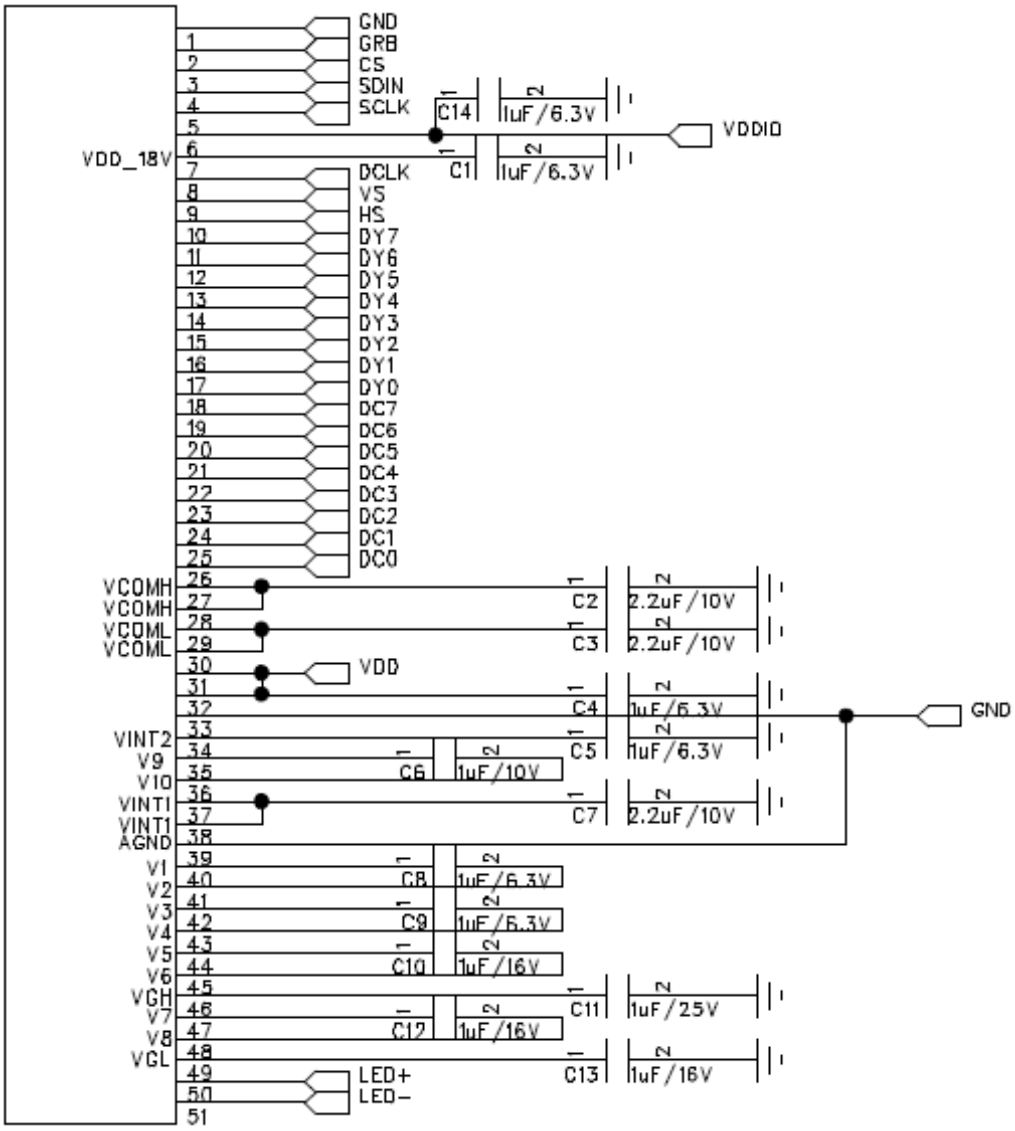
9. Application circuit



Pin Name	Capacitor	Pin Name	Capacitor
V1	1uF / 6.3V / 10% / X5R	VDD_18V	1uF / 6.3V / 10% / X5R
V2		VCOMH	2.2uF / 10V / 10% / X5R
V3	1uF / 6.3V / 10% / X5R	VCOML	2.2uF / 10V / 10% / X5R
V4		VDD	1uF / 6.3V / 10% / X5R
V5	1uF / 16V / 10% / X5R	VINT2	1uF / 6.3V / 10% / X5R
V6		VINT1	2.2uF / 10V / 10% / X5R
V7	1uF / 16V / 10% / X5R	VGH	1uF / 25V / 10% / X5R
V8		VGL	1uF / 16V / 10% / X5R
V9	1uF / 10V / 10% / X5R	VDDIO	1uF / 6.3V / 10% / X5R
V10			

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10. Initial code setting

Name	Address	Setting	Note
RSTB	0x05	0x1E	In refresh mode, don't set .
PFM_EN	0x05	0x5C	
NARROW/Contrast_SEL	0x02	0x14	Default
Brightness	0x03	0x40	Default
IF_SEL	0x04	0x6B	Default
HBLK_EN/VBP	0x06	0x1B	Default
HBP	0x07	0x28	Default
CbCr/VSP/HSP/DCLKP	0x0C	0x06	Default
Contrast_8bit	0x0D	0x40	Default
SUB Contrast_R	0x0E	0x40	Default
SUB Brightness_R	0x0F	0x40	Default
SUB Contrast_B	0x10	0x40	Default
SUB Brightness_B	0x11	0x40	Default
VGL	0x2F	0x40	Default
VGH	0x5A	0x02	Default
Positive Gamma	0x30	0x07	
	0x31	0x57	
	0x32	0x53	
	0x33	0x77	
	0x34	0XB8	
	0x35	0xBD	
	0x36	0XB8	
	0x37	0XE7	
	0x38	0x04	
	0x39	0xFF	
Negative Gamma	0x40	0x0B	
	0x41	0xB8	
	0x42	0xAB	
	0x43	0XB9	
	0x44	0x6A	
	0x45	0x56	
	0x46	0x61	
	0x47	0x08	
	0x48	0x0F	
	0x49	0x0F	
STB	0x2B	0x01	

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11. Register map

	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R02h	Narrow	x	x	Contrast SW	Contrast_A				14
	0	0	0	1	0	1	0	0	
R03h	Brightness								40
	0	1	0	0	0	0	0	0	
R04h	IF_SEL				NTSC/PAL		UD	SHL	6B
	0	1	1	0	1	0	1	1	
R05h	x	RSTB	x	x	x	VGHL_EN	PFM_EN	x	5C
	0	1	0	1	1	1	0	0	
R06h	HBLK_EN	x	x	VBLK					1B
	0	0	0	1	1	0	1	1	
R07h	HBLK								28
	0	0	1	0	1	0	0	0	
R0Ch	VST		x	CbCr	x	VDpol	HDpol	DCLKpol	6
	0	0	0	0	0	1	1	0	
R0Dh	Contrast_B								40
	0	1	0	0	0	0	0	0	
R0Eh	SUB_ Contrast_R								40
	0	1	0	0	0	0	0	0	
R0Fh	SUB_ Brightness_R								40
	0	1	0	0	0	0	0	0	
R10h	SUB_ Contrast_B								40
	0	1	0	0	0	0	0	0	
R11h	SUB_ Brightness_B								40
	0	1	0	0	0	0	0	0	
R13h	REGSEL	x	x	x	x	x	x	x	0
	0	0	0	0	0	0	0	0	
R1Bh	VCOMH								B3
	1	0	1	1	0	0	1	1	
R1Ch	VCOML								76
	0	1	1	1	0	1	1	0	
R2Bh	x	x	x	x	x	x	x	STB	1
	0	0	0	0	0	0	0	1	

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R2Fh	VGL_SEL			x	x	x	x	x	40
	0	1	0	0	0	0	0	0	
R5Ah	x	x	x	x	X	VGH_SEL			2
	0	0	0	0	0	0	1	0	
R5Ch	x	x	x	x	x	x	Gate Input Sequence		2
	0	0	0	0	0	0	1	0	

R30h	VSP2				VSP1				7
	0	0	0	0	0	1	1	1	
R31h	VP7				VP0				57
	0	1	0	1	0	1	1	1	
R32h	VP19				VP13				53
	0	1	0	1	0	0	1	1	
R33h	VP40				VP27				77
	0	1	1	1	0	1	1	1	
R34h	VP85				VP59				B8
	1	0	1	1	1	0	0	0	
R35h	VP159				VP118				BD
	1	0	1	1	1	1	0	1	
R36h	VP230				VP198				B8
	1	0	1	1	1	0	0	0	
R37h	VP252				VP249				E7
	1	1	1	0	0	1	1	1	
R38h	x	x	x	x	VP255				4
	0	0	0	0	0	1	0	0	
R39h	VSP4				VSP3				FF
	1	1	1	1	1	1	1	1	

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R40h	VSN2				VSN1				B
	0	0	0	0	1	0	1	1	
R41h	VN7				VN0				B8
	1	0	1	1	1	0	0	0	
R42h	VN19				VN13				AB
	1	0	1	0	1	0	1	1	
R43h	VN40				VN27				B9
	1	0	1	1	1	0	0	1	
R44h	VN85				VN59				6A
	0	1	1	0	1	0	1	0	
R45h	VN159				VN118				56
	0	1	0	1	0	1	1	0	
R46h	VN230				VN198				61
	0	1	1	0	0	0	0	1	
R47h	VN252				VN249				8
	0	0	0	0	1	0	0	0	
R48h	x	x	x	x	VN255				F
	0	0	0	0	1	1	1	1	
R49h	VSN4				VSN3				F
	0	0	0	0	1	1	1	1	

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12. Register description

Register setting – R2

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R2	1/0	0	0	0	0	0	1	0	Narrow(0)	0	0	Contrast SW(1)	Contrast_A(4h)			

R2[3:0] – CONTRAST_A: RGB contrast setting

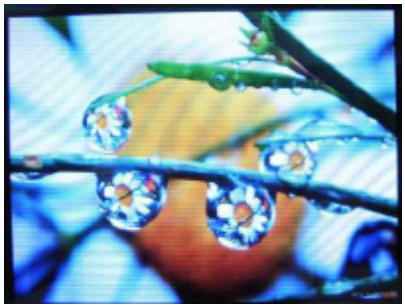
CON-TRAST_A	Contrast gain(0.25/bit)
0000	0
0100	1 (Default)
1111	3.75

R2[4] – CONTRAST_SW: 4-bit or 8-bit contrast selection

CON-TRAST_SW	Description
0	4bit contrast (R02[3:0])
1	8bit contrast (R0D[7:0]) (Default)

R2[7] – Normal/Narrow display selection

CON-TRAST_SW	Function
0	Normal display (Default)
1	Narrow Display



D7=0:Normal display

D7=1:Narrow display

The display at both side of the panel is black display at NW and NB panel.

It doesn't support 16-bit/24-bit RGB mode.

Register setting – R3

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R3	1/0	0	0	0	0	0	1	1	Brightness(40h)							

R3[7:0] – BRIGHTNESS: RGB brightness level setting

BRIGHT-NESS	Brightness gain(1 step/bit)
00h	Dark(-64)
40h	Center(0) (Default)
FFh	Bright(+191)

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Register setting – R4

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R4	1/0	0	0	0	0	1	0	0	IF_SEL(0110)				NTSC/PAL(10)		UD(1)	SHL(1)

R4[0] –SHL: Horizontal shift direction setting

HDIR	Function
0	Shift from right to left, Last data = Y1←Y2…Y959←Y960 = First data
1	Shift from left to right, First data = Y1→Y2…Y959→Y960 = Last data (Default)

R4[1] – UD: Vertical shift direction setting

VDIR	Function
0	Shift from down to up, Last line = L1←L2…L479←L480 = First line
1	Shift from up to down, First line = L1→L2…L479→L480 = Last line (Default)

R4[3:2] – NTSC/PAL: NTSC or PAL input mode selection

NTSC/PAL		MODE
D3	D2	
0	0	PAL
0	1	NTSC
1	X	Auto detection (Default)

R4[7:4] – IF_SEL: Input data format selection

IF_SEL				INPUT TIMING FORMAT
D7	D6	D5	D4	
0	0	0	0	8-bit RGB through mode
0	0	0	1	24-bit RGB DA mode
0	0	1	0	8-bit RGB DA mode
0	0	1	1	24-bit RGB through mode
0	1	0	0	16-bit YUV640 mode
0	1	1	0	16-bit YUV720 mode(Default)
1	0	0	0	8-bit RGBD 320 mode
1	0	1	0	8-bit RGBD 360 mode
1	1	0	0	8-bit YUV640 mode
1	1	0	1	8-bit YUV720 mode
1	1	1	0	16-bit RGB through mode
1	1	1	1	16-bit RGB DA mode

Register setting – R5

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5	1/0	0	0	0	0	1	0	1	0	RSTB(1)	0	1	1	VGHL_EN (1)	PFM_EN (1)	0

R5[1] – PFM_EN: Shut down for back light power converter

PFM_EN	Function
0	The back light power converter is off
1	The back light power converter is controlled by STB's power on/off sequence (Default)

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R5[2] – VGHL_EN: Shut down for VGH/VGL charge pump

VGHL_EN	Function
0	VGH/VGL charge pump is always off
1	VGH/VGL charge pump is controlled by STB's power on/off sequence (Default)

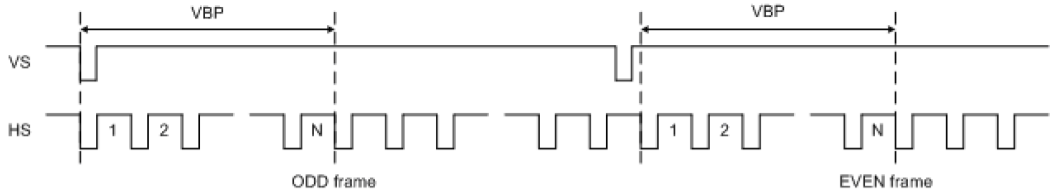
R5[6] – RSTB: Register reset setting

RSTB	Function
0	Global reset activation register. After global reset operation is down, this register will be set to "1" automatically.
1	Normal operation (Default)

Register setting – R6

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	1/0	0	0	0	0	1	1	0	HBLK_EN(0)	0	0	VBP(1Bh)				

R6[4:0] – VBP: Vertical blanking setting

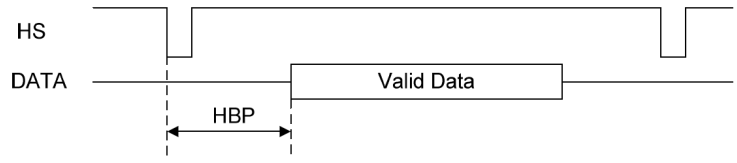


R6[4:0]	VBP		Unit
	NTSC	PAL	
00h~03h	3	3~6	HS
04h~1Ah	4~26	7~29	
1Bh	27(Default)	30(Default)	
1Fh	31	34	

HBLK_EN: Refer horizontal back porch setting table at R07h.

Register setting – R7

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R7	1/0	0	0	0	0	1	1	1	HBP(28h)							



R7[7:0] – HBP: Horizontal blanking setting

HBLK_EN (Reg. 6)	(D7-D0)	HBP	Remark
0 or 1	0~A	10	8-bit RGB
	28h	40(Default)	
	FFh	255	
0	-	40(fixed)	Others
1	0~A	10	
	28h	40	
	FFh	255	

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Register setting – R0C

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0C	1/0	0	0	0	1	1	0	0	VST (0)		0	CbCr(0)	0	VSPI(1)	HSP(1)	DCLKP (0)

R0C[0] – DCLKP: DCLK polarity selection

DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

R0C[1] – HSP: Hsync polarity selection

Hdpol	Function
0	Positive polarity
1	Negative polarity (Default)

R0C[2] – VSP: Vsync polarity selection

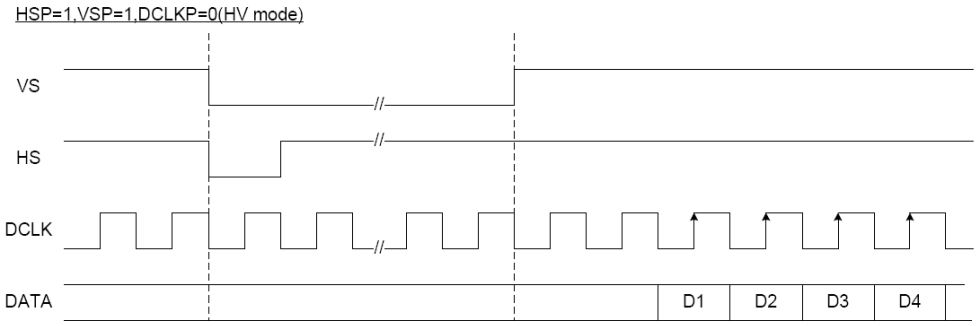
Vdpol	Function
0	Positive polarity
1	Negative polarity (Default)

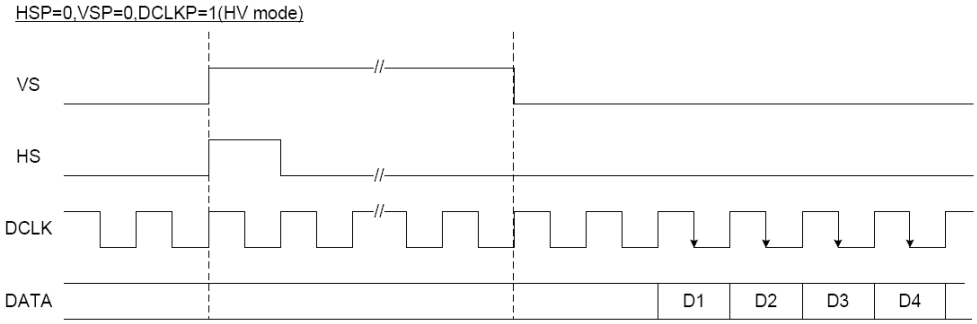
R0C[4] – CbCr: Cb & Cr exchange, valid for 8-bit YUV mode

D4	CbCr Function
0	Cb -> Y -> Cr (Default)
1	Cr -> Y -> Cb

R0C[7:6] – VST: Vertical back porch selection

Refer to Vertical back porch table





Vertical back porch table

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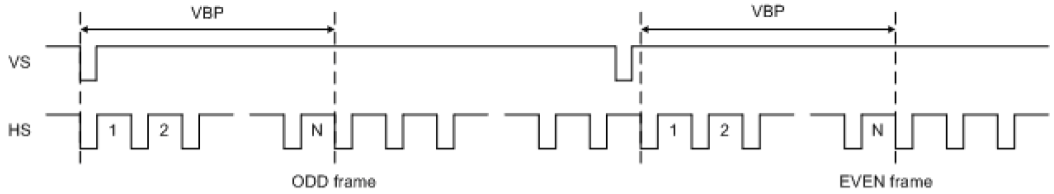

8/16/24-bit RGB mode / 320 Dummy RGB / 360 Dummy RGB

VST		Vertical back porch	Unit
D7	D6	ODD / EVEN frame	
X	0	N / N (Default)	HS
X	1	N / N-1	

N according as the register VBP(R6h[4:0])

8/16-bit YUV mode

VST		Vertical back porch	Unit
D7	D6	ODD / EVEN frame	
0	0	N / N (Default)	HS
0	1	N / N+1	
1	0	N+1 / N	
1	1	N+1 / N+1	

N according as the register VBP(R6h[4:0])

Register setting – R0D

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
RD	1/0	0	0	0	1	1	0	1	Contrast_B(40h)							

R0D[7:0] – Contrast_B: RGB contrast level setting, the gain changes (1/64)/bit

(MSB-MLB)	Contrast Gain
00h	0
40h	1(Default)
FFh	3.984

Register setting – R0E

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0E	1/0	0	0	0	1	1	1	0	0	SUB_Contrast_R(40h)						

R0E[6:0] – SUB-Contrast: R sub-contrast level setting, the gain changes (1/256)step/bit

(MSB-MLB)	Contrast Gain
00h	0.75
40h	1(Default)
7Fh	1.246

Register setting – R0F

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0F	1/0	0	0	0	1	1	1	1	0	SUB_Brightness_R(40h)						

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R0F[6:0] - SUB_Brightness: R sub-brightness level setting, setting accuracy: 1 step / bit

(MSB-MLB)	Brightness Gain
00h	Dark(-64)
40h	Center(0) (Default)
7Fh	Bright(+63)

Register setting – R10

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R10	1/0	0	0	1	0	0	0	0	0	SUB_Contrast_B(40h)						

R10[6:0] – SUB-Contrast: B sub-contrast level setting, the gain changes (1/256)step/bit

(MSB-MLB)	Contrast Gain
00h	0.75
40h	1(Default)
7Fh	1.246

Register setting – R11

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R11	1/0	0	0	1	0	0	0	1	0	SUB_Brightness_B(40h)						

R11[6:0] - SUB_Brightness: B sub-brightness level setting, setting accuracy: 1 step / bit

(MSB-MLB)	Brightness Gain
00h	Dark(-64)
40h	Center(0) (Default)
7Fh	Bright(+63)

Register setting – R13

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R13	1/0	0	0	1	0	0	1	1	REGSEL	0	0	0	0	0	0	0

R13[7] – REGSEL: OTP function control

REGSEL	Description
0	VCOMH and VCOML were according as OTP memory (Default)
1	VCOMH and VCOML were according as the registers(R1Bh/R1Ch)

Note: If OTP didn't programming, VCOMH and VCOML were according as the registers

Register setting – R1B

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R1B	1/0	0	0	1	1	0	1	1	VCOMH(9Dh)							

R1B[7:0] – VCOMH: VCOMH level adjustment(1 step : 10 mV)

VCOMH level	(Unit : V)
00h	2.35
…	
9Dh	3.92 (Default)
…	
FBh	4.86

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FCh	4.87
FDh	4.88
FEh	4.89
FFh	4.9

Register setting – R1C

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R1C	1/0	0	0	1	1	1	0	0	VCOML(60h)							

R1C[7:0] – VCOML: VCOML level adjustment(1 step : 10 mV)

VCOMLlevel	(Unit : V)
00h	-2.7
…	
60h	-1.74 (Default)
…	
F9h	-0.21
FAh	-0.2
FBh	-0.2
FCh	-0.2
FDh	-0.2
FEh	-0.2
FFh	-0.2

Register setting – R2B

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R2B	1/0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	STB(0)

R2B[0] – STB: Standby (power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

Register setting – R2F

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R2F	1/0	0	1	0	1	1	1	1	VGL_SEL(010)			0	0	0	0	0

R2F[7:5] – VGL_SEL: VGL voltage selection

Bit			Output
D7	D6	D5	VGL (V)
0	0	0	-8.0
0	0	1	-9.0
0	1	0	-10.0 (Default)
0	1	1	-11.0
1	0	0	-7.0
1	0	1	-7.0
1	1	0	-12.0
1	1	1	-12.0

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Register setting – R5A

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5A	1/0	1	0	1	1	0	1	0	0	0	0	0	0	VGH_SEL(101)		

R5A[2:0] – VGH_SEL: VGH voltage selection

Bit			Output
D2	D1	D0	VGH (V)
0	0	0	13.0
0	0	1	14.0
0	1	0	15.0 (Default)
0	1	1	16.0
1	0	0	17.0
1	0	1	18.0
1	1	0	18.0
1	1	1	18.0

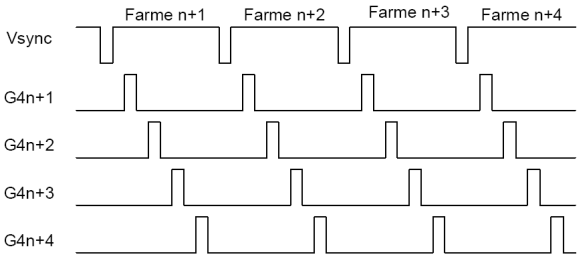
Register setting – R5C

Reg	Address								Data							
NO	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5C	1/0	1	0	1	1	1	0	0	0	0	0	0	0	0	GO_SEQ	

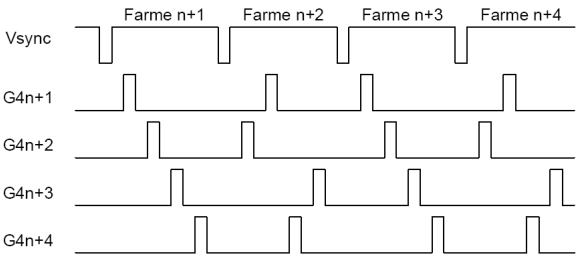
R5C[1:0] – GO_SEQ: Gate output sequence setting

NTSC/PAL		Description
D1	D0	
0	0	Traditional gate output sequence
0	1	Other gate output sequence1
1	0	Other gate output sequence2 (Default)
1	1	Other gate output sequence3

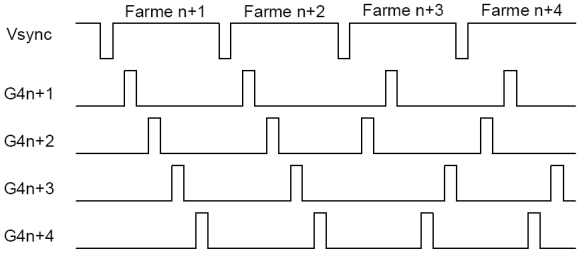
Traditional Gate Output Sequence



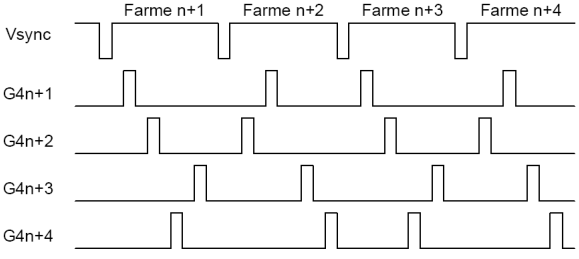
Other Gate Output Sequence 2



Other Gate Output Sequence 1



Other Gate Output Sequence 3



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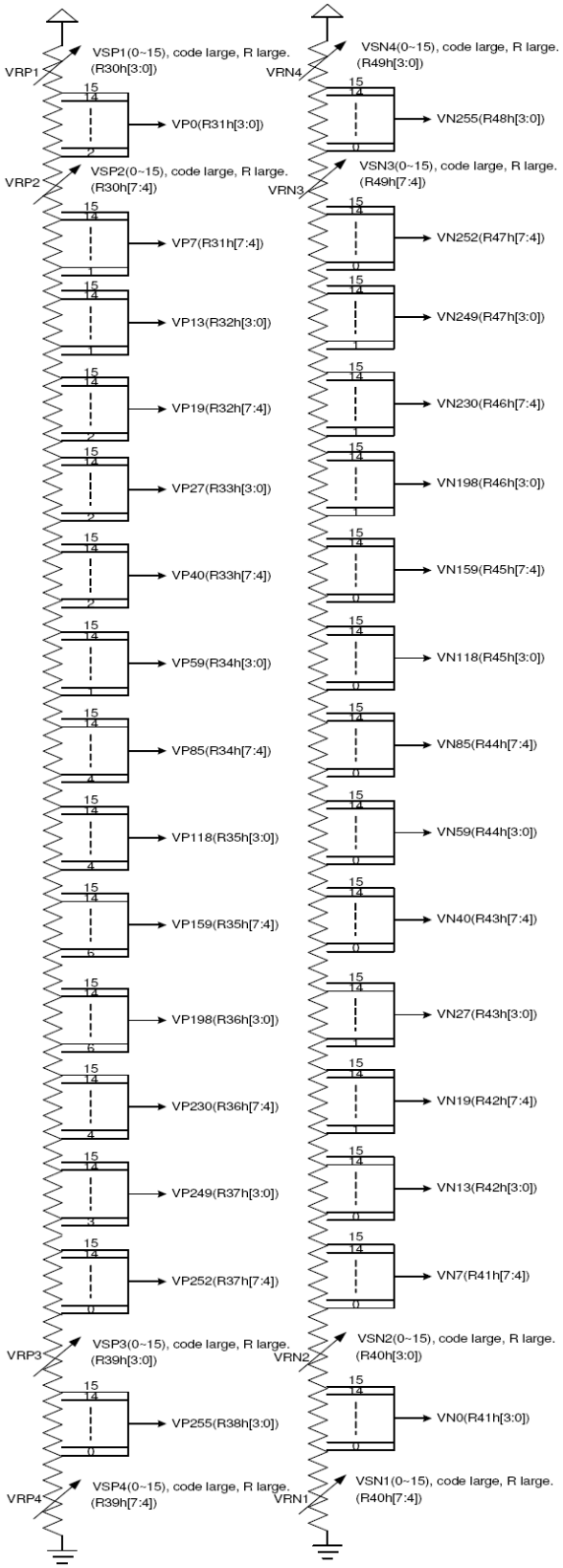
Gamma Register Setting- R30h~R49h

Gamma point	Register	Setting range	Gamma point	Register	Setting range
VSP1	R30h[3:0]	0~15	VSN4	R49h[7:4]	0~15
VP0	R31h[3:0]	2~15	VN255	R48h[3:0]	0~15
VSP2	R30h[7:4]	0~15	VSN3	R49h[3:0]	0~15
VP7	R31h[7:4]	1~15	VN252	R47h[7:4]	0~15
VP13	R32h[3:0]	1~15	VN249	R47h[3:0]	1~15
VP19	R32h[7:4]	2~15	VN230	R46h[7:4]	1~15
VP27	R33h[3:0]	2~15	VN198	R46h[3:0]	1~15
VP40	R33h[7:4]	2~15	VN159	R45h[7:4]	0~15
VP59	R34h[3:0]	1~15	VN118	R45h[3:0]	0~15
VP85	R34h[7:4]	4~15	VN85	R44h[7:4]	0~15
VP118	R35h[3:0]	4~15	VN59	R44h[3:0]	0~15
VP159	R35h[7:4]	6~15	VN40	R43h[7:4]	0~15
VP198	R36h[3:0]	6~15	VN27	R43h[3:0]	1~15
VP230	R36h[7:4]	4~15	VN19	R42h[7:4]	1~15
VP249	R37h[3:0]	3~15	VN13	R42h[3:0]	0~15
VP252	R37h[7:4]	0~15	VN7	R41h[7:4]	0~15
VSP3	R39h[3:0]	0~15	VSN2	R40h[7:4]	0~15
VP255	R38h[3:0]	0~15	VN0	R41h[3:0]	0~15
VSP4	R39h[7:4]	0~15	VSN1	R40h[3:0]	0~15

Note:

1. The registers VSPn/VSNn adjust the value of the resistor VRPn/VRNn.
2. When n=1 and n=4 affect the voltage of all gamma point at the resistor string.
3. When n=2 affects the voltage of all gamma point at resistor string besides VP0/VN0.
4. When n=3 affects the voltage of all gamma point at resistor string besides VP255/VN255.



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13. OPTICAL CHARACTERISTICS

13-1. Optical Specification

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles		Θ11	CR ≥ 10		60	-	Degree	Note 13-1
		Θ12			60	-		
		Θ21			50	-		
		Θ22			55	-		
Contrast Ratio		CR	Θ=0°		500	-		Note 13-2
Response Time		Tr+Tf		-	35		ms	Note 13-3
Luminance (I_F=25mA)		L		400	500		cd/m^2	Note 13-4
Chromaticity	White	x_W		0.25	0.30	0.35		Note 13-5
		y_W		0.27	0.32	0.37		
Uniformity			Θ=0°	70			%	

13-2. Basic Measure Conditions

(1) Driving voltage

Vcc= 3.3 V

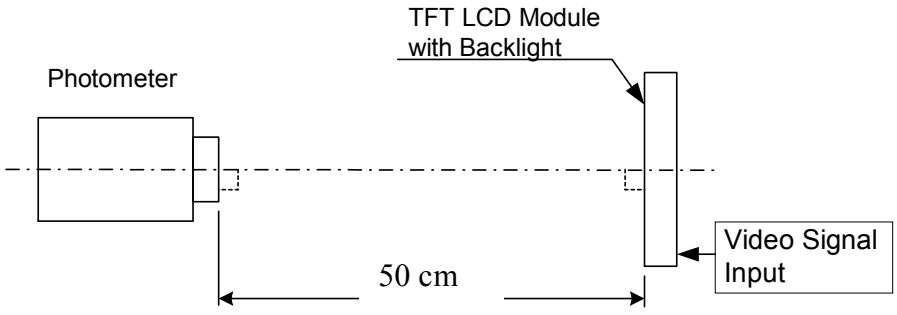
(2) Ambient Temperature: Ta=25℃

(3) Testing Point: Measure in the display center point and the test angle Θ=0°

(4) LED Current: I_F=25mA.

(5) Testing Facility

Environmental illumination: ≤ 1 Lux



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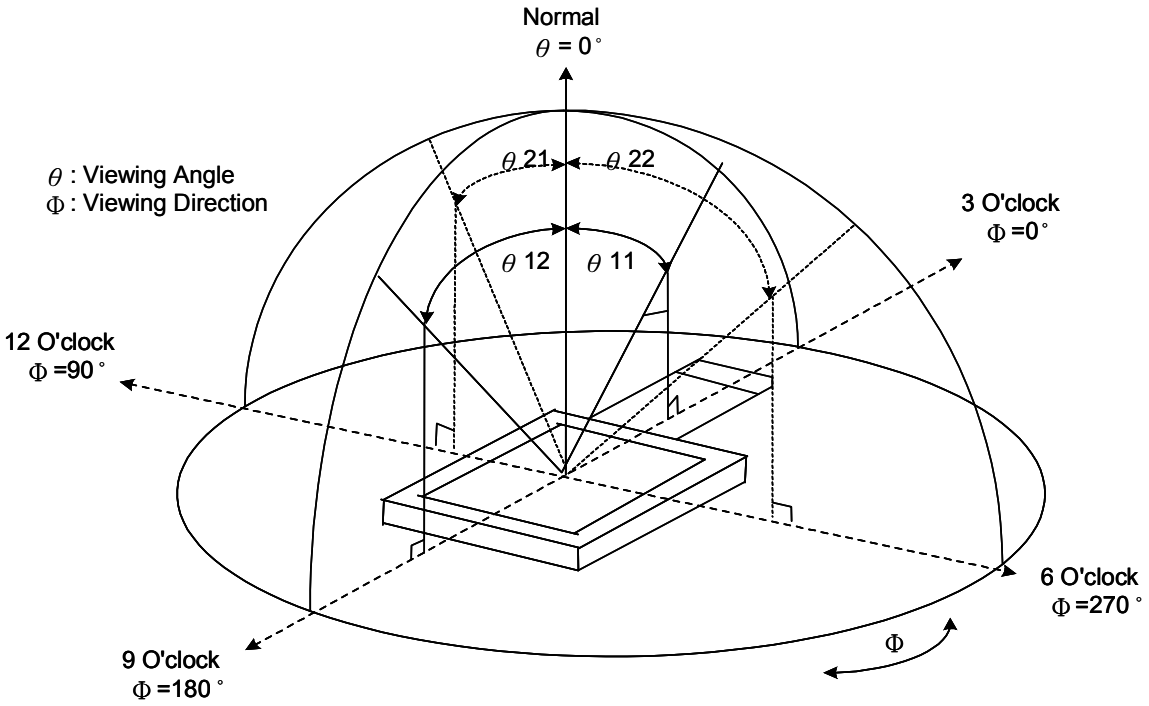
Note 13-1: Viewing angle diagrams:

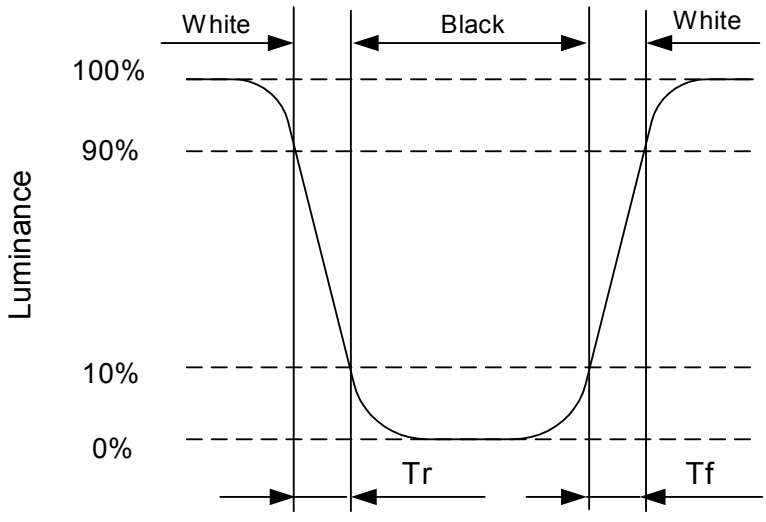


Note 13-2: Contrast Ratio:

Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 13-3: Definition of response time:



Note 13-4: Luminance:

Test Point: Display Center

Note 13-5: Chromaticity: The same test condition as Note 13-4.

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14. RELIABILITY

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta= 0℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+80℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta=-30℃, 240hrs
6	Thermal Shock (non-operation)	-30℃←→80℃, 50 cycles 30 min 30 min
7	Resistance to Static Electricity Discharge (non-operation)	C=200pF, R=0Ω; Discharge: ±150V 3 times / Terminal
8	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
9	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Twice

Ta: Ambient Temperature

＊ For environment stress test, the image quality guarantee after recover time 2 hours at ambient environment.

＊ Polarizer cosmetic is not guarantee after reliability test.

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15. HANDLING CAUTIONS

15.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommend ESD strategy

(1) In handling LCD panel, please wear non-charged material gloves. And the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD prohibition strategy.

(3) In handling the panel, ionize flowing decrease the charge in the environment is necessary.

(4) In the process of assembly the module, shield case should connect to the ground.

15.2 Environment

(1) Working environment of the panel should in the clean room.

(2) The front polarizer is easy damaged, handle it carefully and do not scratch it by sharp material.

(3) Panel has polarizer protective film in the surface please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

15.3 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) The connection area of FPC and panel is very weak, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

(5) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

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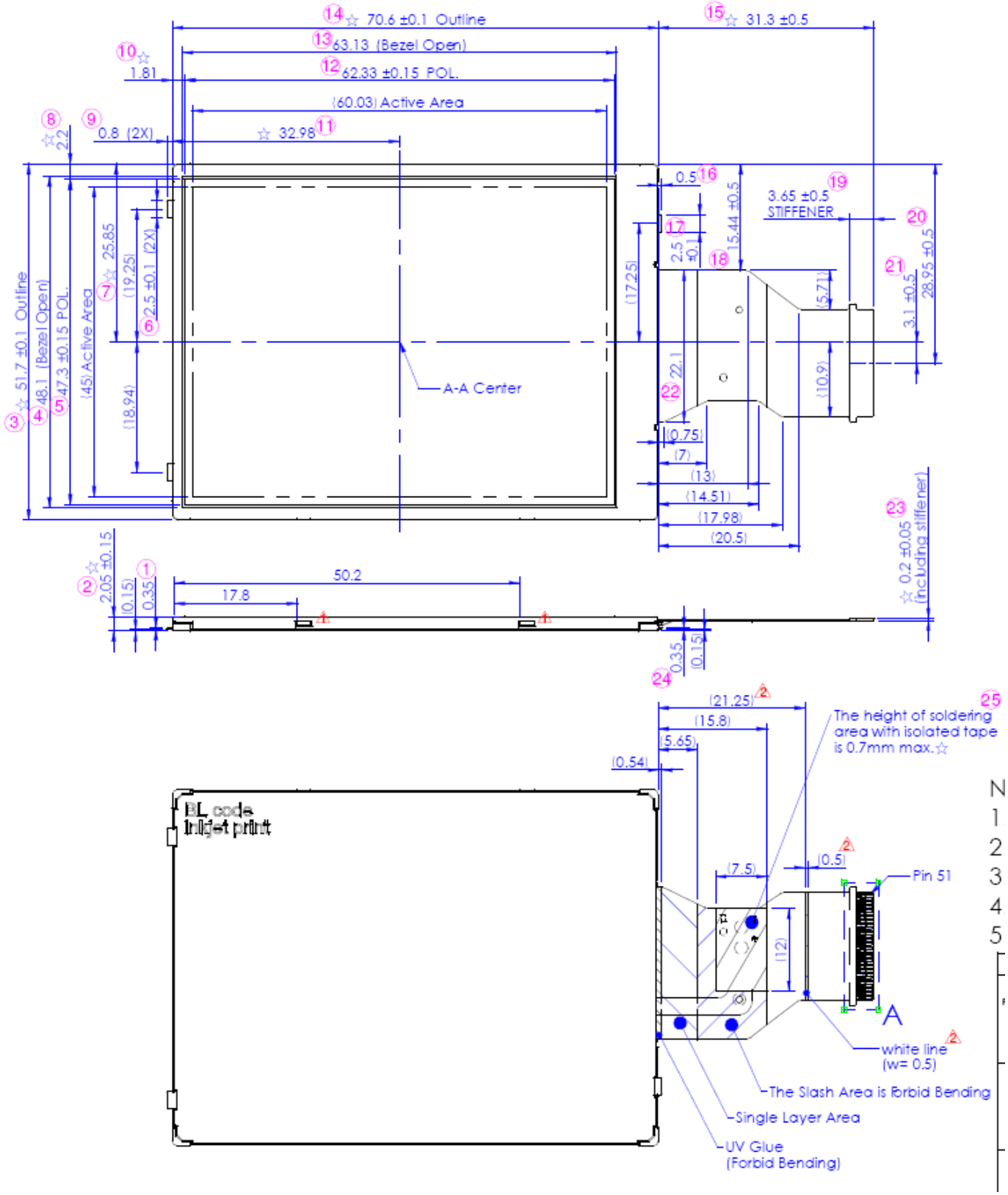
16. MECHANICAL DRAWING



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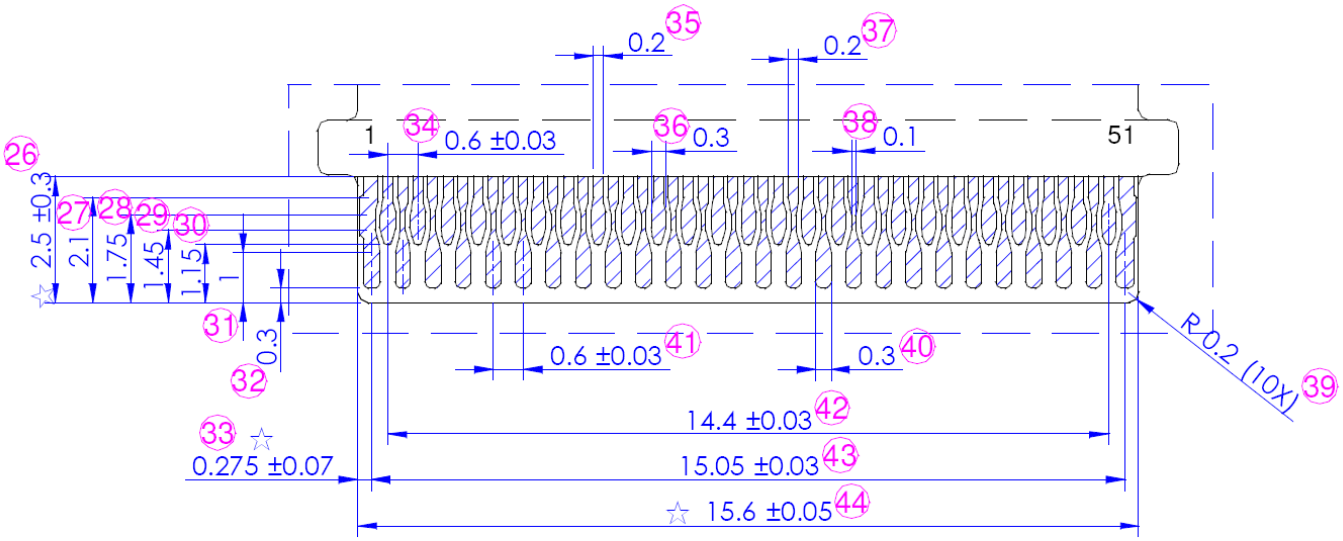

Detail A
8:1

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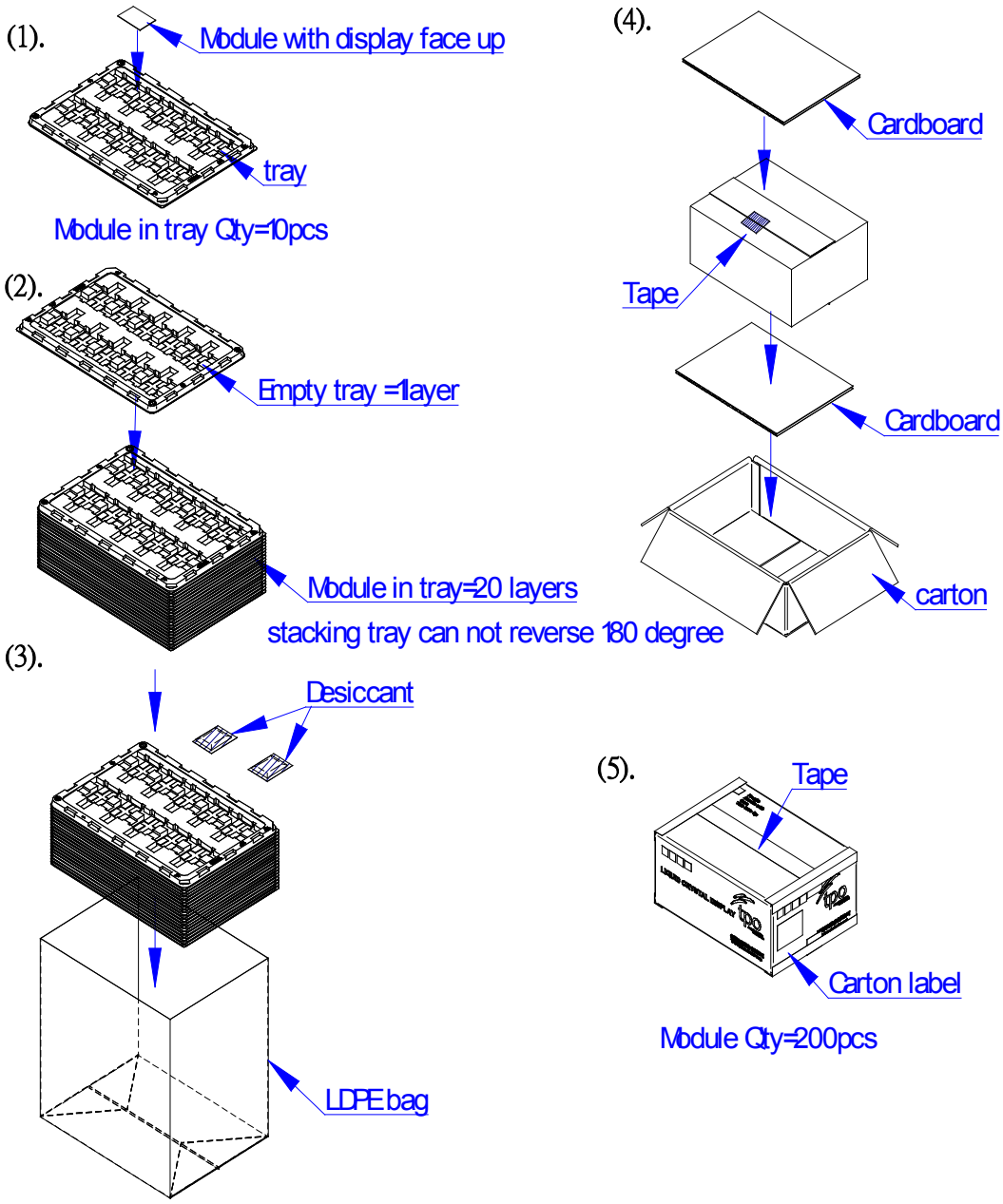
17. Packing Drawing



3.0" module (EJ030NA-01B) delivery packing method

(1). Module packed into tray cavity (with Module display face up).

(2). Tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton. Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape.

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(6). Lot Number

Describe: there are two lines. In the first line, the first is model, such as" 990001265", the second is type name, such as "EJ030NA-01B", and the second line is LN of 13 sequences.

Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	Z12	Z13

Definition as follows:

Z1: Code of assembly factory buildings, LCM1:K ; LCM2:H

Z2: Lot type: N, R, S, M……

Z3: The last code is producing year, such as 2010 is"0 ".

Z4~Z5: The code is producing week

Z6~Z9: The codes are SN.

Z10: The code of reserve number is A.

Z11: The No.11 code is dot.

Z12~Z13: The codes are Sub ID.

(7). Bottom Metal Shot-Case Mark

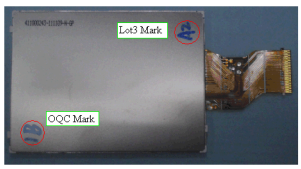
Describe: The mark defined with the permutation of numeral and alphabet in random.

Each mark represented for one operator and won't be repeated.

Lot3 marks on right-bottom corner and OQC marks on left-top corner (FPC toward down side).

OQC mark will keep 100% mark until customer's approval that CMI can sampling this process.

* When wipe mark out from S/C, please don't let Alcohol solvent permeate into panel inside.



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