

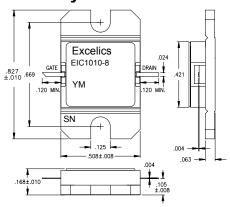
EIC1010-8

UPDATED 02/15/2005

10.00-10.70 GHz 8-Watt Internally Matched Power FET

FEATURES

- 10.00-10.70GHz Bandwidth
- Input/Output Impedance Matched to 50 Ohms
- +39.5 dBm Output Power at 1dB Compression
- 7.0 dB Power Gain at 1dB Compression
- 31% Power Added Efficiency
- -46 dBc IM3 at Po = 28.5 dBm SCL
- **Hermetic Metal Flange Package**
- 100% Tested for DC, RF, and R_{TH}



ELECTRICAL CHARACTERISTICS (Ta = 25°C)



Caution! ESD sensitive device.

SYMBOL	PARAMETERS/TEST CONDITIONS ¹	MIN	TYP	MAX	UNITS
P _{1dB}	Output Power at 1dB Compression $f = 10.00-10.70GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 2200\text{mA}$	38.5	39.5		dBm
G _{1dB}	Gain at 1dB Compression $f = 10.00-10.70GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 2200\text{mA}$	6.0	7.0		dB
ΔG	Gain Flatness $f = 10.00-10.70GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 2200\text{mA}$			±0.6	dB
PAE	Power Added Efficiency at 1dB Compression $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 2200 \text{mA}$ f = 10.00-10.70GHz		31		%
Id _{1dB}	Drain Current at 1dB Compression f = 10.00-10.70GHz		2300	2600	mA
IM3	Output 3rd Order Intermodulation Distortion $\Delta f = 10$ MHz 2-Tone Test; Pout = 28.5 dBm S.C.L ² $V_{DS} = 10$ V, $I_{DSQ} \approx 65\%$ IDSS $f = 10.70$ GHz	-43	-46		dBc
I _{DSS}	Saturated Drain Current $V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}$		4000	5000	mA
V_P	Pinch-off Voltage $V_{DS} = 3 \text{ V}, I_{DS} = 40 \text{ mA}$		-2.5	-4.0	V
R _{TH}	Thermal Resistance ³		3.5	4.0	°C/W

¹⁾ Tested with 100 Ohm gate resistor.

ABSOLUTE MAXIMUM RATING^{1,2}

SYMBOL	CHARACTERISTIC	VALUE
V_{DS}	Drain to Source Voltage	10 V
V_{GS}	Gate to Source Voltage	-4.5 V
I _{DS}	Drain Current	IDSS
I _{GSF}	Forward Gate Current	80 mA
P _{IN}	Input Power	@ 3dB compression
P_{T}	Total Power Dissipation	38 W
T _{CH}	Channel Temperature	175°C
T _{STG}	Storage Temperature	-65/+175°C

Operating the device beyond any of the above ratings may result in permanent damage or reduction of MTTF. Bias conditions must also satisfy the following equation $P_T < (T_{CH} - T_{PKG})/R_{TH}$; where $T_{PKG} = t_{PKG} = t_{PKG}$ and $P_T = (V_{DS} * I_{DS}) - (P_{OUT} - P_{IN})$.

²⁾ S.C.L. = Single Carrier Level.

³⁾ Overall Rth depends on case mounting.