



EDI8M8256C/LP/P

Two Megabit SRAM Module

256Kx8 Static RAM CMOS, Module

The EDI8M8256C/LP/P is a 4096K bit CMOS Static RAM based on eight 32Kx8 Static RAMs mounted on a multi-layered ceramic substrate.

Functional equivalence to the monolithic four megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address to select one of the 32Kx8 Static RAMs.

The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device, to ensure compatibility with future monolithics.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8256C/LP/P requires no clocks or refreshing for operation.

The 85-150ns device is available with Low Power (P) and Low Power with Data Retention (LP).

EDI Military Modules are built with RAMs that are compliant to MIL-STD-883, paragraph 1.2.1.

Features

256Kx8 bit CMOS Static
Random Access Memory

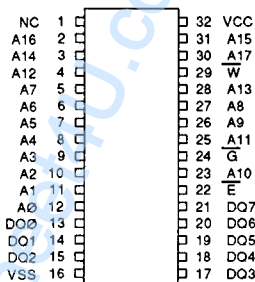
- Access Times 70 thru 150ns
- Data Retention Function (LP version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

32 pin DIP, JEDEC Approved Pinout

- Ceramic LCCs on Ceramic Substrate, No. 119
- Plastic VSOPs on Ceramic Substrate, No. 107

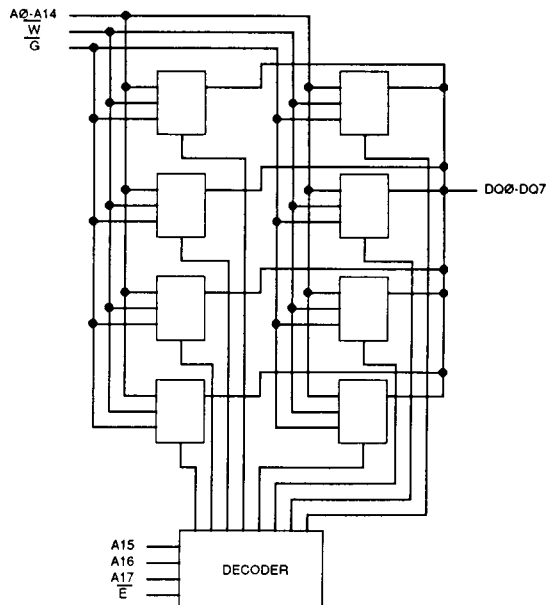
Single +5V ($\pm 10\%$) Supply Operation

Pin Configuration and Block Diagram



Pin Names

A0-A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS -0.5V to 7.0V
 Operating Temperature TA (Ambient)
 Commercial 0°C to +70°C
 Industrial -40°C to +85°C
 Military -55°C to +125°C
 Storage Temperature
 Plastic -55°C to +125°C
 Ceramic -65°C to +150°C
 Power Dissipation 1 Watt
 Output Current 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels VSS to 3.0V
 Input Rise and Fall Times 5ns
 Input and Output Timing Levels 1.5V
 Output Load 1TTL, CL = 100pF
 (note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Temp Range	Min	Typ*	Max	Units
Operating Power	ICC1	$\overline{W}, \overline{E} = VIL, I/O = 0mA$	Com/Ind	--	70	90	mA
Supply Current		Min Cycle	Mil		80	110	mA
Standby (TTL) Power	ICC2	$\overline{E} \geq VIH, VIN \leq VIL$	Com/Ind	--	10	25	mA
Supply Current		$VIN \geq VIH$	Mil	--	20	40	mA
Full Standby Power	ICC3	$\overline{E} \geq VCC - 0.2V$	Com/Ind/C		2	5	mA
Supply Current		$VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$	Mil / C	--	5	10	mA
			Mil / LP/P	--	2	5	mA
Input Leakage Current	ILI	$VIN = 0V$ to VCC		--	--	± 10	μA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC		--	--	± 10	μA
Output High Voltage	VOH	$IOH = -1.0mA$		2.4	--	--	V
Output Low Voltage	VOL	$IOL = 2.1mA$		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

G	E	W	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f = 1.0MHz, VIN = VCC or VSS)

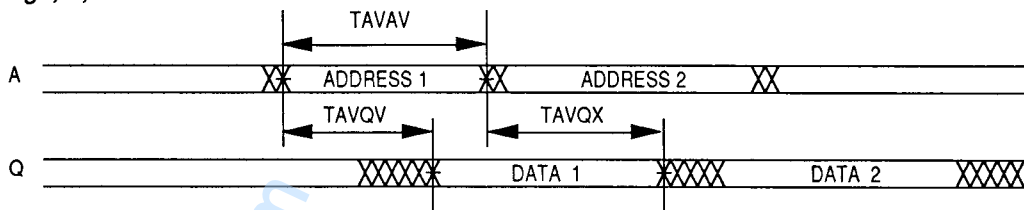
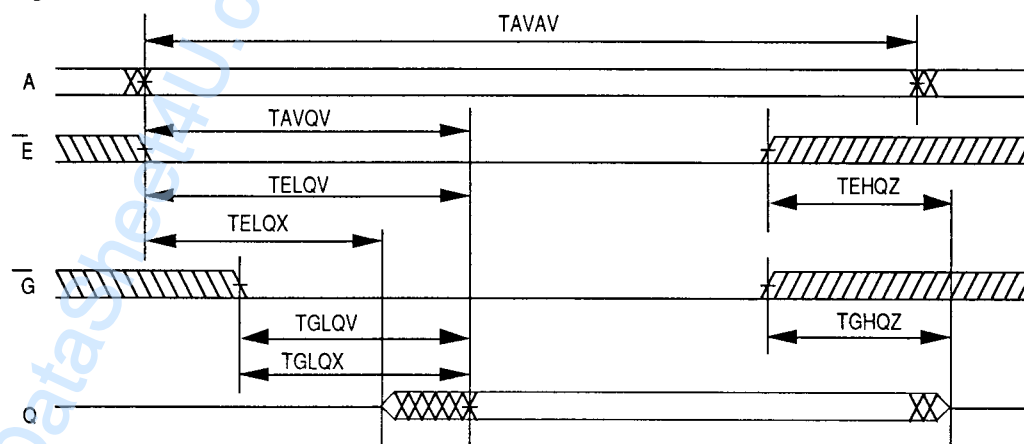
Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	45	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$)	CC	20	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

These parameters are sampled, not 100% tested.

AC Characteristics**Read Cycle**

Parameter	Symbol	70ns		85ns		100ns		120ns		150ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	70		85		100		120		150		ns
Address Access Time	TAVQV		70		85		100		120		150	ns
Chip Enable Access Time	TELQV		70		85		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		5		5		ns
Output Enable to Output Valid	TGLQV		30		45		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	0		0		0		0		0		ns
Chip Disable to Output in High Z (1)	TEHQZ		30		35		40		45		50	ns
Output Disable to Output in High Z (1)	TGHQZ		30		35		40		45		50	ns
Output Hold from Address Change	TAVQX	3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

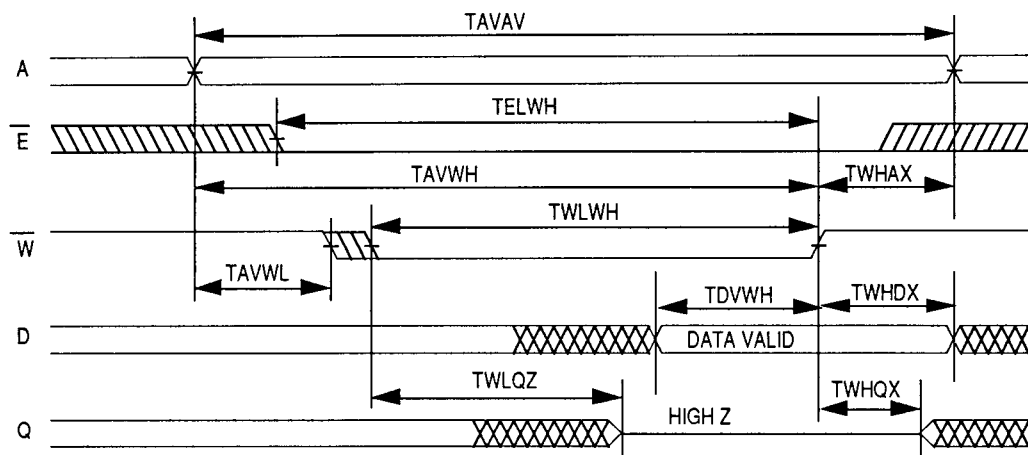
Read Cycle 1***W High; $\overline{G}$, $\overline{E}$ Low*****Read Cycle 2*****W High***

AC Characteristics**Write Cycle**

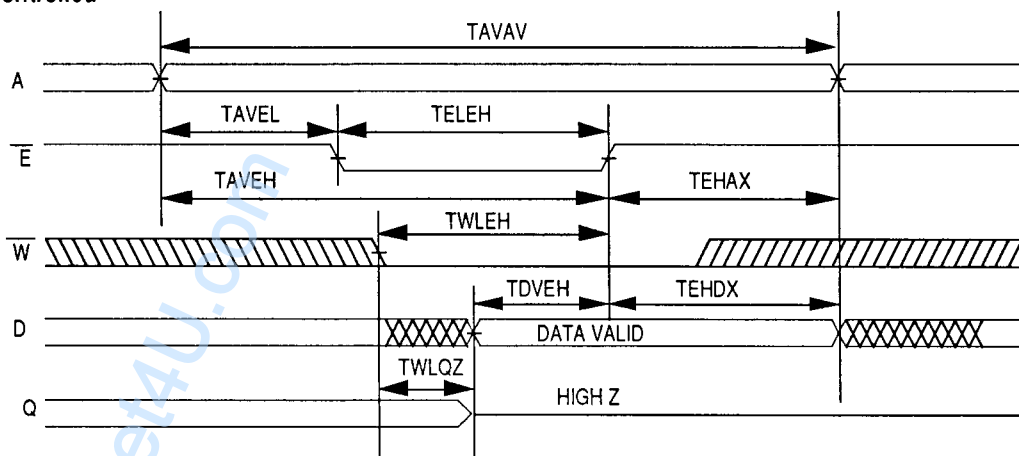
Parameter	Symbol		70ns		85ns		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		70		85		100		120		150		ns
Chip Enable to	TELWH	$\overline{W}$	45		70		80		100		110		ns
End of Write	TELEH	$\overline{E}$	45		70		80		100		110		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	45		70		80		100		110		ns
	TAVEH	$\overline{E}$	45		70		80		100		110		ns
Write Pulse Width	TWLWH	$\overline{W}$	45		70		80		100		110		ns
	TWLEH	$\overline{E}$	45		70		80		100		110		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	25	0	35	0	40	0	45	0	50	ns
Data to Write Time	TDVWH	$\overline{W}$	30		35		40		45		50		ns
	TDVEH	$\overline{E}$	30		35		40		45		50		ns
Output Active from End of Write (1)	TWHQX		3		5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 W Controlled



Write Cycle 2 $\overline{E}$ Controlled



Data Retention Characteristics

LP Version Only

85-150ns only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max			Unit
		$\overline{E} \geq VDD - 0.2V$ $VIN \geq VDD - 0.2V$ or $VIN \leq 0.2V$				70°C	85°C	125°C	
Data Retention Voltage	VDD			2	--	--	--	--	V
Data Retention Quiescent Current	ICCDR		2V	--	10	125	185	850	μA
			3V	--	20	200	250	1100	μA
Chip Disable to Data Retention Time	TCDR			0		--	--	--	ns
Operation Recovery Time	TR			5		--	--	--	ms

Data Retention
 $\overline{E}$ Controlled

