



Features

64Kx32 bit CMOS Static

Random Access Memory Array

- Fast Access Times: 12*, 15, 20, and 25ns
- Individual Byte Selects
- User Configurable Organization with Minimal Additional Logic
- Master Output Enable and Write Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Surface Mount Package

- 68 Lead PLCC, No. 99 (JEDEC-MO-47AE)
- Small Footprint, 0.990 Sq. In.
- Multiple Ground Pins for Maximum Noise Immunity

Single +5V ($\pm 5\%$) Supply Operation

*Advance Information

64Kx32 CMOS High Speed Static RAM

The EDI8L3265C is a high speed, high performance, four megabit density Static RAM organized as a 64Kx32 bit array.

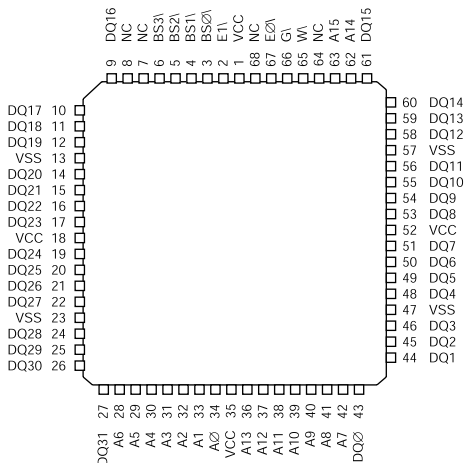
Four Byte Selects, two Chip Enables, Write Control, and Output Enable provide the user with a flexible memory solution. The user may independently enable each of the four bytes, and, with minimal additional peripheral logic, the unit may be configured as a 128Kx16 array.

Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

The EDI8L3265C, allows 2 megabits of memory to be placed in less than 0.990 square inches of board space. The EDI8L3265C can be upgraded to 128K, 256K or 512Kx32 in the same footprint using the EDI8L32128, EDI8L32256 or the EDI8L32512C. (See page 6 for upgrade paths).

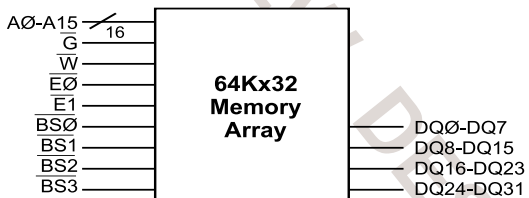
Note: Solder Reflow temperatures should not exceed 260°C for 10 seconds.

Pin Configurations and Block Diagram



Pin Names

A0-A15	Address Inputs
E0-E1	Chip Enables (one per word)
BS0-BS3	Byte Selects (One per Byte)
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V $\pm 5\%$)
VSS	Ground
NC	No Connection



Notes: 1. See page 6 for upgrade paths.



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	3.0 Watts
Output Current	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.75	5.0	5.25	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

Figure 1

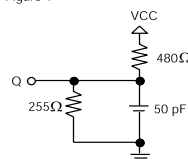
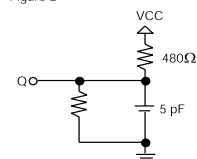


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max	Unit
Operating Power	ICC1	$\bar{W} = V_{IL}$, I/O = 0mA, Min Cycle	500	460	mA
Supply Current				420	
Standby (TTL)	ICC2	$\bar{E} \geq V_{IH}$, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, f=0MHz	60	60	mA
Supply Current				60	
Full Standby	ICC3	$\bar{E} \geq V_{CC}-0.2V$	20	20	mA
Supply Current CMOS		$V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$		20	
Input Leakage Current	ILI	$V_{IN} = 0V$ to VCC	±10	±10	µA
Output Leakage Current	ILO	$V_{I/O} = 0V$ to VCC	±10	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4		V
Output Low Voltage	VOL	IOL = 8.0mA	0.4	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

*Advanced Information

Truth Table

$\bar{E}$	W	$\bar{G}$	BS0-3	Mode	Output	Power
H	X	X	X	Standby	High Z	ICC2, ICC3
L	H	H	X	Output Disable	High Z	ICC1
L	X	X	H	Output Disable	High Z	ICC1
L	H	L	L	Read	Dout	ICC1
L	L	X	L	Write	Din	ICC1

X Means Don't Care

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CA	20	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	W, $\bar{G}$	16	pF
Chip Enable Lines	$\bar{E}$, $\bar{BS}$	9	pF

These parameters are sampled, not 100% tested.

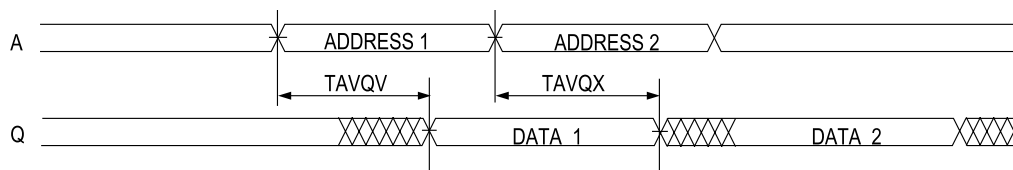
AC Characteristics Read Cycle

Parameter	Symbol		12ns*		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	12		15		20		25		ns
Address Access Time	TAVQV	TAA		12		15		20		25	ns
Chip Enable Access Time	TELQV	TACS		12		15		20		25	ns
Byte Select Access Time	TBLQV	TBA		12		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Byte Select to Output in Low Z	TBLQX	TBLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		7		8		10		10	ns
Byte Select to Output in High Z	TBHQZ	TBHZ		7		8		10		10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		6		8		10	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	2		2		2		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		4		5		8		10	ns

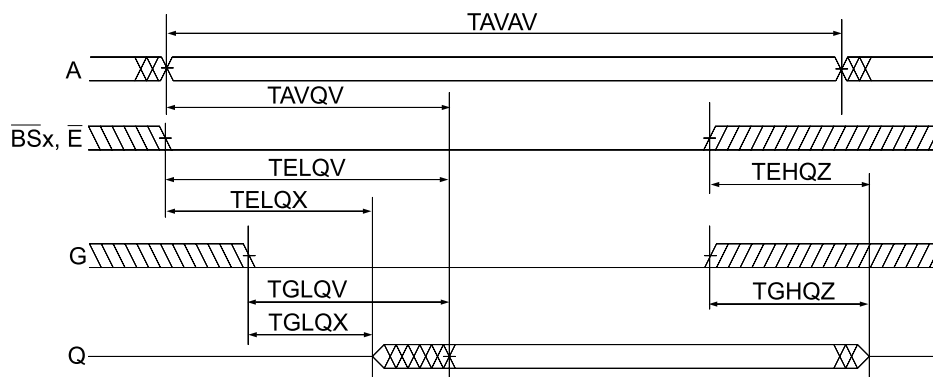
Note 1: Parameter guaranteed, but not tested.

*Advanced Information

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High



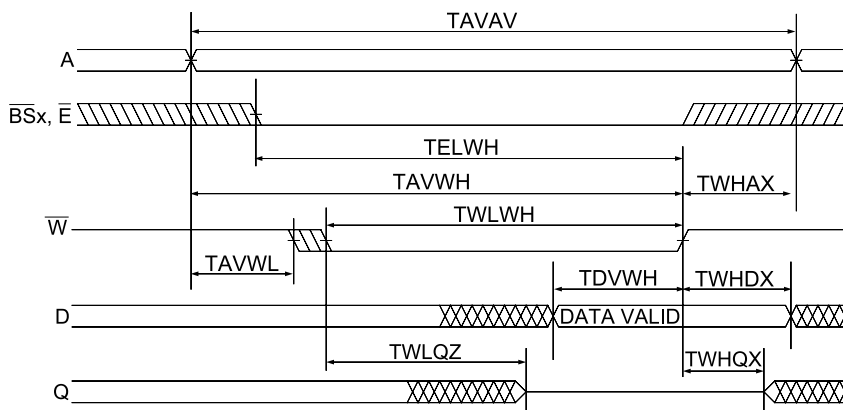
AC Characteristics Write Cycle

Parameter	Symbol		12ns*		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	12		15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	8		9		15		20		ns
	TELEH	TCW	8		9		15		20		ns
Byte Select to end of Write	TBLWH	TBW	8		9		15		20		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	9		10		15		15		ns
	TAVEH	TAW	9		10		15		15		ns
Write Pulse Width	TWLWH	TWP	9		10		15		15		ns
	TWLEH	TWP	9		10		15		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	7	0	10	ns
Data to Write Time	TDVWH	TDW	5		6		8		12		ns
	TDVEH	TDW	5		6		8		12		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		2		ns

Note 1: Parameter guaranteed, but not tested.

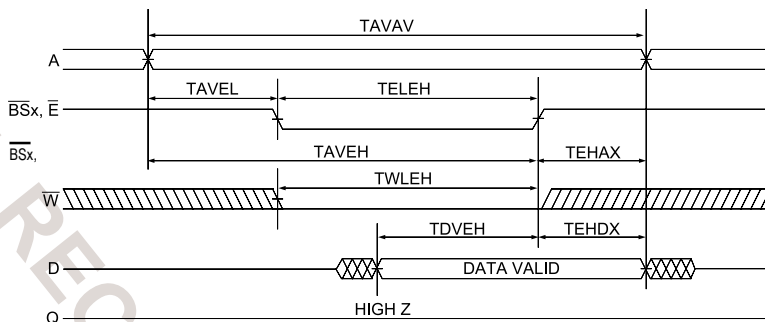
*Advanced Information

Write Cycle 1 - $\overline{W}$ Controlled





Write Cycle 2 - $\bar{E}$ Controlled



Ordering Information

Commercial (0°C to 70°C)

Part Number	Speed (ns)	Package No.
EDI8L3265C12AC*	12	99
EDI8L3265C15AC	15	99
EDI8L3265C20AC	20	99
EDI8L3265C25AC	25	99

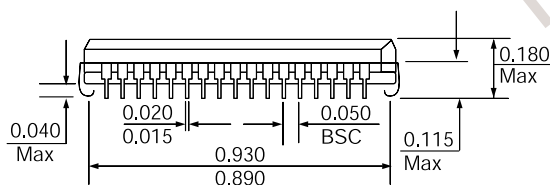
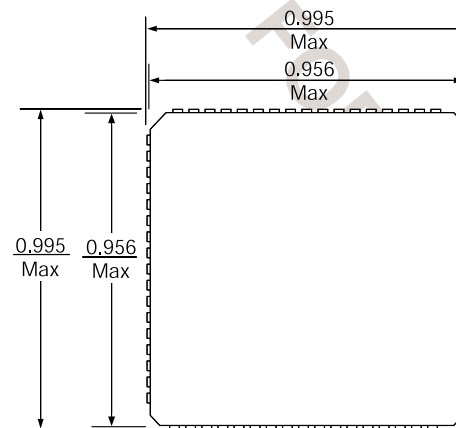
*Advanced Information

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L3265C15AI	15	99
EDI8L3265C20AI	20	99
EDI8L3265C25AI	25	99

Package Description

Package No. 99
68 Lead PLCC
JEDEC M0-47AE





8L3265C

Pinout diagram for the 8L3265C integrated circuit. The diagram shows a 60-pin package with pins numbered 1 to 60. The pinout is as follows:

- Pin 1: Vcc
- Pin 2: GND
- Pin 3: Vcc
- Pin 4: GND
- Pin 5: Vcc
- Pin 6: GND
- Pin 7: Vcc
- Pin 8: GND
- Pin 9: Vcc
- Pin 10: GND
- Pin 11: Vcc
- Pin 12: GND
- Pin 13: Vcc
- Pin 14: GND
- Pin 15: Vcc
- Pin 16: GND
- Pin 17: Vcc
- Pin 18: GND
- Pin 19: Vcc
- Pin 20: GND
- Pin 21: Vcc
- Pin 22: GND
- Pin 23: Vcc
- Pin 24: GND
- Pin 25: Vcc
- Pin 26: GND
- Pin 27: Vcc
- Pin 28: GND
- Pin 29: Vcc
- Pin 30: GND
- Pin 31: Vcc
- Pin 32: GND
- Pin 33: Vcc
- Pin 34: GND
- Pin 35: Vcc
- Pin 36: GND
- Pin 37: Vcc
- Pin 38: GND
- Pin 39: Vcc
- Pin 40: GND
- Pin 41: Vcc
- Pin 42: GND
- Pin 43: Vcc
- Pin 44: GND
- Pin 45: Vcc
- Pin 46: GND
- Pin 47: Vcc
- Pin 48: GND
- Pin 49: Vcc
- Pin 50: GND
- Pin 51: Vcc
- Pin 52: GND
- Pin 53: Vcc
- Pin 54: GND
- Pin 55: Vcc
- Pin 56: GND
- Pin 57: Vcc
- Pin 58: GND
- Pin 59: Vcc
- Pin 60: GND