



1Mx32 FLASH MODULE

DESCRIPTION

The EDI7F331MC and EDI7F2331MC are organized as one and two banks of 1Mx32 respectively. The modules are based on AMDs AM29F080 - 1Mx8 Flash device in TSOP packages which are mounted on an FR4 substrate.

Both modules offer access times between 80 and 150ns allowing for operation of high-speed microprocessors without wait states.

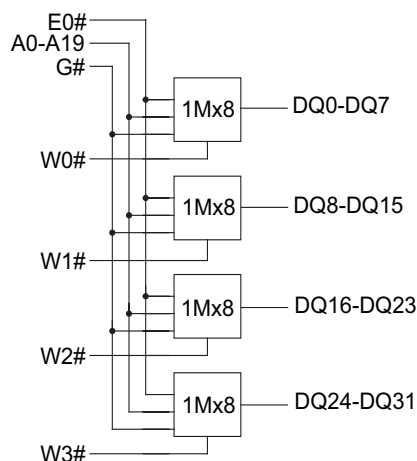
FEATURES

- 1Mx32 and 2x1Mx32 Densities
- Based on AMD - AM29F080 Flash Device
- Fast Read Access Time - 80ns
- 5V Only Reprogramming
- Sector Erase Architecture
 - Uniform sectors of 64 Kbytes each
 - Any combination of sectors can be erased
 - Also supports full chip erase
- Sector Protection
 - Hardware method that disables any combination of sectors from write or erase operations
- Embedded Erase Algorithms
 - Automatically preprograms and erases the chip or any combination of sectors
- Embedded Program Algorithms
 - Automatically programs and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Low Power Dissipation
 - 60mA per Device Active Current
 - 10µA per Device CMOS Standby Current
- Typical Endurance >100,000 Cycles
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Range
- Package
 - 80 Pin SIMM (JEDEC)

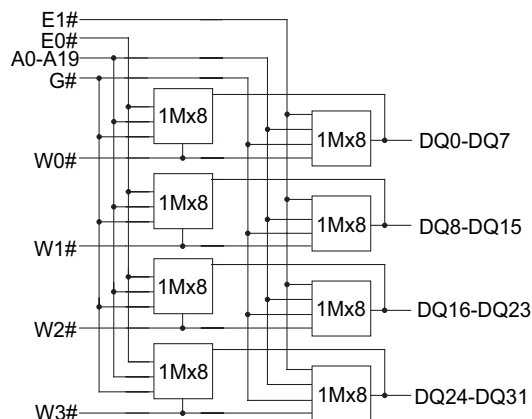
FIG. 1

BLOCK DIAGRAMS

EDI7F331MC-BNC: 1Mx32 80 PIN SIMM



EDI7F2331MC-BNC: 2x1Mx32 80 PIN SIMM



**CAPACITANCE**(f=1.0MHz, $V_{IN} = V_{CC}$ or V_{SS})

		1Meg	2x1Meg	
Parameter	Sym	Max	Max	Unit
Address Lines	CA	35	70	pF
Data lines	CDQ	15	30	pF
Chip & Write Enable Lines	CC	15	30	pF
Output Enable lines	CG	35	70	pF

PIN CONFIGURATIONS

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	V _{SS}	21	*	41	A11	61	DQ9
2	V _{CC}	22	*	42	A10	62	DQ8
3	NC	23	*	43	A9	63	DQ7
4	G#	24	*	44	A8	64	DQ6
5	W0#	25	V _{SS}	45	A7	65	DQ5
6	W1#	26	DQ29	46	A6	66	DQ4
7	NC	27	DQ30	47	A5	67	DQ3
8	DQ16	28	DQ31	48	A4	68	DQ2
9	DQ17	29	W2#	49	A3	69	DQ1
10	DQ18	30	NC	50	A2	70	DQ0
11	DQ19	31	NC	51	A1	71	NC
12	DQ20	32	NC	52	A0	72	V _{CC}
13	DQ21	33	A19	53	W3#	73	PD1
14	DQ22	34	A18	54	V _{SS}	74	PD2
15	DQ23	35	A17	55	DQ15	75	PD3
16	DQ24	36	A16	56	DQ14	76	PD4
17	DQ25	37	A15	57	DQ13	77	PD5
18	DQ26	38	A14	58	DQ12	78	PD6
19	DQ27	39	A13	59	DQ11	79	PD7
20	DQ28	40	A12	60	DQ10	80	V _{SS}

*TBD

SIMM Density

Pin	1Meg	2x1Meg
21	NC	NC
22	NC	NC
23	NC	E1#
24	E0#	E0#

Presence Detect Pin Out

Pin	1Meg	2x1Meg
PD1	NC	V _{SS}
PD2	V _{SS}	V _{SS}
PD3	NC	NC
PD4	V _{SS}	V _{SS}

A0-A19	Address input
E0#, E1#	Chip Enable
W0#-W3#	Write Enable
G#	Output Enable
DQ0-DQ31	Data Input/Output
P _D	Presence Detect
V _{CC}	Power 5V±10%
V _{SS}	Ground
NC	No Connect

