16Kx16 Static RAM CMOS, High Speed Module

The EDH816H16C is a 256K bit high speed CMOS Static RAM module based on four 16Kx4 Static RAMs in leadless chip carriers, mounted on a multilayered ceramic substrate.

The 36 pin vertical dual-in-line package (100 mil centers) provides high density in addition to fast access times of 25, 35, and 45 ns.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

EDI Military Modules are constructed using semiconductor components which have been 100% screened to the test methods of MIL-STD-883C, Class B.

Features

16Kx16 bit CMOS Static Random Access Memory Module

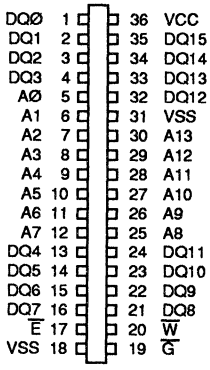
- Access Times 25, 35, and 45ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- 36 Pin Vertical Dual-in-line Package, 100 mil centers

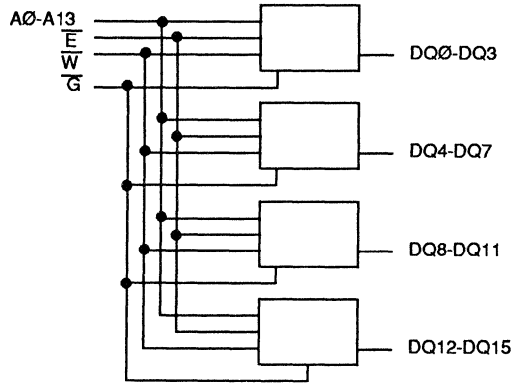
Ideal for:

- Bit Slice Micro Code
- Cache Memory
- Long Word Applications

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A13	Address Inputs
Ē	Chip Enable
W̄	Write Enable
Ḡ	Output Enable
DQØ-DQ15	Data Input/ Data Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.3V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Military ..... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation ..... 2 Watts
Output Current. ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA	--	240	440	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH	--	40	65	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC, $\overline{E}$=VIH	--	--	10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	Output Deselect	HIGH Z	ICC1
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance	CI	50	pF
Input Capacitance Control Lines	CC	35	pF
Output Capacitance	CO	25	pF

These parameters are sampled, not 100% tested.

AC Characteristics

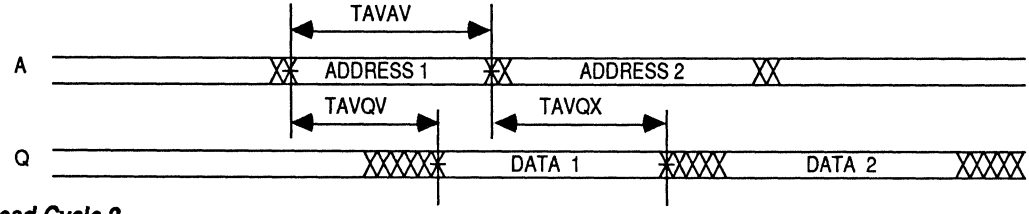
Read Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

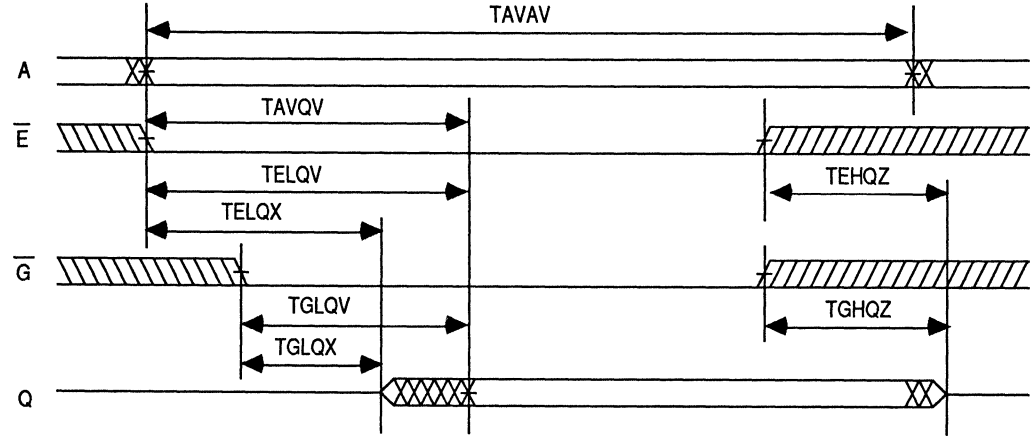
Parameter	Symbol	25ns		35ns		45ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	25		35		45		ns
Address Access Time	TAVQV		25		35		45	ns
Chip Enable Access Time	TELQV		25		35		45	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		ns
Output Enable to Output Valid	TGLQV		15		20		25	ns
Output Enable to Output in Low Z	TGLQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ		10		15		15	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD		25		35		45	ns

Note 1: Parameter guaranteed, but not tested.

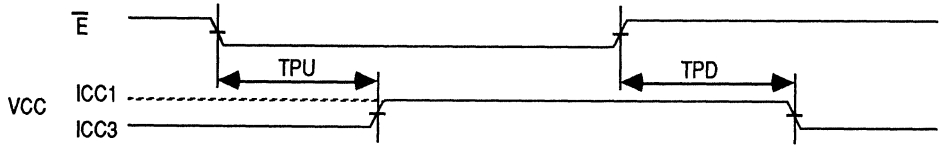
Read Cycle 1
$\overline{W}$ High; G, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



$\overline{E}$ Power Down Function



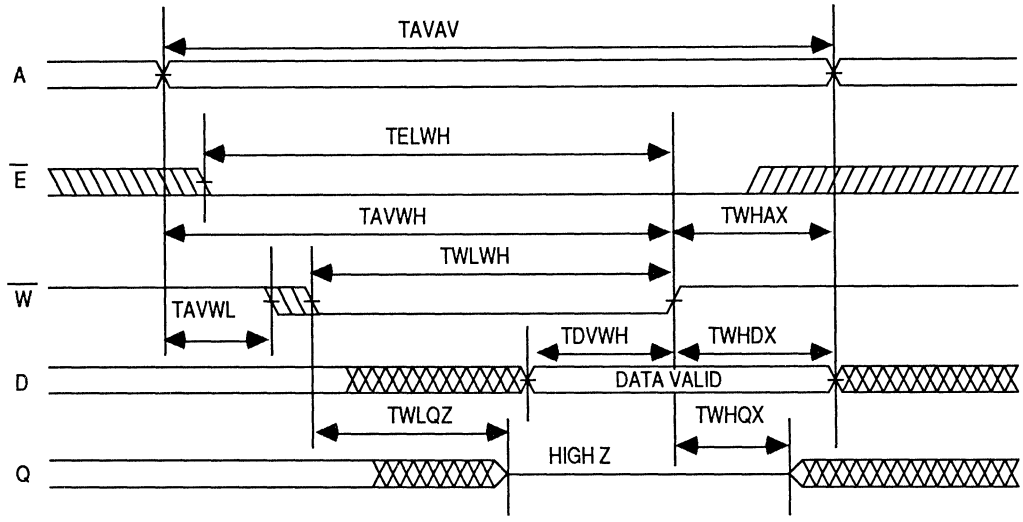
AC Characteristics
Write Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		25ns		35ns		45ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		25		35		45		ns
Chip Enable to	TELWH	$\overline{W}$	20		30		40		ns
End of Write	TWLEH	$\overline{E}$	20		30		40		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	20		25		35		ns
End of Write	TAVEH	$\overline{E}$	20		25		35		ns
Write Pulse Width	TWLWH	$\overline{W}$	20		25		35		ns
	TELEH	$\overline{E}$	20		25		35		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ			10		10		15	ns
Data to Write Time	TDVWH	$\overline{W}$	15		15		20		ns
	TDVEH	$\overline{E}$	15		15		20		ns
Output Active from End of Write (1)	TWHQX		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled