Description

The Edge6435/6436 is a low-cost, 40-channel, monolithic ATE level DAC solution manufactured in a wide-voltage bi-CMOS process.

The Edge6435/6436 features independent buffered voltage and current outputs that are serially programmed and can be used to provide all of the reference levels required for up to 8 channels of pin electronics in an ATE system.

Designated Voltage Output DACs
- Wide Voltage Range (16.75V)
- Adjustable Full-Scale Range
- Adjustable Minimum Offset Voltage
- 13-bit Resolution
- 11-bit Accuracy (E6436)
- 10-bit Accuracy (E6435)

Selectable Voltage/Current Output DACs
- Wide Voltage/Current Range (16.75V/2 mA)
- Adjustable Full-Scale Range
- Adjustable Minimum Offset
- Configurable as either Voltage or Current Output
- 13-bit Resolution
- 11-bit Accuracy (E6436)
- 10-bit Accuracy (E6435)

Designated Current Output DACs
- 1.6 mA Range
- Adjustable Full-Scale Range
- 6-bit Resolution

On-chip, digital storage of offset and gain calibration coefficients allow the E6435/6436 output levels to be programmed using “Ideal Code”, helping to reduce some of the complexity and time normally associated with programming level DACs in ATE systems.

PINCAST allows the Edge6435/6436 to further reduce this complexity and time by allowing channels across multiple Edge6435/6436 devices to be digitally assigned to up to 8 distinct sets that can be addressed and programmed with a limited number of instructions.

The Edge6435/6436 features 2 ranks of input latches into each DAC, whereby all DAC values may be updated at one time.

For Automated Test Equipment, the Edge6435/6436 can support Pin Electronics and Parametric Measurement Units whose outputs are in the range of –3.25V to +13V, and Driver Super Voltages to +13V after calibration. It provides 10 or 5 per pin levels for 4 or 8 channels respectively. The Edge6435/6436 is designed such that DACs may be shared for various levels whereby minimizing the total number of DACs required in a specific application.

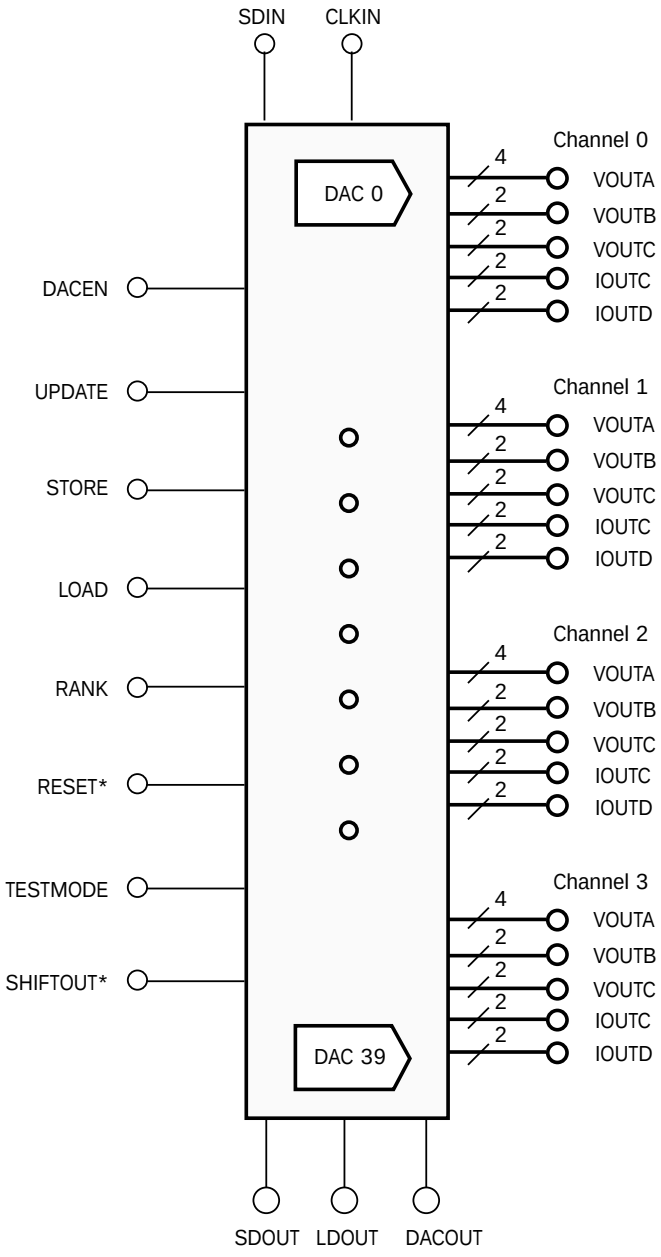
Features

- 40 DACs Partitioned into 4 Groups for 4 or 8 Pin Channels
- Wide Voltage Output Range (16.75V Range)
- 24 Voltage DACs per Package
- 8 Voltage / Current DACs per Package
- 8 Current DACs per Package
- Adjustable Full-Scale Range and Offset per Group
- DUT GND or Analog GND Reference per Group
- Self-Calibrating DACs via Internal Offset, Gain Registers
- Two Offset, Gain Registers to Support Sharing of DACs
- DAC Programming per Channel or Set of Channels
- Readback of DAC Input Data and Output Value
- Small 100-Pin MQFP Package
- Low-Cost, Highly Integrated Multi-DAC Solution

Applications

- Automated Test Equipment (ATE)
- Cost Sensitive applications requiring multiple programmable voltage and currents

Functional Block Diagram



PIN Description

Pin Name	Pin #	Description
Power Supplies		
AVCC	29, 58, 76	Positive Analog Supply Pins (Output Buffer Supply)
AVEE	2, 3, 22, 27, 28, 57, 61, 73, 77	Negative Analog Supply Pins
AVDD	21, 26, 60, 74, 96	Positive Analog Supply Pins (Core DAC Supply)
AGND	20, 25, 59, 75, 99	Analog Supply Ground Pins
DVDD	65, 67	Digital Supply Input Pins
DGND	64, 68	Digital Supply Ground Pins
VREF	4, 63, 69	Reference Voltage Input
Digital I/O Pins		
CLKIN	14	Clock input pin.
SDIN	12	Serial data input pin that is used to read 24-bit words into the E6435 input shift register.
LOAD	15	Digital input pin that triggers the transfer of data from the serial data input shift register to the central DAC register at up to 33 MHz.
STORE	10	Digital input pin that is used to update the rank A latches.
UPDATE	9	Digital input pin that is used to update the rank B latches.
RANK	66	Digital input pin that selects either data in the rank A or rank B latches as the DAC input.
FORMAT	11	Digital input pin used to select between "4-channel" or "8-channel" decoding schemes.
RESET*	7	Digital input pin that is used to initialize the E6435 by placing it into a known state.
DACEN	6	Digital input pin that is used to set all DAC outputs ~0V (Voltage output DACs) or ~0mA (Current output DACs).
SDOUT	17	Serial data output pin.
Diagnostic Pins		
TEST_MODE	16	Digital input pin that is used to enable/disable the DAC_OUT and LD_OUT functions.
DAC_OUT	54	High impedance analog voltage output pin that displays the output level of a selected DAC (used for system level diagnostics) when enabled using the TEST_MODE pin.
SHIFTOUT*	8	Digital input pin that is used to begin the transmission of serial data through the LD_OUT pin.
LD_OUT	13	Serial data output pin used to display the binary value stored in a selected rank A or rank B latch.

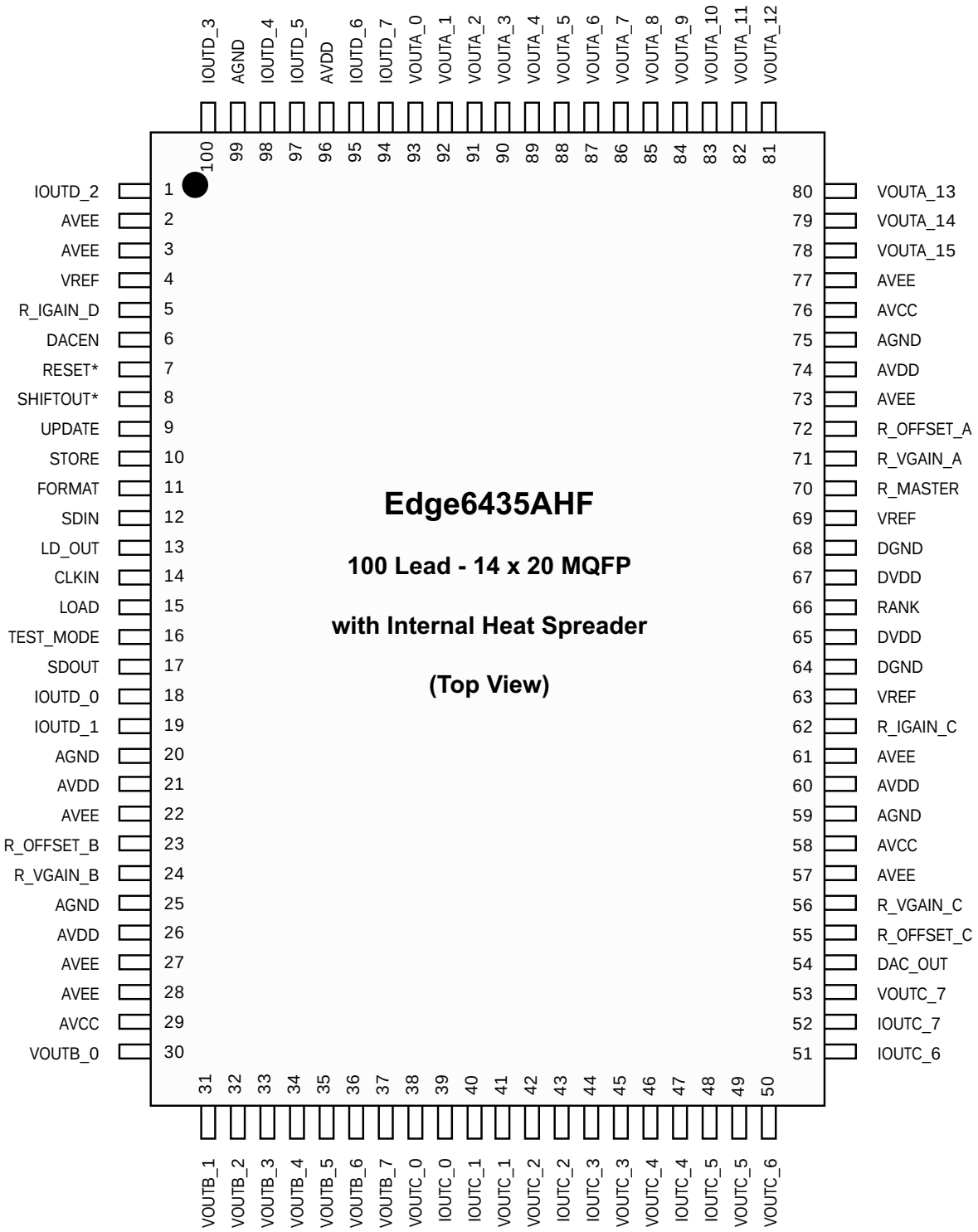
PIN Description *(continued)*

Pin Name	Pin #	Description
13-Bit Voltage Output DACs		
VOUTA_0 VOUTA_1 VOUTA_2 VOUTA_3 VOUTA_4 VOUTA_5 VOUTA_6 VOUTA_7 VOUTA_8 VOUTA_9 VOUTA_10 VOUTA_11 VOUTA_12 VOUTA_13 VOUTA_14 VOUTA_15	93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78	Group A Voltage DAC Output Pins.
VOUTB_0 VOUTB_1 VOUTB_2 VOUTB_3 VOUTB_4 VOUTB_5 VOUTB_6 VOUTB_7	30 31 32 33 34 35 36 37	Group B Voltage DAC Output Pins.
13_Bit Selectable Voltage/Current Output DACs		
VOUTC_0 VOUTC_1 VOUTC_2 VOUTC_3 VOUTC_4 VOUTC_5 VOUTC_6 VOUTC_7	38 41 42 45 46 49 50 53	Group C Voltage DAC Output Pins.
IOUTC_0 IOUTC_1 IOUTC_2 IOUTC_3 IOUTC_4 IOUTC_5 IOUTC_6 IOUTC_7	39 40 43 44 47 48 51 52	Group C Current DAC Output Pins.
6-Bit Current Output DACs		
IOUTD_0 IOUTD_1 IOUTD_2 IOUTD_3 IOUTD_4 IOUTD_5 IOUTD_6 IOUTD_7	18 19 1 100 98 97 95 94	Group D Current DAC Output Pins.

PIN Description *(continued)*

Pin Name	Pin #	Description
Resistor Connections		
R_MASTER	70	External resistor connection used in combination with R_VGAIN_A, R_VGAIN_B, and R_VGAIN_C to set the maximum output range for the Group A, B, and C voltage output DACs.
R_VGAIN_A	71	External Resistor connection used in combination with R_MASTER to set the maximum range for the group A voltage DAC outputs.
R_VGAIN_B	24	External Resistor connection used in combination with R_MASTER to set the maximum range for the group B voltage DAC outputs.
R_VGAIN_C	56	External Resistor connection used in combination with R_MASTER to set the maximum range for the group C voltage DAC outputs.
R_OFFSET_A	72	External resistor connection used to set the base offset voltage for group A voltage DAC outputs.
R_OFFSET_B	23	External resistor connection used to set the base offset voltage for group B voltage DAC outputs.
R_OFFSET_C	55	External resistor connection used to set the base offset voltage for group C voltage DAC outputs.
R_IGAIN_C	62	External resistor connection used to set the maximum range for the group C current DAC outputs.
R_IGAIN_D	5	External resistor connection used to set the maximum range for the group D current DAC outputs.

PIN Description *(continued)*



Chip Overview

The Edge6435/6436 provides 40 output levels. These outputs can easily be configured to generate the specific analog voltage and current requirements for 4 or 8 channels of ATE pin electronics including:

- 3 level driver
- Window comparator
- Active load
- Per pin PMU or PTU

without requiring any scaling or shifting via external components.

Selection of 4 or 8 channel format is via the FORMAT input.

Programming of the chip is done using a 6 wire digital interface comprised of:

- Serial Data In
- Clock In
- Load

Grouping of DACs

DACs are separated into 4 or 8 channels of 4 distinct functional groups. Groups are defined by:

- Type (voltage or current output)
- Resolution (# of bits)
- Output range
- Output compliance.

Table 1 defines the DACs on a per group and channel basis.

Group C DACs have both voltage and current output pins.

Group C DACs can be individually configured via the serial interface to be either a voltage or current DAC (but not both at the same time).

Tables 3 and 4 identify the code needed to configure Group C DACs. Please note that 24 clock cycles are required to load the configuration code for each channel.

Attribute		**Group A**	**Group B**	**Group C**	**Group D**
Total # of DACs in Group	4 CH Format	4 per channel	2 per channel	2 per channel	2 per channel
	8 CH Format	2 per channel	1 per channel	1 per channel	1 per channel
Type		V	V	V/I	I
Resolution (# of bits)		13	13	13	6
Output Range: Max DAC Range (Note 1) Offset Range		16.75V –3.5V to –0.75V	16.75V –3.5V to –0.75V	16.75V –3.5V to –0.75V or 2.05 mA (Note 2)	1.6 mA
Adjustable Output Offset		yes	yes	yes for Vout no for Iout	no
Compliance		±200 µA	±200 µA	±200 µA(V) –0.2 to +3V(I)	–0.2 to +3V

Note 1: The max DAC range is achieved through specific AVCC, AVEE, and Gain resistor settings. See the equations in the "DAC Voltage Output Overview", "DAC Current Output Overview", and specifications for details.

Note 2: Group C has both voltage and current outputs.

Table 1. DAC Grouping

Circuit Description *(continued)*

Voltage Outputs DACs (Groups A, B, C)

The output voltage of each E6435/6436 V_{OUT} DAC is a function of external resistor values (R_MASTER, R_VGAIN and R_OFFSET), a reference voltage level (V_{REF}), contents of digital offset and gain registers, and the programmed input code (DATA). The general equation that describes the output voltage as a function of these variables is presented below as Equation 1:

$$V_{OUT\_[A:C]} = \left(8 * V_{REF} * \frac{R\_VGAIN\_[A:C]}{R\_MASTER} * \frac{CODE}{8192}\right) + V_{OFFSET\_[A:C]}$$

Equation 1.

where:

V_{OUT}[A:C] is the output voltage of a Group A, B, or C Voltage DAC.

V_{REF} is an externally applied 2.5V reference voltage

R_VGAIN[A:C] is the value of an external resistor used to set the range for Group A, B, or C DACs

R_MASTER is the value of an external resistor that sets the bias point/range for the voltage DACs

CODE is the base-10 value of the binary code (DATA) loaded into the DAC shift register (see Figures 4 and 5) after it has been modified by the contents of the digitally programmable offset and gain calibration registers as shown in Figure 2.

$V_{OFFSET[A:C]}$ is the raw DAC offset voltage that is programmed using an external resistor per group, R_OFFSET[A:C] as follows:

$$V_{OFFSET\_[A:C]} = -V_{REF}\left(\frac{R\_OFFSET\_[A:C]}{R\_MASTER}\right)$$

Equation 2.

As can be seen from Equation 1, the accuracy of the DAC output voltage after calibration is dependent upon the temperature coefficients of V_{REF} and the external resistors.

Minimum / Maximum Output Voltages

See Table 2 for the minimum and maximum possible voltages of a voltage output, where:

$V_{OFFSET[A:C]}$ is defined in equation 2, and

$$V_{MAX\_[A:C]} = \left(8 * V_{REF} * \frac{R\_VGAIN\_[A:C]}{R\_MASTER} * \frac{8191}{8192}\right) + V_{OFFSET\_[A:C]}$$

Equation 3.

Resolution

The resolution of the DACs in Groups A, B and C is:

$$V_{RANGE\_[A:C]} / (2^{13} - 1)$$

where $V_{RANGE\_[A:C]}$ is defined in Equation 4.

Range

The range of the DACs in Groups A, B and C is:

$$V_{RANGE\_[A:C]} = 8 * V_{REF} * \frac{R\_VGAIN\_[A:C]}{R\_MASTER} * \frac{8191}{8192}$$

Equation 4.

External Resistors

Typically computed for R_MASTER = 100kΩ.

DAC Setting MSB ... LSB	$V_{OUT\_[A:C]}$ (V)
0000H	$V_{OFFSET\_[A:C]}$
1FFFH	$V_{MAX\_[A:C]}$

Table 2. Minimum/Maximum Output Voltages

Circuit Description *(continued)*

Current Output DACs (Groups C, D)

Group C DACs

The output current of each Group C Current DAC is a function of an external resistor value (R_IGAIN_C), a reference voltage level (V_{REF}), contents of digital offset and gain registers, and the input code (DATA). The general equation that describes the output current as a function of these variables is presented below as Equation 5:

$$I_{OUT\_C} = \frac{CODE}{8192} * \frac{50 \times V_{REF}}{R\_IGAIN\_C}$$

Equation 5.

where:

I_{OUT_C} is the output current of the Group C Current DAC

V_{REF} is an externally applied 2.5V reference voltage

R_IGAIN_C is the value of an external resistor that sets the output current range for Group C DACs ($60.97K\Omega \leq$ R_IGAIN_C $\leq 250K\Omega$)

CODE is the base-10 value of the binary code (DATA) loaded into the DAC shift register (see Figures 4 and 5) after it has been modified by the contents of the digitally programmable offset and gain calibraiotn registers as shown in Figure 2.

Group D DACs

The output current of each group D DAC is a function of an external resistor value (R_IGAIN_D), a reference voltage level (V_{REF}) and the input code (DATA). The general equation that describes the output current as a function of these variables is presented below as Equation 6:

$$I_{OUT\_D} = \frac{DATA}{64} * \frac{50 \times V_{REF}}{R\_IGAIN\_D}$$

Equation 6.

where:

I_{OUT_D} is the output current of the Group D DAC

V_{REF} is an externally applied 2.5V reference voltage

R_IGAIN_D is the value of an external resistor that sets the output current range for Group D DACs ($78.12K\Omega \leq$ R_IGAIN_D $\leq 156.25K\Omega$)

DATA is the base-10 value of the binary code loaded into the DAC shift register (see Figures 4 and 5).

Functional Description

Figure 1 provides a Functional Block Diagram. Figures 2 and 3 show details of the data latches and logic for the DACs. The Edge6435/6436 features a serial data input to program a channel or set of channel's DACs and functions. The Edge6435/6436 also features self-calibrating DAC outputs via internal offset and gain registers (Figure 2).

Figures 4 and 5 show the format of the Serial Input Data for 4 pin channel and 8 pin channel formats.

Figure 6 shows the Serial Data Programming Sequence

Tables 3 and 4 provide the Address Maps for 4 pin channel and 8 pin channel formats.

FORMAT

FORMAT Low selects the 4 pin channel format.
FORMAT High selects the 8 pin channel format.

Circuit Description *(continued)*

RESET*

RESET* low resets the input shift register (no CLKIN required), the central register, and input registers. With RESET* high, the following leading edge of CLKIN will cause reset condition to be removed (see Figure 21). Two clock cycles are required after RESET* is set to logic "high" for the DAC outputs to be enabled.

Programming Sequence

The DACs are programmed serially (see Figures 1 and 6). On each rising edge of CLKIN, SDIN is loaded into a shift register. It requires 24 Clocks to fully load the shift register.

LOAD

Following the serial input of a new DAC value, then LOAD high for the leading edge of CLKIN loads the new DAC value and its address into the Central Register. Following the loading of the Central Register, LOAD needs to go low followed by a leading edge of CLKIN so as to enable the address decoder (see Figure 6).

STORE

Following the LOAD of the Central Register and the enabling of the address docoder, the channel or set of channels addressed DACs input register or channel function is "stored" by a CLKIN with STORE high. Only upon the STORE of a DAC or set of DAC's "value latch" (Figure 2) does the Edge6435/6436 compute the input to DAC's Latch A (of Rank A). There needs to be at least one clock edge after LOAD is set to logic "low" before STORE is set to logic "high" (see Figure 21).

UPDATE

Following the STORE of multiple DAC values into Rank A DAC latches, Rank B latches may be updated in parallel with the values of their Rank A DAC latches by a CLKIN with UPDATE high. There must be at least 16 clock cycles between when STORE is set to logic "low" and UPDATE is latched to logic "high" in order to latch the latest data (see Figure 21).

RANK Selection

Referring to Figures 1, 2 and 3:

RANK low selects Rank A latches to the DACs (no CLKIN required).

RANK high selects Rank B latches to the DACs (no CLKIN required).

DACEN

DACEN low forces all DAC voltage outputs to ~0V and all current outputs to ~0 mA (no CLKIN required). With DACEN high, then a following leading edge of CLKIN will cause DACs to be enabled (see Figure 23).

TEST MODE/SHIFTOUT*

TEST_MODE is used to enable the LDOUT and DACOUT channels. Once enabled (TESTMODE = 1), SHIFTOUT* can be used to begin transmission of serial data through the LDOUT pin, or DAC outputs can be monitored at the DACOUT pin (see Figure 24) (TEST_MODE functionality does not depend on CLKIN)).

When addressing DAC channels that have been assigned to a PinCast "set", TEST-MODE is internally disabled in order to prevent multiple DAC outputs from being connected in parallel and possibly damaging the E6435/6436.

Circuit Description *(continued)*

Serial Programming

The Edge6435/6436 is programmed with 24-bit serial data (Figure 6) in either a 4 channel (Figure 4) or 8 Channel (Figure 5) format.

Following the input of serial data, it is loaded into a central register by LOAD (Figure 1). The central register's contents are stored in the "addressed" latch by the STORE input. Tables 3 and 4 show the "Address Maps" for the 4 and 8 channel formats.

Referring to Table 3 for 4 channel format, a channel's DACs Set Register or Function may be addressed and the "stored" value changed. For each DAC, there are associated multiple latches (Figures 2 and 3). For the 13-bit DACs (Figure 2) the DAC's output is a function of the contents of its value, gain and offset latches. The Edge6435/6436 features two gain and offset latches per DAC whereby a DAC's output may be shared. For example, in ATE a DAC's value may be shared between a pin driver's high level and a pin's parametric unit's high limit level, where each application requires different offset and gain factors to calibrate each path correctly. Gains and offsets are computed externally to the Edge6435/6436 in the process of pin channel level calibration in the ATE. Gains and offsets are stored in the Edge6435/6436 in the same manner as other latches. Selection of what is stored is determined by the "register selection" bits in the 24-bit input data (Figures 2 and 4). Upon storing a 13-bit DAC's Value, the resultant DAC's $\frac{(\text{Value} \times \text{Gain})}{4096}$ + Offset + Value) is updated by UPDATEA (Figure 2) into the DAC's output latch of RANKA. The contents of all RANKA latches may be transferred to RANKB latches, in parallel, across multiple Edge6435/6436's by the UPDATE input into the Edge6435/6436. The RANK input into the Edge6435/6436 selects either RANKA or RANKB latches for all DACs.

For the 6-bit DACs (Figure 3) the DAC's output is selected from four "value latches".

Referring to Table 3, a channels Set Register may also be programmed. This is an independent 8-bit register per channel which determines the "sets" to which the channel belongs. Figure 7 shows details of programming a channel's Set Register, which is stored in the Edge6435/6436 by the STORE input. A channel may belong to none, one, or any combination of up to 8 distinct sets. The address maps show that a channel's DAC (or Function) may be addressed individually, or a DAC (or Function) of multiple channels belonging to the same set may be programmed in parallel. Figure 11 shows an example of addressing channels by sets.

Referring to Table 3, a Channel's function is programmed as indicated in Figure 9 (offset and gain selection as well as Group C DAC V/I output selection, see below).

Channel's Functions (for 13 bit DACs only), with R2 = R1 = R0 = 0, then:

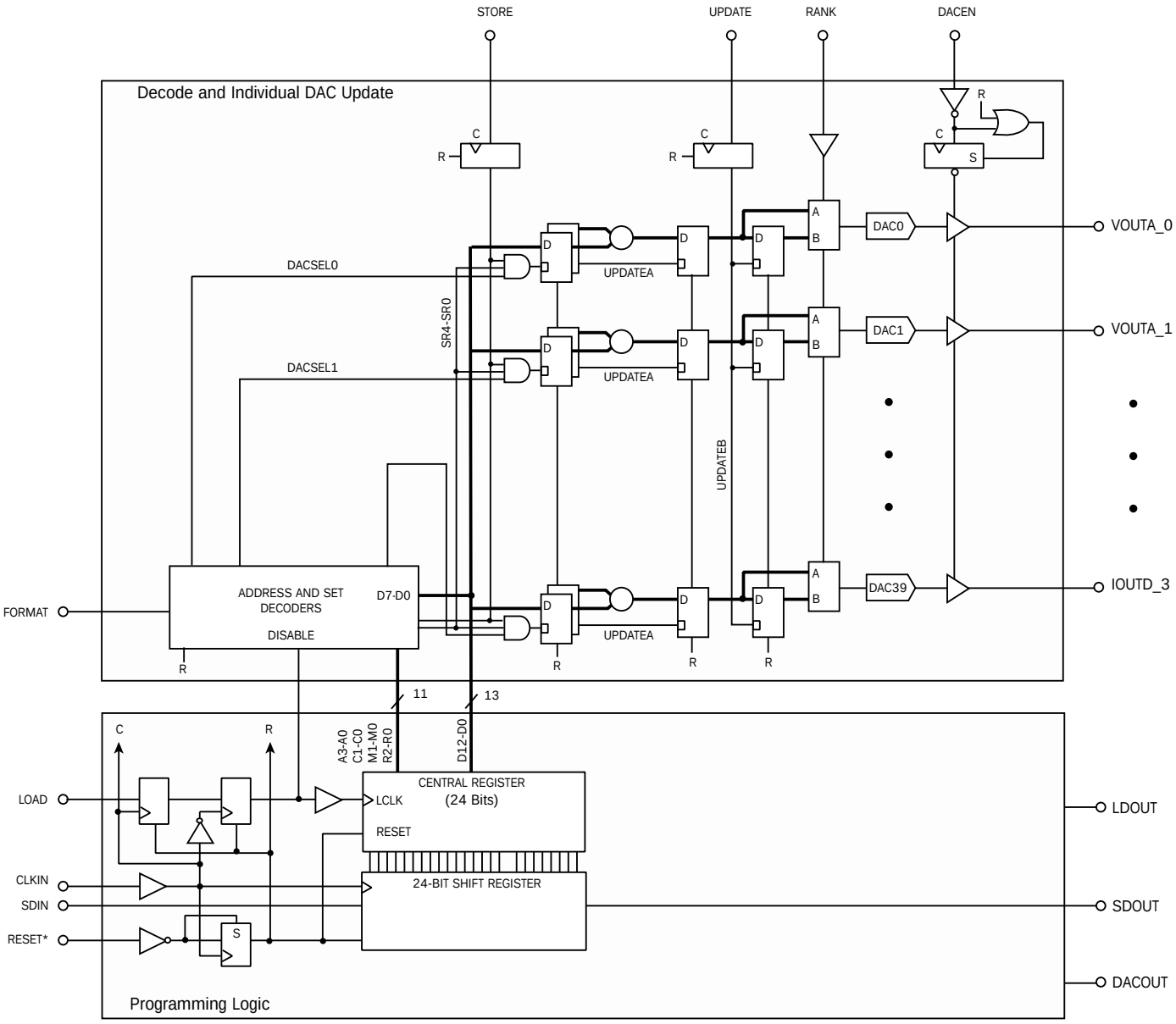
D0 = 0: Selects 1st Offset/Gain Registers
D0 = 1: Selects 2nd Offset/Gain Registers
D1 = 0: Selects Voltage Output on Group C DACs
D1 = 1: Selects Current Output on Group C DACs

Referring to Table 4 for 8 channel format, and Figures 2, 3, 5, 8 and 10, a channel's DACs, Set Registers and Function, etc. are programmed and operate similar to the 4 channel format described above.

NOTE: The STORE of a DAC's offset or gain does not result in a DAC output change. Only upon the STORE of a DAC or set of DAC's "value" does the Edge6435/6436 compute the input to DAC's "A" latches.

In a tester having multiple Edge6435/6436s, DACs or channel functions may be programmed individually or as a set (1 of 8) of channels across all channels. If multiple E6435/6436s are programmed in parallel, individual DAC or Function programming requires the STORE input to the associated Edge6435/6436 to be applied where all STORE inputs to other Edge6435/6436s are to be inhibited (externally). Programming a DAC or Function of a Set of Channels requires STORE input to be applied to all Edge6435/6436s. Edge6435/6436's DACs may be "updated" in parallel following the programming of DACs as individual DACs or sets of DACs.

Circuit Description *(continued)*

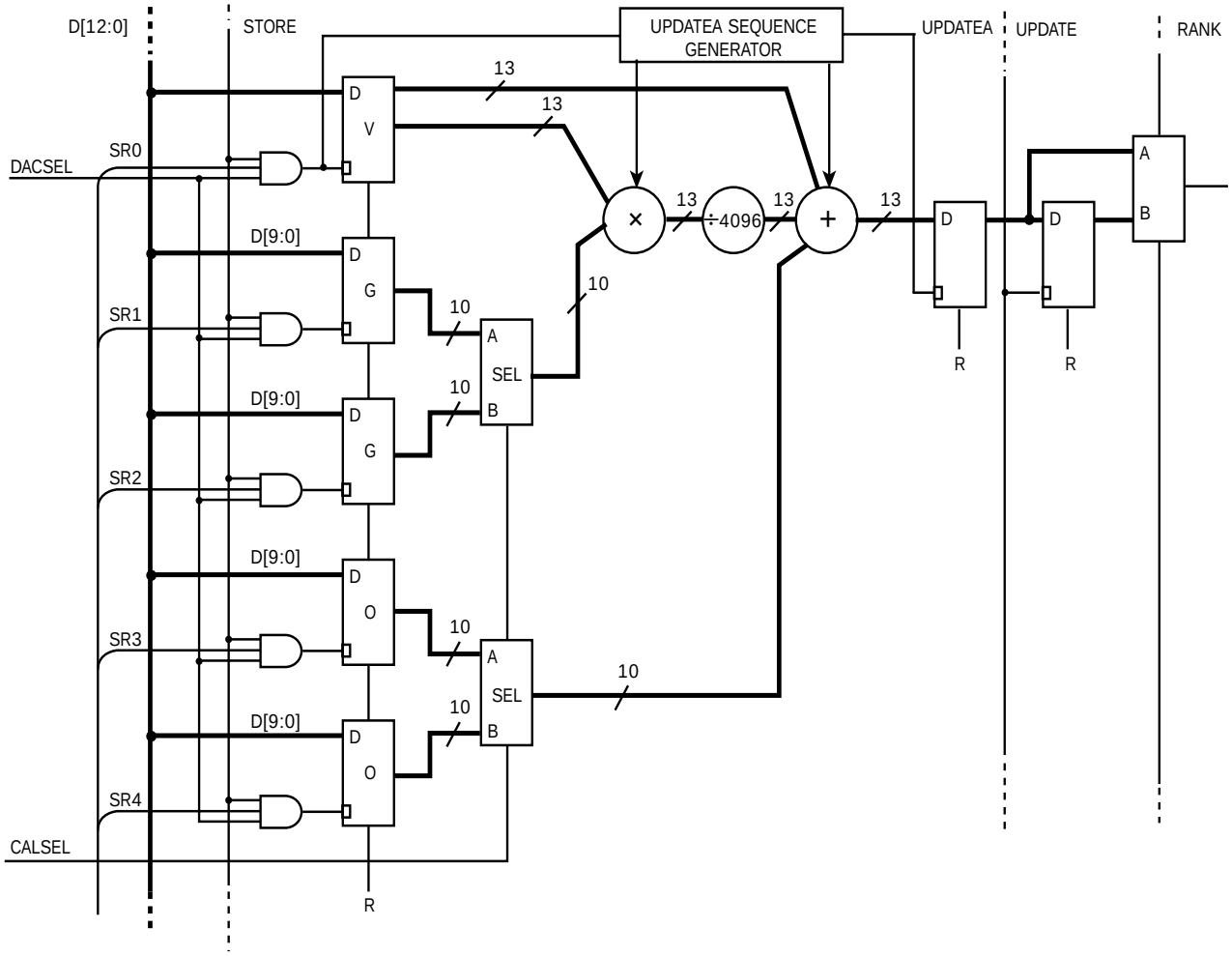


NOTE: VOUT, IOUT names shown for 4 Channel Format.

NOTE: Not shown is the function of the Latched Data Readback (via LDOUT) and the DAC Value Readback (via DACOUT). Details of the 'Store' Latches are shown on the following pages.

Figure 1. DAC Functional Block Diagram

Circuit Description *(continued)*



KEY:
V: Value Latch that contains DATA programmed to a DAC (see Figures 4 & 5).

O: Offset Latches that are used to store offset calibration coefficients (two offset latches per DAC allow the DAC to be shared in a system).

G: Gain Latches that are used to store gain calibration coefficients (two gain latches per DAC allow the DAC to be shared in a system).

NOTE: CALSEL common to all DACs assigned to a Channel

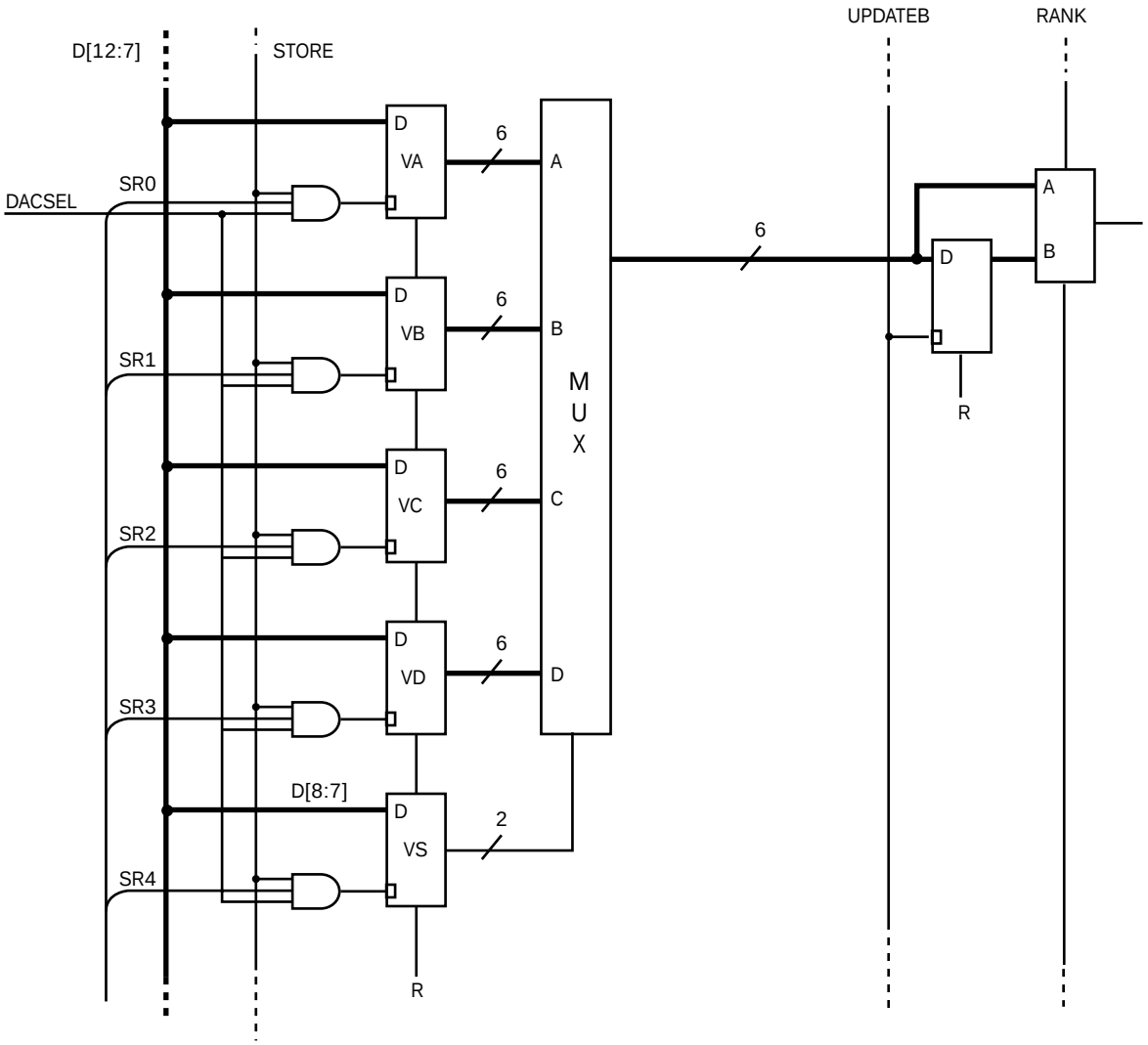
DAC Output (CODE):

$$CODE = \frac{V * (G + 4096)}{4096} + O$$

Function	Register Selection			
	R2	R1	R0	Select
DAC Data	0	0	0	SR0
Gain Register A	0	0	1	SR1
Gain Register B	0	1	0	SR2
Offset Register A	0	1	1	SR3
Offset Register B	1	0	0	SR4

Figure 2. Details of DAC Data Latches for 13 Bit DACs (Groups A, B, and C)

Circuit Description *(continued)*



KEY:
VA, VB, VC, VD: Value Latches A, B, C, D
VS: Value Selection Latch

Value Selection (VS)		
D8	**D7**	**Select**
0	0	A
0	1	B
1	0	C
1	1	D

Figure 3. Details of DAC Data Latches for 6 Bit DACs (Group D)

Circuit Description *(continued)*

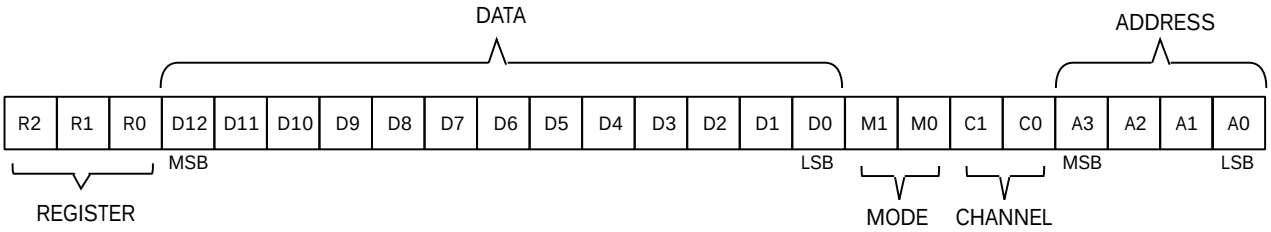


Figure 4. Format of Address and Data in Shift Register (4 Channel Format)

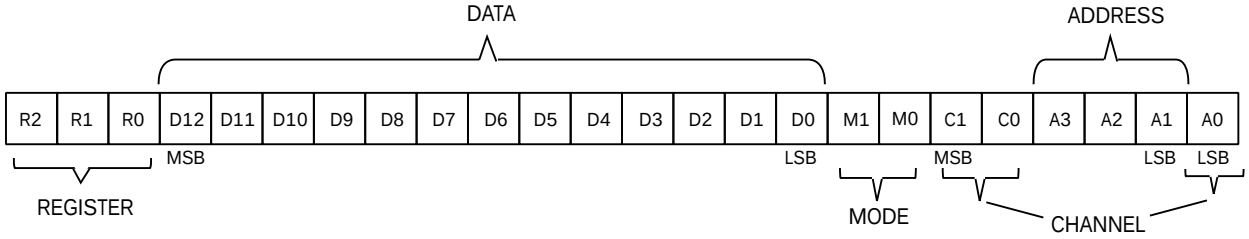


Figure 5. Format of Address and Data in Shift Register (8 Channel Format)

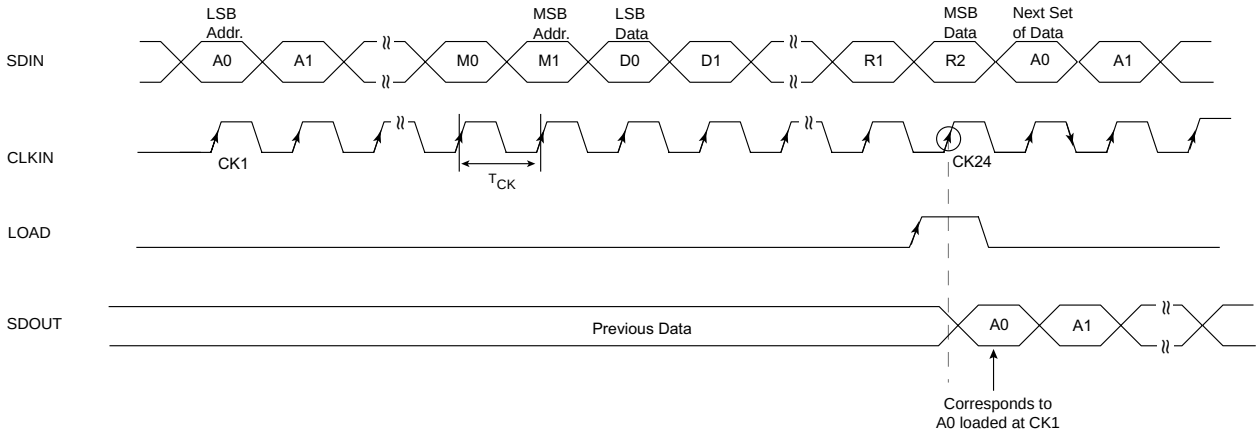


Figure 6. Serial Data Programming Sequence

Circuit Description *(continued)*

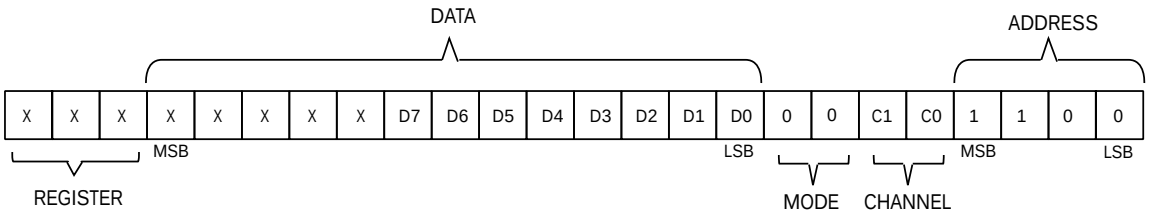


Figure 7. Format of Address and Data for Programming to SET REGISTER (4 Channel Format)

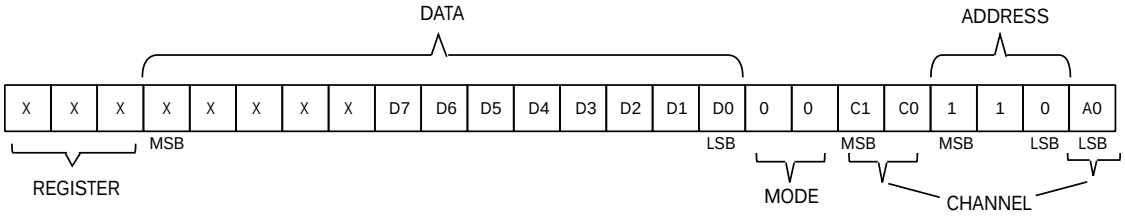


Figure 8. Format of Address and Data for Programming to SET REGISTER (8 Channel Format)

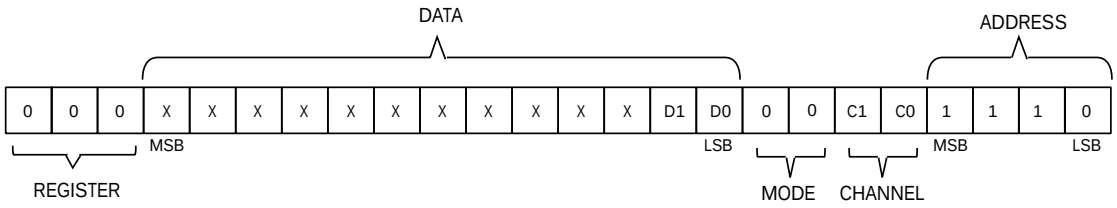


Figure 9. Format of Address and Data for Programming a Channel's Function (4 Channel Format)

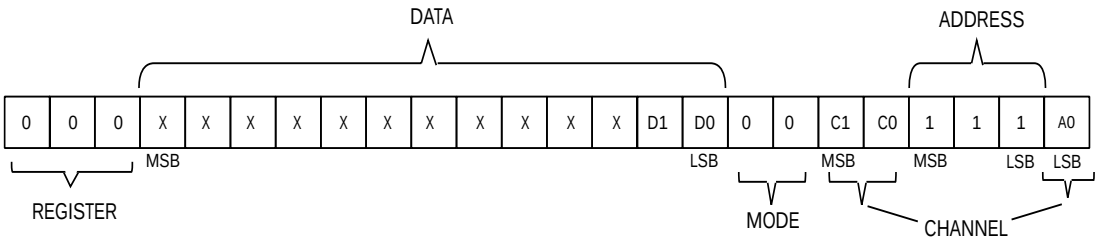
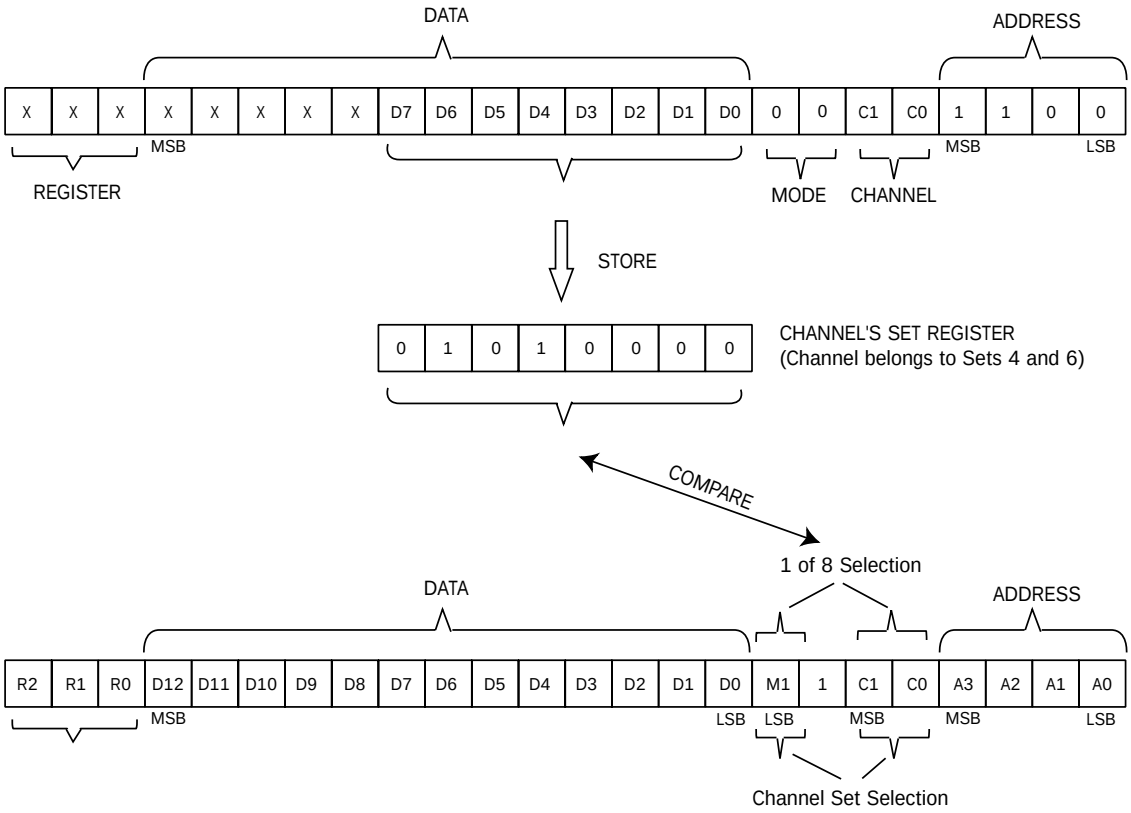


Figure 10. Format of Address and Data for Programming a Channel's Function (8 Channel Format)

Circuit Description *(continued)*



If Set 4 is selected, then channel's DAC value or Function will be 'stored'. If Set 3 is selected, then the channel will not be 'addressed'.

Figure 11. Example of Channel's Set Selection (4 Channel Format)

Circuit Description *(continued)*

FORMAT = 0		Bit #		23	22	21	20	19-16	15-12	11	10	9	8	7	6	5	4	3	2	1	0	
		Hex Multiplier		0x10 0000				0x01 0000	0x1000	0x0100												
		Binary Position		8	4	2	1	8 - 1	8 - 1	8	4	2	1	8	4	2	1	8	4	2	1	
		Item	DAC Output Pin Name	Register				Data														
				R2	R1	R0	D12	D11 - D8	D7 - D4	D3	D2	D1	D0	M1	M0	C1	C0	A3	A2	A1	A0	
CHANNEL FUNCTIONS	CHANNEL 0	Group A 13-bit V	VOUTA_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	
			VOUTA_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	1	
			VOUTA_2	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	1	0	
			VOUTA_3	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0					N/A
		Group B 13-bit V	VOUTB_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	1	0	
			VOUTB_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	1	1	
		Group C 13-bit V/I	VOUTC_0, IOUTC_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	0	0	
			VOUTC_1, IOUTC_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	0	1	
		Group D 6-bit I (Note 1)	IOUTD_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	1	0	
			IOUTD_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	1	1	
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	0	N/A
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	1	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	0	0	1	1	1	0	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	0	0	1	1	1	0	
		Configure Group C DACs as Vout		0	0	0	X	X	X	X	X	0	X	0	0	0	0	1	1	1	0	
		Configure Group C DACs as Iout		0	0	0	X	X	X	X	X	1	X	0	0	0	0	1	1	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1	N/A
	CHANNEL 1	Group A 13-bit V	VOUTA_4	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	0	0	
			VOUTA_5	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	0	1	
			VOUTA_6	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	1	0	
			VOUTA_7	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1					N/A
		Group B 13-bit V	VOUTB_2	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	1	1	0	
			VOUTB_3	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	1	1	1	
		Group C 13-bit V/I	VOUTC_2, IOUTC_2	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	0	0	
			VOUTC_3, IOUTC_3	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	0	1	
		Group D 6-bit I (Note 1)	IOUTD_2	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	0	
			IOUTD_3	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	
		PINCAST Register 1	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	1	0	0	N/A
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	1	0	1	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	0	1	1	1	1	0	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	0	1	1	1	1	0	
		Configure Group C DACs as Vout		0	0	0	X	X	X	X	X	0	X	0	0	0	1	1	1	1	0	
		Configure Group C DACs as Iout		0	0	0	X	X	X	X	X	1	X	0	0	0	1	1	1	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	1	1	1	N/A
	CHANNEL 2	Group A 13-bit V	VOUTA_8	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	0	0	
			VOUTA_9	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	0	1	
			VOUTA_10	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	1	0	
			VOUTA_11	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0					N/A
		Group B 13-bit V	VOUTB_4	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	1	1	0	
			VOUTB_5	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	1	1	1	
		Group C 13-bit V/I	VOUTC_4, IOUTC_4	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	0	0	
			VOUTC_5, IOUTC_5	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	0	1	
		Group D 6-bit I (Note 1)	IOUTD_4	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	1	0	
			IOUTD_5	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	1	1	
		PINCAST Register 2	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	N/A
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	1	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	1	0	1	1	0	1	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	1	0	1	1	0	1	
		Configure Group C DACs as Vout		0	0	0	X	X	X	X	X	0	X	0	0	1	0	1	1	0	1	
		Configure Group C DACs as Iout		0	0	0	X	X	X	X	X	1	X	0	0	1	0	1	1	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	1	1	N/A
	CHANNEL 3		VOUTA_12	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	0	0	
			VOUTA_13	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	0	1	
			VOUTA_14	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	1	0	
			VOUTA_15	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1					N/A
			VOUTB_6	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	1	1	0	
			VOUTB_7	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	1	1	1	
			VOUTC_6, IOUTC_6	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	0	0	
			VOUTC_7, IOUTC_7	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	0	1	
		Group D 6-bit I (Note 1)	IOUTD_6	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	1	0	
			IOUTD_7	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	1	1	
		PINCAST Register 3	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	1	0	0	N/A
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	1	0	1	N/A
		Select Rank 1 Calibration Registers		0	0	0	X	X	X	X	X	X	0	0	0	1	1	1	1	0	1	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	1	1	1	1	0	1	
		Configure Group C DACs as Vout		0	0	0	X	X	X	X	X	0	X	0	0	1	1	1	1	0	1	
		Configure Group C DACs as Iout		0	0	0	X	X	X	X	X	1	X	0	0	1	1	1	1	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	1	1	1	N/A

(continued next page)

Note 1: All 6-bit DACs are programmed with the MSB at the D12 bit position and extending down to D7 for the LSB. D[6:0] bit positions are “don’t cares”.

Table 3. Address Map (4 Channel Format)

Circuit Description *(continued)*

FORMAT = 0		Bit #		23	22	21	20	19-16	15-12	11	10	9	8	7	6	5	4	3	2	1	0
		Hex Multiplier		0x10		0000		0x01	0000	0x1000		0x0100		0x0010							
		Binary Position		8	4	2	1	8 - 1		8 - 1		8	4	2	1	8	4	2	1	8	4	2	1
		Item	DAC Output Pin Name	Register				Data						Mode				Address			
				R2	R1	R0	D12	D11 - D8	D7 - D4	D3	D2	D1	D0	M1	M0	C1	C0	A3	A2	A1	A0
PINCAST SET FUNCTIONS	All DACs	Parallel Load of All DACs	All DAC Output Pins	X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	0
	GROUP A DACs	Parallel Load of denoted VOUTA DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTA_0 VOUTA_4 VOUTA_8 VOUTA_12	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	0	0	0
		Parallel Load of denoted VOUTA DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTA_1 VOUTA_5 VOUTA_9 VOUTA_13	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	0	0	1
		Parallel Load of denoted VOUTA DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTA_2 VOUTA_6 VOUTA_10 VOUTA_14	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	0	1	0
		Parallel Load of denoted VOUTA DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTA_3 VOUTA_7 VOUTA_11 VOUTA_15	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	0	1	1
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	X	X	X	X				
	GROUP B DACs	Parallel Load of denoted VOUTB DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTB_0 VOUTB_2 VOUTB_4 VOUTB_6	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	1	1	0
		Parallel Load of denoted VOUTB DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTB_1 VOUTB_3 VOUTB_5 VOUTB_7	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	1	1	1
	GROUP C DACs	Parallel Load of denoted VOUTC or IOUTC DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTC_0 VOUTC_2 VOUTC_4 VOUTC_6 or IOUTC_0 IOUTC_2 IOUTC_4 IOUTC_6	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	1	0	0	0
		Parallel Load of denoted VOUTC or IOUTC DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTC_1 VOUTC_3 VOUTC_5 VOUTC_7 or IOUTC_1 IOUTC_3 IOUTC_5 IOUTC_7	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	1	0	0	1
	GROUP D DACs	Parallel Load of denoted IOUTD DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	IOUTD_0 IOUTD_2 IOUTD_4 IOUTD_6	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	1	0	1	0
		Parallel Load of denoted IOUTD DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	IOUTD_1 IOUTD_3 IOUTD_5 IOUTD_7	X	X	X	X	X	X	X	X	X	X	PS0	1	PS2	PS1	1	0	1	1
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	X	X	X	X				

Table 3. Address Map (4 Channel Format) – cont'd

Circuit Description *(continued)*

FORMAT = 1		Bit #		23	22	21	20	19-16	15-12	11	10	9	8	7	6	5	4	3	2	1	0	
		Hex Multiplier		0x10 0000				0x01 0000	0x1000	0x0100												
		Binary Position		8	4	2	1	8 - 1	8 - 1	8	4	2	1	8	4	2	1	8	4	2	1	
		Item	DAC Output Pin Name	Register			Data															
				R2	R1	R0	D12	D11 - D8	D7 - D4	D3	D2	D1	D0	M1	M0	C1	C0	A3	A2	A1	A0	
CHANNEL FUNCTIONS (Channels 0 to 3)	CHANNEL 0	Group A 13-bit V	VOUTA_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	
			VOUTA_2	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	1	0	-3.5V to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_0, IOUTC_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	0	0	**V:** -3.5V to +13.75V (16.75V Max Swing) **I:** 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_0	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	1	0	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	0	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	0	0	1	1	1	0	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	0	0	1	1	1	0	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	0	0	1	1	1	0	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	0	0	1	1	1	0	
	CHANNEL 1	Group A 13-bit V	VOUTA_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	1	
			VOUTA_3	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	1	1	-3.5V to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_1, IOUTC_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	0	1	**V:** -3.5V to +13.75V (16.75V Max Swing) **I:** 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	1	1	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	1	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	0	0	1	1	1	1	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	0	0	1	1	1	1	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	0	0	1	1	1	1	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	0	0	1	1	1	1	
	CHANNEL 2	Group A 13-bit V	VOUTA_4	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	0	0	-3.5V to +13.75V (16.75V Max Swing)
			VOUTA_6	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_2	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	1	1	0	-3.5V to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_2, IOUTC_2	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	0	0	**V:** -3.5V to +13.75V (16.75V Max Swing) **I:** 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_02	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	0	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	1	0	0	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	0	1	1	1	1	0	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	0	1	1	1	1	0	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	0	1	1	1	1	0	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	0	1	1	1	1	0	
	CHANNEL 3	Group A 13-bit V	VOUTA_5	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	0	1	
			VOUTA_7	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_3	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0	1	1	1	-3.5V to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_3, IOUTC_3	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	0	1	**V:** -3.5V to +13.75V (16.75V Max Swing) **I:** 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_3	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	1	0	1	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	0	1	1	1	1	1	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	0	1	1	1	1	1	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	0	1	1	1	1	1	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	0	1	1	1	1	1	

(continued next page)

Note 1: All 6-bit DACs are programmed with the MSB at the D12 bit position and extending down to D7 for the LSB. D[6:0] bit positions are “don’t cares”.

Table 4. Address Map (8 Channel Format)

Circuit Description *(continued)*

FORMAT = 1		Bit #		23	22	21	20	19-16	15-12	11	10	9	8	7	6	5	4	3	2	1	0	
		Hex Multiplier		0x10 0000				0x01 0000	0x1000	0x0100												
		Binary Position		8	4	2	1	8 - 1	8 - 1	8	4	2	1	8	4	2	1	8	4	2	1	
		Item	DAC Output Pin Name	Register				Data														
				R2	R1	R0		D12 D11 - D8	D7 - D4	D3	D2	D1	D0	M1	M0	C1	C0	A3	A2	A1	A0	
CHANNEL FUNCTIONS (Channels 4 to 7)	CHANNEL 4	Group A 13-bit V	VOUTA_8	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	0	0	
			VOUTA_10	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_4	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	1	1	0	-3.5 to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_4, IOUTC_4	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	0	0	**V**: -3.5 to +13.75V (16.75V Max Swing) **I**: 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_4	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	1	0	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	1	0	1	1	1	0	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	1	0	1	1	1	0	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	1	0	1	1	1	0	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	1	0	1	1	1	0	
	CHANNEL 5	Group A 13-bit V	VOUTA_9	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	0	1	
			VOUTA_11	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_5	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	1	1	1	-3.5 to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_5, IOUTC_5	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	0	1	**V**: -3.5 to +13.75V (16.75V Max Swing) **I**: 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_5	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	0	1	1	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	1	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	1	0	1	1	1	1	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	1	0	1	1	1	1	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	1	0	1	1	1	1	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	1	0	1	1	1	1	
	CHANNEL 6	Group A 13-bit V	VOUTA_12	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	0	0	-3.5 to +13.75V (16.75V Max Swing)
			VOUTA_14	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	1	0	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_6	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	1	1	0	-3.5 to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_6, IOUTC_6	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	0	0	**V**: -3.5 to +13.75V (16.75V Max Swing) **I**: 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_6	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	1	0	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	1	0	0	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	1	1	1	1	1	0	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	1	1	1	1	1	0	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	1	1	1	1	1	0	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	1	1	1	1	1	0	
	CHANNEL 7	Group A 13-bit V	VOUTA_13	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	0	1	
			VOUTA_15	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	1	1	
		Reserved	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	1	0	0	N/A
		Group B 13-bit V	VOUTB_7	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	1	1	1	-3.5 to +13.75V (16.75V Max Swing)
		Group C 13-bit V/I	VOUTC_7, IOUTC_7	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	0	1	**V**: -3.5 to +13.75V (16.75V Max Swing) **I**: 0.5mA to 2.05mA
		Group D 6-bit I (Note 1)	IOUTD_7	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	0	1	1	0.8mA to 1.6mA
		PINCAST Register 0	N/A	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	1	0	1	N/A
		Select Rank 1 Calibration Registers	N/A	0	0	0	X	X	X	X	X	X	0	0	0	1	1	1	1	1	1	
		Select Rank 2 Calibration Registers		0	0	0	X	X	X	X	X	X	1	0	0	1	1	1	1	1	1	
		Configure Group C DAC as Vout		0	0	0	X	X	X	X	X	0	X	0	0	1	1	1	1	1	1	
		Configure Group C DAC as Iout		0	0	0	X	X	X	X	X	1	X	0	0	1	1	1	1	1	1	

(continued next page)

Note 1: All 6-bit DACs are programmed with the MSB at the D12 bit position and extending down to D7 for the LSB. D[6:0] bit positions are “don’t cares”.

Table 4. Address Map (8 Channel Format) – cont’d

FORMAT = 1		Bit #		23	22	21	20	19-16	15-12	11	10	9	8	7	6	5	4	3	2	1	0
		Hex Multiplier		0x10 0000				0x01 0000	0x1000	0x0100											
		Binary Position		8	4	2	1	8 - 1	8 - 1	8	4	2	1	8	4	2	1	8	4	2	1
		Item	DAC Output Pin Name	Register				Data													
				R2	R1	R0		D12	D11 - D8	D7 - D4	D3	D2	D1	D0	M1	M0	C1	C0	A3	A2	A1	A0
PINCAST SET FUNCTIONS	All DACs	Parallel Load of All DACs	All DAC Output Pins	X	X	X		X	X	X	X	X	X	X	1	0	0	0	0	0	0	X
	GROUP A DACs	Parallel Load of denoted VOUTA DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTA_0 VOUTA_1 VOUTA_4 VOUTA_5 VOUTA_8 VOUTA_9 VOUTA_12 VOUTA_13	X	X	X		X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	0	0	X
		Parallel Load of denoted VOUTA DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTA_2 VOUTA_3 VOUTA_6 VOUTA_7 VOUTA_10 VOUTA_11 VOUTA_14 VOUTA_15	X	X	X		X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	0	1	X
	GROUP B DACs	Parallel Load of denoted VOUTB DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB) across multiple E6435 devices.	VOUTB_0 VOUTB_1 VOUTB_2 VOUTB_3 VOUTB_4 VOUTB_5 VOUTB_6 VOUTB_7	X	X	X		X	X	X	X	X	X	X	PS0	1	PS2	PS1	0	1	1	X
	GROUP C DACs	Parallel Load of denoted VOUTC or IOUTC DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	VOUTC_0 VOUTC_1 VOUTC_2 VOUTC_3 VOUTC_4 VOUTC_5 VOUTC_6 VOUTC_7 or IOUTC_0 IOUTC_1 IOUTC_2 IOUTC_3 IOUTC_4 IOUTC_5 IOUTC_6 IOUTC_7	X	X	X		X	X	X	X	X	X	X	PS0	1	PS2	PS1	1	0	0	X
	GROUP D DACs	Parallel Load of denoted IOUTD DACs assigned to the PINCAST "Set" addressed using the PS2, PS1, PS0 bits (PS0 is LSB).	IOUTD_0 IOUTD_1 IOUTD_2 IOUTD_3 IOUTD_4 IOUTD_5 IOUTD_6 IOUTD_7	X	X	X		X	X	X	X	X	X	X	PS0	1	PS2	PS1	1	0	1	X

Table 4. Address Map (8 Channel Format) – cont'd

Digital Inputs

All digital inputs are LV_TTL compatible inputs.

Digital Outputs

SDOUT and LDOUT are CMOS outputs that switch between DGND and DVDD.

Power Supply Sequence

Power supplies must be controlled such that they maintain correct polarity with respect to each other and ground at all times during power-up and power-down. The following sequence is recommended:

1. AVEE
2. AVCC
3. AVDD, VREF
4. DVDD

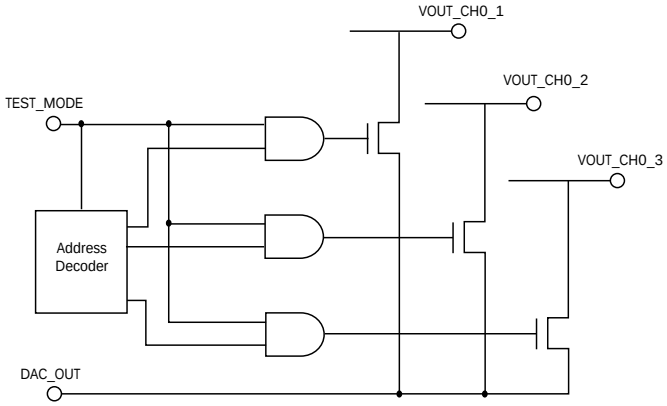


Figure 12. DAC Voltage Output via DAC_OUT

DAC Value Readback via DAC_OUT

Voltage Outputs

Each voltage output of the Edge6435/6436 has high impedance FET(s) connected from the outputs to a common analog line, DAC_OUT, that provides readback of each DAC's value. The primary purpose of this feature is to provide means for diagnostics of correct DAC functionality in an application that can monitor DAC_OUT, and is not intended for DAC calibration.

The feature utilizes the normal address decoding, as shown in Tables 3 and 4, as well as a "high" level on the TEST_MODE pin (see truth table below).

TEST_MODE	DAC_OUT
0	Off
1	On

NOTE: A CLK input is not required to change the state of the DAC_OUT pin when TEST_MODE is toggled.

To test an output, a DAC should be loaded as described above. At this point, the DAC_OUT pin, which is an analog output, will reflect the voltage at the addressed DAC's output pin.

Note that DAC_OUT is switched off when the parallel load is selected (address 64). This prevents a parallel connection of all the DAC outputs when the scan feature is used.

Circuit Description *(continued)*

Current Outputs

The TEST_MODE and DAC_OUT pins on the Edge6435/6436 are used in the same way as for voltage outputs. The scan circuits for current outputs are shown in Figure 13.

The voltage measured at the DAC_OUT pin, using the configuration in Figure 13, for Group C and D current outputs are as follows:

$$V_{DAC\_OUT\_C} = (R_{SENSE\_C} + R_{PAD}) * I_{OUT\_C}$$

where:

$R_{SENSE\_C} = 160\Omega \pm 30\%$
$R_{PAD} = 30\Omega \pm 30\%$

and

$$V_{DAC\_OUT\_D} = (R_{SENSE\_D} + R_{PAD}) * I_{OUT\_D}$$

where:

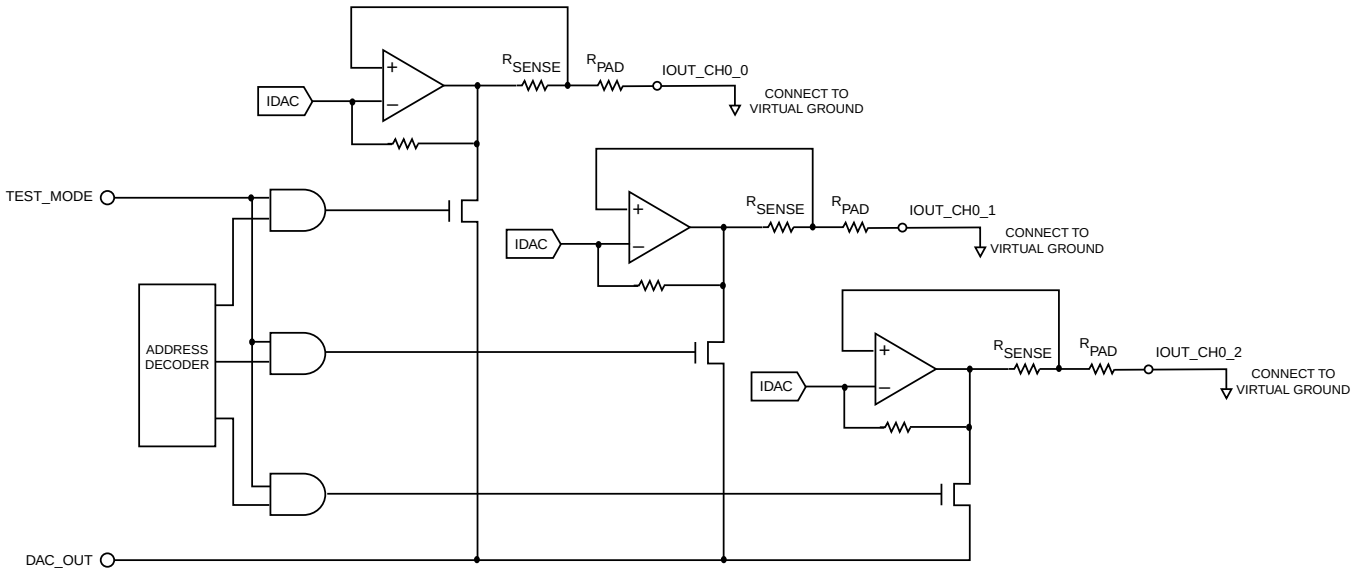
$R_{SENSE\_D} = 160\Omega \pm 30\%$
$R_{PAD} = 30\Omega \pm 30\%$

The typical "ON" resistance of the FET switch is 2 kΩ, but can vary from 900Ω to 3 kΩ as a function of process and output voltage.

Notes when Using DAC_OUT Feature with Multiple Chips

When multiple 6435/6436s are used on a board, and it is desired to gang the DAC_OUT pins of these 6435/6436s, or gang the TEST_MODE inputs to one point, it is required to ***protect*** the 6435/6436s against damage that the following rules be followed:

1) If TEST_MODE inputs are ganged together, DAC_OUT cannot be ganged, or invalid results will be observed at the DAC_OUT pin and ***damage*** could occur to the device. Hence, each DAC_OUT pin on a 6435/6436 will have to be measured separately.
2) If DAC_OUT is ganged, the TEST_MODE is used to select only one DAC at a time.



NOTE: WHEN ADDRESS 64 IS INVOKED (PARALLEL LOAD), SCAN IS DISABLED.

Figure 13. DAC Current Output vs DAC_OUT

Circuit Description *(continued)*

Latched Data readback via LD_OUT

Figure 14 provides a Functional Block Diagram of the means to readback, via LD_OUT, the status of latch's input into a selected DAC.

A DAC's latches are addressed for readback in the same way they are addressed to be written via the serial input, SDIN.

A DACs Rank A or Rank B latches are selcted by the RANK input for subsequent readback.

Readback is enabled internally by TESTMODE high whereupon the selected DAC's Rank A or Rank B latch outputs are loaded into the READBACK REGISTER by a leading edge of CLKIN while SHIFTOUT* is high. With SHIFTOUT* low, subsequent clocks into CLKIN will shift out, via LD_OUT, the status of the selected DAC's latches of Rank A or Rank B.

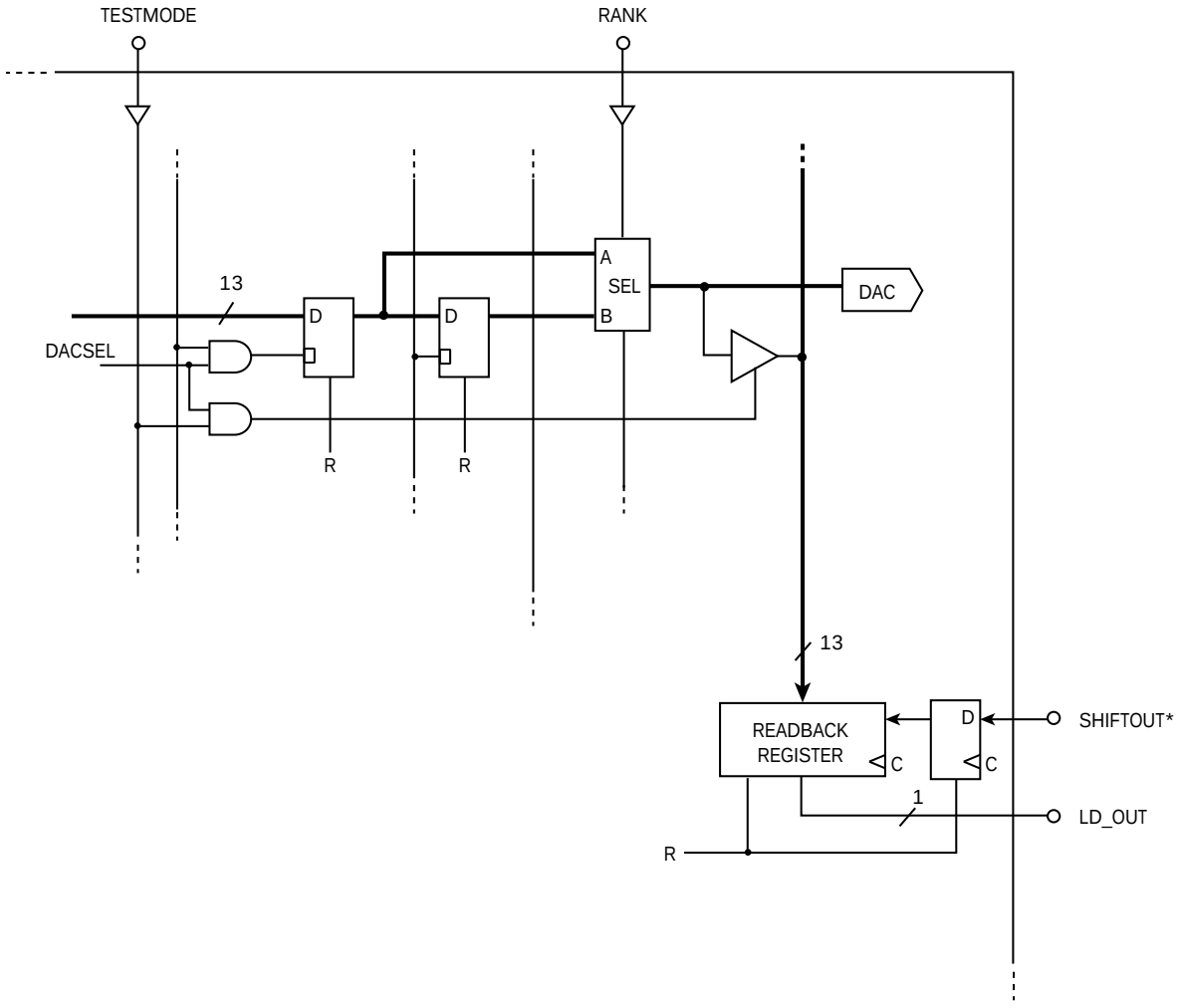
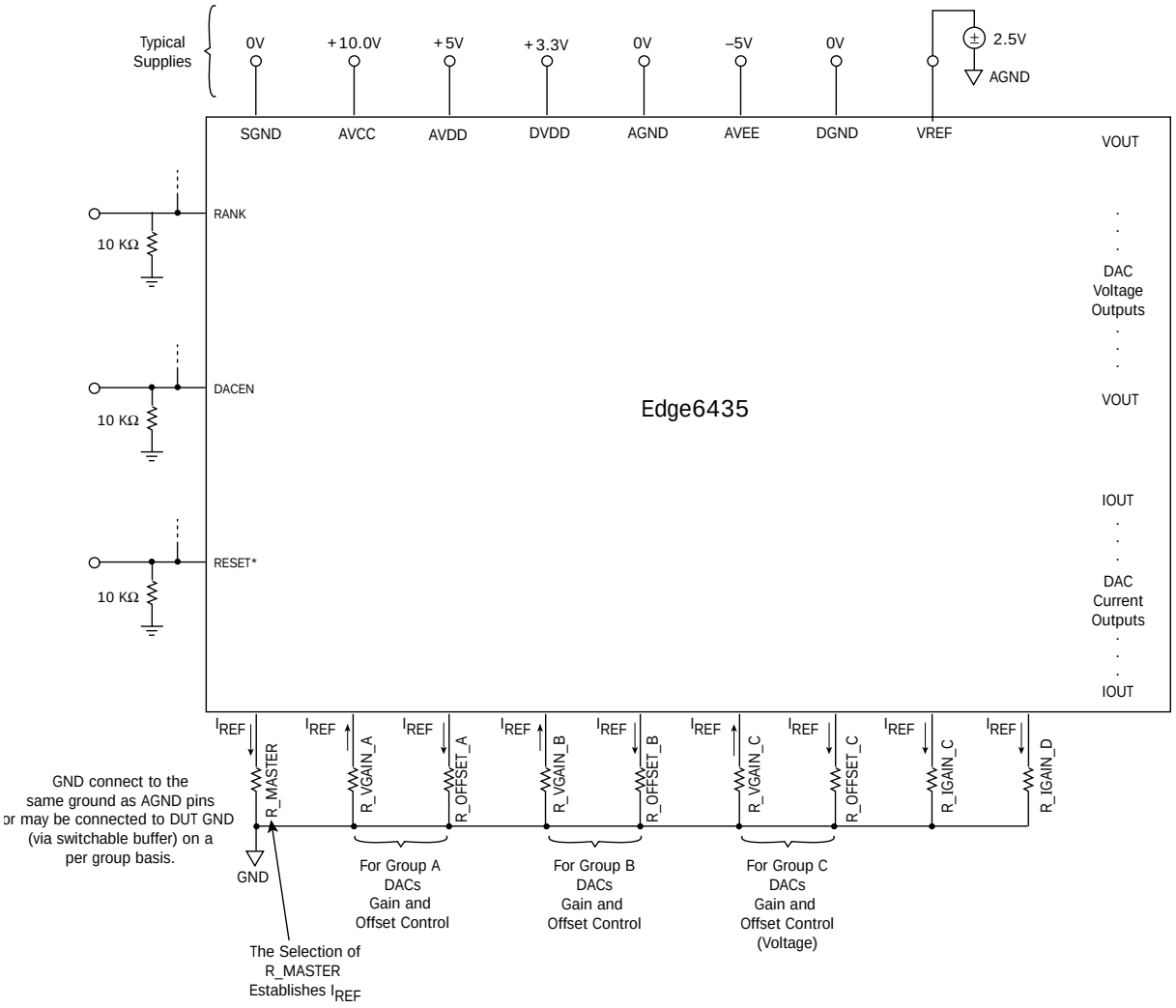


Figure 14. Latched Data Readback Functional Block Diagram



NOTE: Pull-down resistors required on RANK, DACEN, and RESET* to ensure they are low upon power-up. Such resistors may be common to multiple Edge6435s.

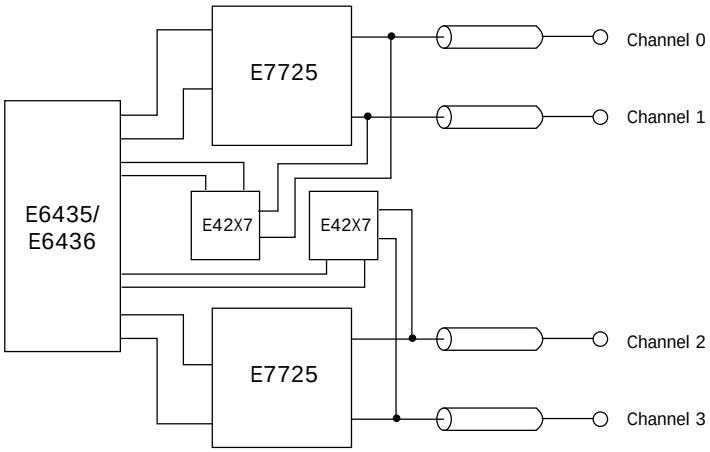
NOTE: Power Supply inputs AVCC, AVDD, DVDD and AVEE need bypass capacitors located at the inputs to the chip of 10 µF (tant.) and 0.1 µF (ceramic).

Figure 15. Required External Components

Application Information *(continued)*

The E6435/E6436 can be configured to provide all of the DAC levels required for 4 fully-featured high-speed pin channels or 8 fully-featured low-speed pin channels when used with other Semtech pin electronics components.

Since each E6435/E6436 DAC channel includes 2 sets of calibration registers, DAC channels can be shared across two distinct functions in an application to minimize the overall number of level DACs required in a system. Tables 5 and 6 show the recommended shorting scheme for a couple of possible pin electronics solutions.



High-Speed Pin Electronics Solution:

1 – E6435/E6436 per 4 Channels
2 – E7725 Dual Channel, High Speed Pin Driver + Comparator + Load + Signal Clamp devices per 4 Channels
2 – E42X7 Dual-Channel, Parametric Measurement Unit + Clamps per 4 Channels

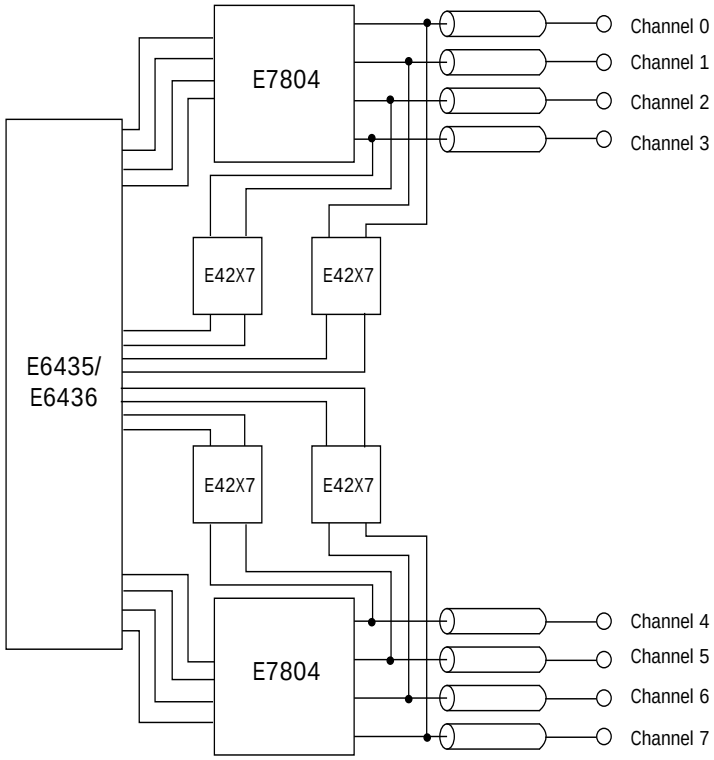
E6435/6436		E7725		E42X7	
Group	**V/I**	**Function**	**Symbol**	**Function**	**Symbol**
A	V	Driver "High" Level	DVH	Not used	N/A
A	V	Driver "Low Level	DVL	Not used	N/A
A	V	Upper Voltage Clamp	VCH	Upper Voltage Clamp	HLV
A	V	Lower Voltage Clamp	VCL	Lower Voltage Clamp	LLV
B	V	Comparator Threshold	CVA, CVC	Lower Comparator Threshold	IVMIN
B	V	Comparator Threshold	CVB	Upper Comparator Threshold	IVMAX
C	V	Termination Voltage	DVT, VCM	Not used	N/A
C	V	Not used	N/A	Voltage/Current Programming	VINP
C	I	Load Source Current	ISC	Not used	N/A
C	I	Load Sink Current	ISK	Not used	N/A
D	I	Driver "+" Slew Rate Adjust	RADJ	Not used	N/A
D	I	Driver "–" Slew Rate Adjust	FADJ	Not used	N/A

Table 5. E6435/E6436 Per-Channel DAC Connectivity for High-Speed Pin Driver, Comparator, Clamp and Load Solution Featuring Differential Capability and Fast Settling PMU Per Pin

Application Information *(continued)*

Low-Speed Pin Electronics Solution:

1 – E6435/E6436 per 8 Channels
2 – E7804 Quad Channel, Driver + Comparator + CTC per 8 Channels
devices per 4 Channels
4 – E42X7 Dual-Channel, Parametric Measurement Unit + Clamps per 8 Channels

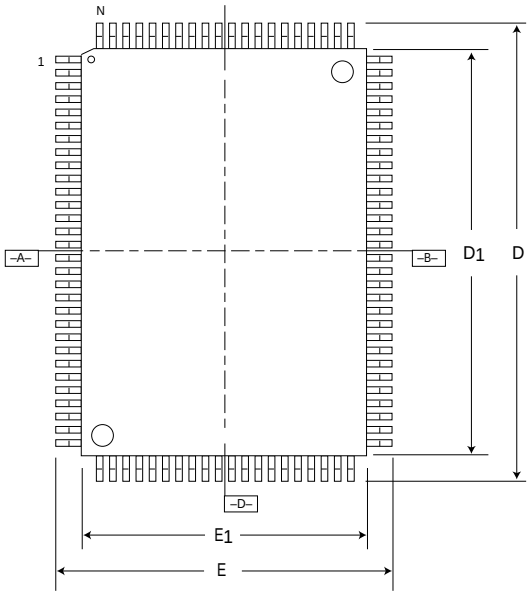


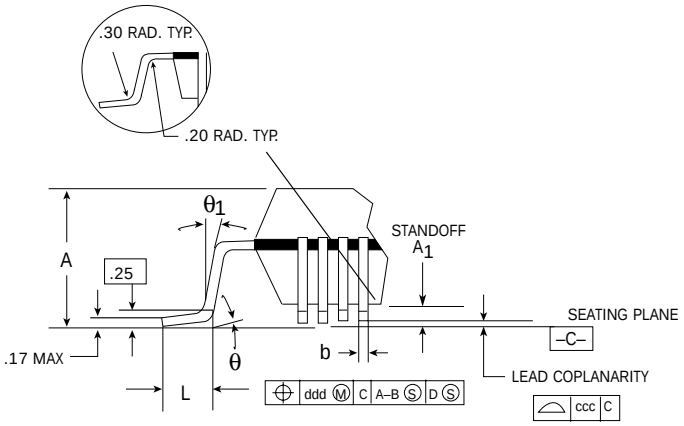
E6435/6436			E7804		E42X7	
Group	**V/I**	**Interconnect Circuit**	**Function**	**Symbol**	**Function**	**Symbol**
A	V	None required	Driver "High" Level	DVH	Voltage/Current Programming	VINP
A	V	None required	Driver "Low" Level	DVL	Comparator Threshold	IVMIN
B	V	None required	Comparator Threshold	CVA	Comparator Threshold	IVMAX
C	V	None required	Comparator Threshold	CVB	Upper Voltage Clamp	HLV
D(0)*	I	I to V Converter	Continuity Test Circuit	CTCFIV	Lower Voltage Clamp	LLV
D(1)*	I	I to V Converter	Continuity Test Voltage	CTCLV	Not used	N/A
D(2)*	I	I to V Converter	Pull-up Voltage	PVP	Not used	N/A
D(3-7)*	I	None required	Not used	N/A	Not used	N/A

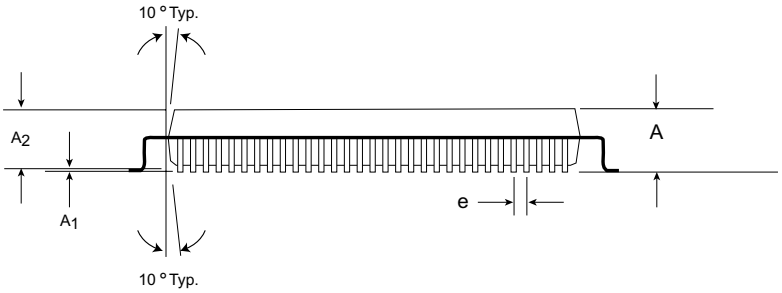
*D(0), D(1), D(n) correspond to DAC channels that are used for common continuity test voltage/current programming values across multiple E7804 devices and are shared with the lower voltage clamp threshold on the E42X7.

Table 6. E6435/E6436 Per-Channel DAC Connectivity for Low-Speed Pin Driver, Comparator, Continuity Test Circuit, and Per-Pin PMU Solution

Figure 16. 14 x 20 x 2.0 mm, 100-Pin MQFP (with Internal Heat Spreader, Requires Heat Sink)







BODY + 3.2mm FOOTPRINT, 2.0mm THICK		
DIMS.	**TOLS.**	
A	Max.	2.35
A1	Max.	.25
A2	±.10	2.00
D	±.20	23.20
D_1	±.10	20.00
E	±.20	17.20
E_1	±.10	14.00
L	±0.15	.88
e	Basic	.65
b		0.24~0.38
θ		0° – 7°
θ_1	±.4°	6°
ddd	Nom.	.12
ccc	Max	.10
JEDEC Ref. Dwg.		
Variation Designator		Note 8

Notes:
1. All dimensions in millimeters (mm).
2. Dimensions shown are nominal with tolerances indicated.
3. Foot length “L” is measured at gage plane 0.25mm above the seating plane.
4. Use MS-022 variation GA-1 for body dimensions.
5. Use MO-112 variation CA-1 for body dimensions.
6. Use variation GA-1 for lead form options and BB for body dime.
7. Use variation GB-1 for lead form options and BB for body dime.
8. Use variation GC-1 for lead form options and BB for body dime.
9. Use MS-022 variation BB for body dimensions.
10. N.J.R. means no single JEDEC reference putline or standard.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply	AVCC	+8.0	+10.0	+15.0	V
Positive Analog Power Supply 2	AVDD	+4.75	+5.0	+5.25	V
Negative Power Supply 1	AVEE	–5.25	–5.0	–4.75	V
Reference Voltage	VREF	2.499		2.501	V
Total Analog Supply 1	AVCC – AVEE	12.75		20.25	V
Digital Power Supply	DVDD – DGND	3.0		+5.25	V
Digital Ground	DGND	–0.5	0	+0.5	V
Thermal Resistance of Package					
Junction to Case	θ_{JC}		12.4		°C/W
Junction to Ambient	θ_{JA}				
Still Air			28		°C/W
100 lfpm			25.2		°C/W
400 lfpm			22.1		°C/W
Case Temperature	T_{CASE}	25		65	°C

NOTE: All supplies are referenced to AGND unless otherwise noted.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Positive Analog Supply	AVCC	–0.5	+16	V
Positive Analog Supply 2	AVDD		+5.5	V
Negative Analog Supply	AVEE	–5.5	+0.5	V
Digital Power Supply	DVDD	–0.5	+5.5	V
Total Power Supply				
	AVCC – AVEE	–0.5	+21.5	V
	AVCC –AVDD	–0.5	+16.0	V
	AGND	–0.5	+5.5	V
	AGND	–5.5	+0.5	V
	AGND	–0.5	+0.5	V
	VREF	AGND – 0.5	AVDD + 0.5	V
Digital Input Voltages				
DVDD < 5.0V	SDIN, CLKIN, LOAD, STORE, UPDATE, SELVIC, RANK, RESET*	DGND – 0.5	DVDD + 0.5	V
DVDD > 5.0V		DGND – 0.5	+5.5	V
Analog Input Voltages	$V_{REF[1:4]}$, V_{MASTER}, $V_{OFFSET\_[A:C]}$, $V_{GAIN\_[A:C]}$	AGND – 0.5	AVDD + 0.5	V
Analog Input Currents	$I_{GAIN\_[C:D]}$	–100	+100	µA
	I_{MASTER}	–100	+100	µA
Analog Output Voltages				
Groups A, B, C	VOUT_[A:C]	AVEE – 0.5	AVCC + 0.5	V
Analog Output Currents				
Groups A, B, C Continuous DC Current	IOUT_[A:C]	–300	+300	µA
Ambient Operating Temperature	TA	0	+125	˚C
Storage Temperature	TS	–65	+150	˚C
Junction Temperature	TJ		+125	˚C
Soldering Temperature (5 seconds, .25" from the pin)	TSOL		+260	˚C

NOTE: All supplies are referenced to AGND unless otherwise noted.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

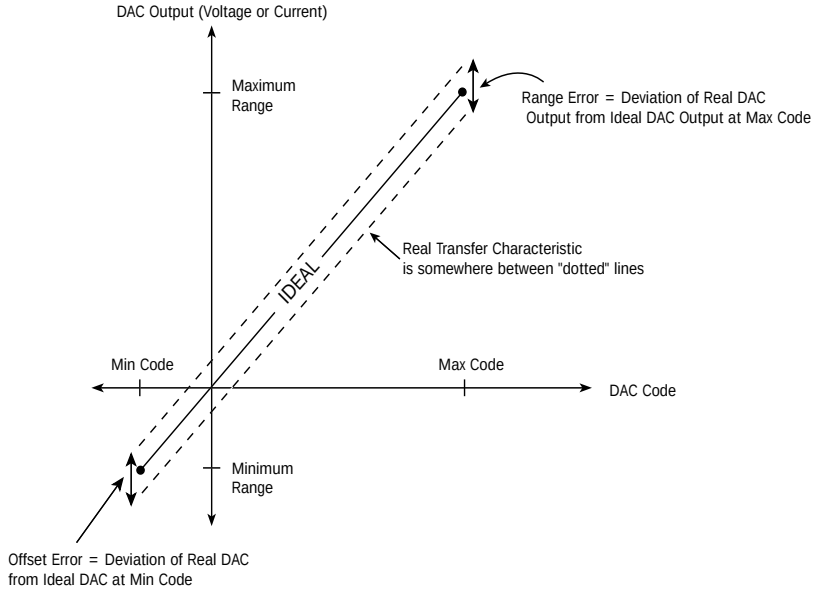
DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs (SDIN, CLKIN, LOAD, STORE, UPDATE, RANK, RESET*, TESTMODE, DACEN, FORMAT)					
Input Low Voltage	VIL			0.8	V
Input High Voltage	VIH				
3.0V ≤ DVDD ≤ 3.3V		2.0			V
3.3V < DVDD ≤ 5.25V		2.6			V
Input Current	IIL, IIH	–1		1	µA
Digital Outputs (SDOUT, LDOUT)					
Output Low Voltage	VOL			0.4	V
Output High Voltage	VOH	2.4		DVDD	V
Output Current Low	IOL			1.6	mA
Output Current High	IOH	–0.4			mA
DAC Voltage Outputs					
Groups A, B, and C (Voltage Outputs) Resolution		13			Bits
Output Voltage Range	VOUT_RANGE	AVEE + 1.25		AVCC – 1.25	V
Output Voltage Span	VOUT_SPAN	8.0		16.75	V
Output Offset Range	V_{OFFSET}	–3.5		–0.75	V
Output Current Compliance	$I_{COMPLIANCE}$	–200		+200	µA
Range Error (Figure 17)	FS_ERROR	–215		+215	mV
Offset Error (Figure 17)	V_{OS}	–35		+35	mV
Integral Linearity Error following 2-Point Calibration 20% - 80% Calibration Points (Figure 18)					
E6436 DACs		–4		+4	LSB
E6435 DACs		–8		+8	LSB
Endpoint Calibration Points (Figure 19)					
E6436 DACs		–4		+4	LSB
E6435 DACs		–8		+8	LSB
Integral Linearity Error following 7-Point Calibration (Calibration Points: 0, 1365, 2730, 4095, 5460, 6825, 8191)	INL	–2		2	LSB
Differential Linearity Error (Figure 19)	DNL	–1		+1	LSB
Gain TempCo			250		µV/°C
Offset Error TempCo			250		µV/°C
DAC Disabled Output Voltage (DACEN = 0)		–100		+100	mV
DAC Interaction (DC Channel-to-Channel Crosstalk)		–1		+1	mV

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Group C (Current Outputs)					
Resolution		13			Bits
Output Current Range	IOUT	0.5		2.05	mA
Output Voltage Compliance		–0.2		3.0	V
Integral Linearity Error following Calibration (Figure 18)	INL				
20% - 80% Calibration Points (Figure 18)		–7		+7	LSB
Endpoint Calibration Points (Figure 19)		–7		+7	LSB
Diffrential Linearity Error (Figure 19)	DNL	–1		1	LSB
Range Error (Figure 17)		–70		+70	µA
Offset Error (Figure 17)	I_{OS}	–20		+ 20	µA
Gain TempCo			–130		pA/˚C
Offset Error TempCo			30		pA/˚C
DAC Disabled Output Current		–20	0	+20	µA
Group D (Current Outputs)					
Resolution		6			Bits
Output Current Range	IOUT	0.8		1.6	mA
Output Voltage Compliance		–0.2		3.0	V
Integral Linearity Error following Calibration (Figure 18)	INL				
20% - 80% Calibration Points (Figure 18)		–0.075		+0.075	LSB
Endpoint Calibration Points (Figure 19)		–0.075		+0.075	LSB
Differential Linearity Error (Figure 20)	DNL	–0.025		+0.025	LSB
Range Error (Figure 17)		–70		+70	µA
Offset Error (Figure 17)	I_{OS}	–20	0	20	µA
Gain TempCo			50		pA/˚C
Offset Error TempCo			30		pA/˚C
DAC Disabled Output Current		–20	0	+20	µA

DC Characteristics *(continued)*



Range error and offset error are due to E6435/6436 only. External resistor tolerances and VREF tolerance not included.

Figure 17. Representation of DAC Offset Error and Range Error for 13-Bit DACs (6-bit DACs similar)

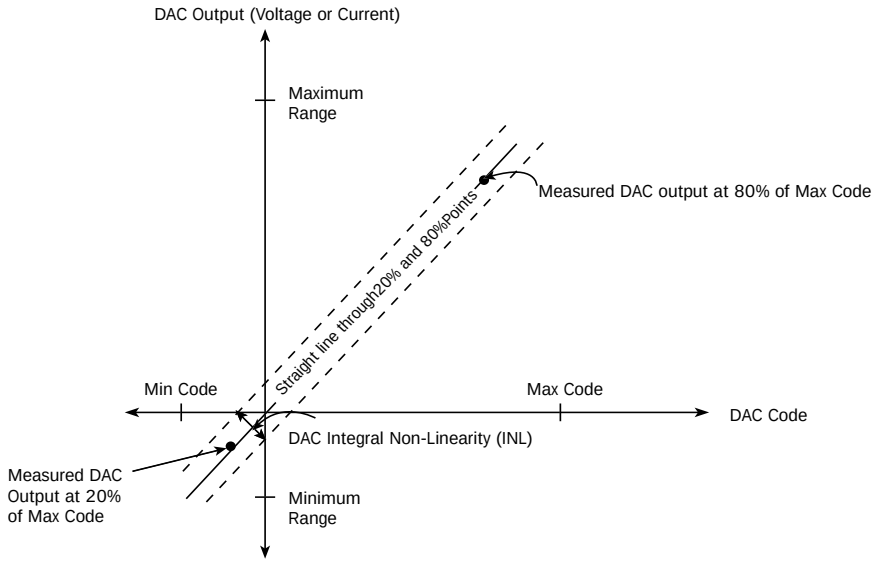


Figure 18. Representation of 2-Point DAC Integral Non-Linearity (INL)

DC Characteristics *(continued)*

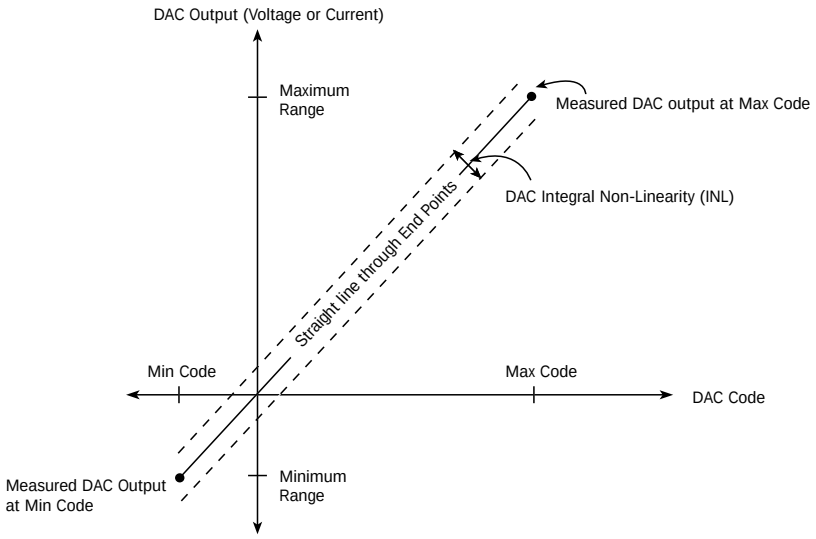


Figure 19. Representation of 2-Point DAC Integral Non-Linearity (INL)

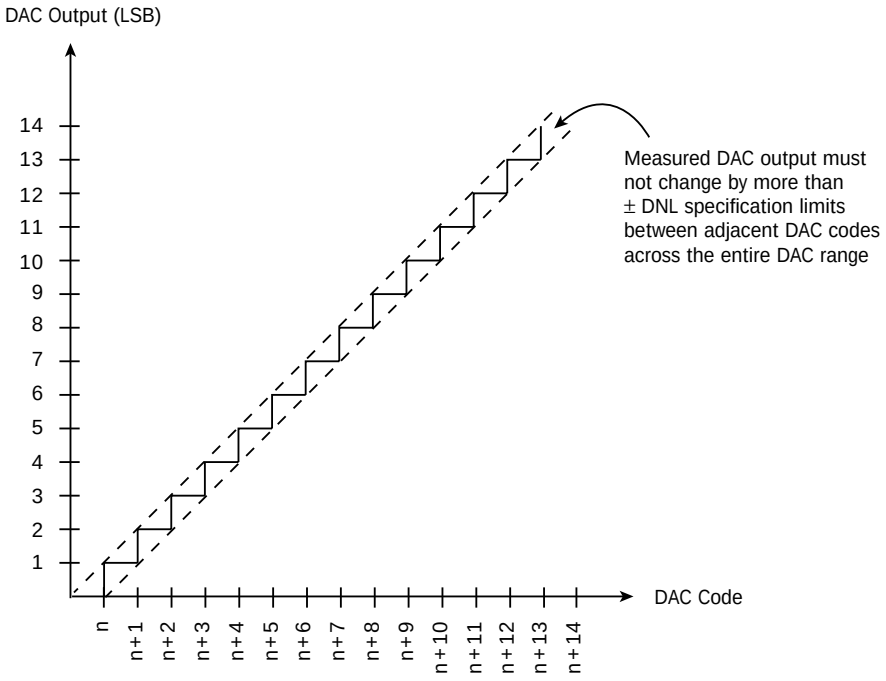


Figure 20. Representation of Differential Non-Linearity (DNL)

DC Characteristics *(continued)*

Power Supplies

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Consumption (Note 1)					
Positive Analog Supply (AVCC)	ICC		15	20	mA
Positive Analog Supply (AVDD)	IADD		20	30	mA
Digital Supply (DVDD)	IDDD				
3.0V ≤ DVDD ≤ 3.3V			250	500	µA
3.3V < DVDD ≤ 5.25V				800	µA
Negative Power Supply (AVEE)	IEE	–50	–30		mA
Reference Supply	IREF	–0.2		+0.2	µA

Note 1: CLKIN Low, quiescent.

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Rejection Ratio	PSRR				
AVCC to any DAC Output					
DC		–88			dB
100 kHz			–27		dB
500 kHz			–20		dB
1 MHz			–18		dB
AVEE to any DAC Output					
DC		–66			dB
100 kHz			–8		dB
500 kHz			–5		dB
1 MHz			–13		dB
AVDD to any DAC Output					
DC		–62			dB
100 kHz			–3		dB
500 kHz			–18		dB
1 MHz			–26		dB

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Set Up Times (to CLKIN rising edge)					
SDIN	T_{SU_SDI}	2			ns
LOAD	T_{SU_LD}	2			ns
STORE	TSU_STR	2			ns
UPDATE	TSU_UPD	2			ns
RESET*	TSU_RST	2			ns
DACEN	TSU_DEN	2			ns
SHIFTOUT*	TSU_SOUT	2			ns
Hold Times					
SDIN (to CLKIN rising edge)	T_{HLD_SDI}	2			ns
LOAD	T_{HLD_LD}	2			ns
STORE	THLD_STR	2			ns
UPDATE	THLD_UPD	2			ns
SHIFTOUT*	THLD_SOUT	2			ns
Output Times (to CLKIN Rising Edge)					
SDOUT	TO_SDOUT			18	ns
LDOUT	TO_LDOUT			18	ns
CLKIN					
Fmax	F_{max}				
DVDD = 3.0V to 3.3V				60	MHz
DVDD = 4.75V to 5.25V				80	MHz
Clock Spacing	CS_CK	5			ns
Clock Width	CW_CK	5			ns
RESET Pulse Width	PW_{RESET}	3			ns
DAC Output Settling Time (Note 2)					
Full-Scale Step (DAC Code 0 to 8191)	V_{settle}				
Voltage DACs (Groups A, B, C)					
16V Range					
Settling to Specified Linearity Error				65	µs
Settling to ±0.5% FSR				50	µs
8V Range					
Settling to Specified Linearity Error				30	µs
Settling to ±0.5% FSR				30	µs
Current DACs					
Grroup C					
Settling to Specified Linearity Error				45	µs
Settling to ±0.5% FSR				35	µs
Grroup D (Full-Scale Step, DAC Code 0 to 63)					
Settling to Specified Linearity Error				40	µs
Settling to ±0.5% FSR				30	µs
DAC_OUT Readback Time (Note 1)			2.3	5	µs
Voltage DAC Output Enable Time (Note 4)	V_{toe}			4	µs
Voltage DAC Output Disable Time (Note 5)	V_{tz}			18	µs
Current DAC Output Enable Time (Note 4)	I_{toe}			1.5	µs
Current DAC Output Disable Time (Note 6)	I_{tz}			7	µs
Rank Transition Time (Note 3)	T_{rank}			1.5	µs

AC Characteristics *(continued)*

Note 1: DAC_OUT Readback Time is the amount of time required for DAC_OUT to display a valid voltage for a selected (and fully settled) DAC channel and only includes channel-to-channel switching time.

Note 2: Measured from CLKIN using edge of update to specified accuracy.

Note 3: Rank Transition Time is a measurement of the time required to change between Rank A and Rank B latches and does not include DAC Output Settling time.

Note 4: DAC Output Enable Time is measured after DACEN is transitioned from 0 to 1 from the rising edge of the clock signal applied to CLKIN as the time required for the DAC output to change by 10%.

Note 5: Voltage DAC output disable time is measured from the falling edge of DACEN as the amount of time required for the DAC output to change from positive full-scale to 0.5V.

Note 6: Current DAC Output Disable Time is measured from the falling edge of DACEN as the amount of time required for the DAC output to change by 10%.

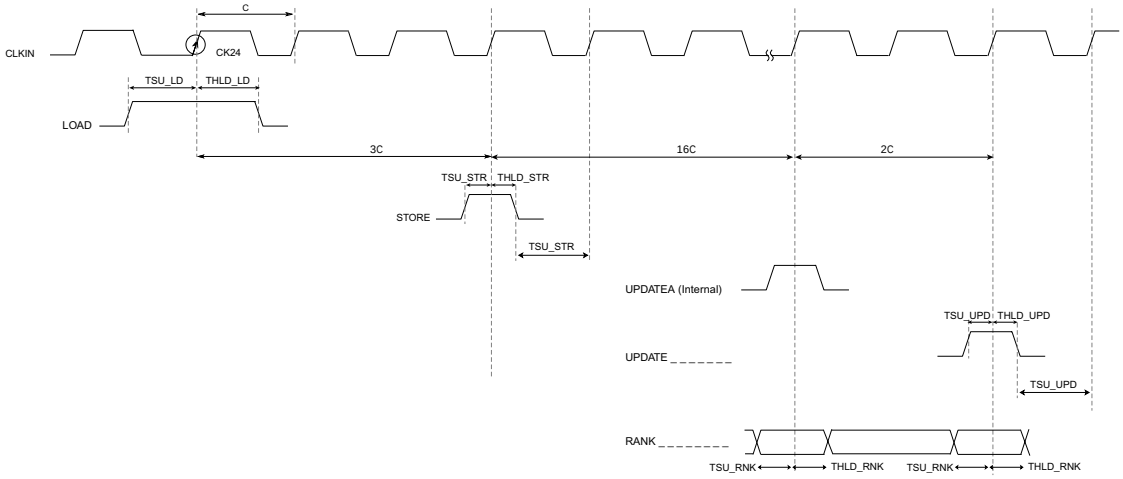


Figure 21. Individual DAC Storing and DAC Updating (RESET* high)

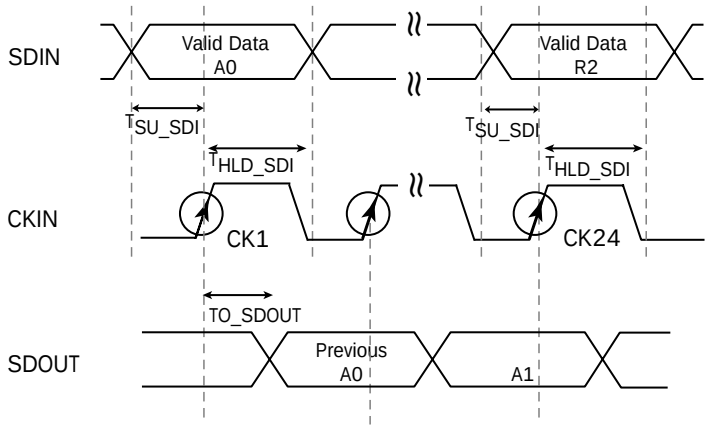


Figure 22. Shift Register Loading Timing Diagram

AC Characteristics *(continued)*

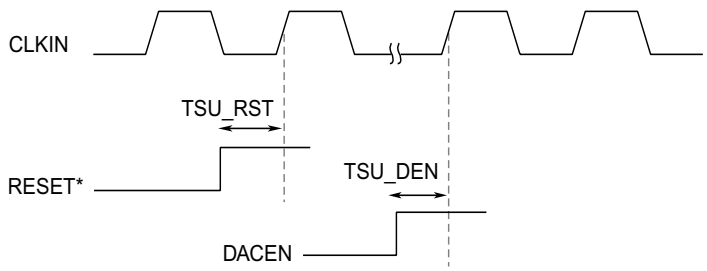


Figure 23. RESET* and DACEN Timing

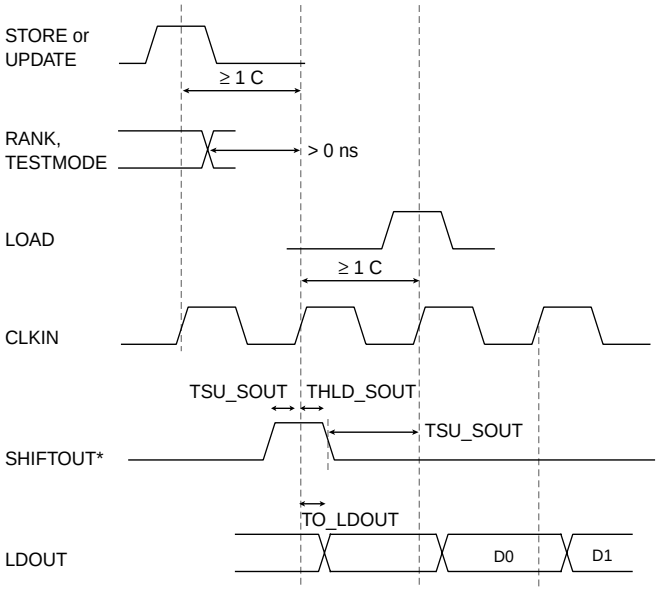


Figure 24. SHIFTOUT*, LDOUT Timing

Ordering Information

Model Number	Package
E6435BHFT	14 x 20 x 2 mm, 100 Pin MQFP (with Internal Heat Spreader)
EVM6435	Edge6435 Evaluation Board
E6436BHFT	14 x 20 x 2 mm, 100 Pin MQFP (with Internal Heat Spreader)
EVM6436	Edge6436 Evaluation Board

Pb This product is lead-free.

Contact Information

Semtech Corporation
Test and Measurement Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633