ELPIDA

DATA SHEET

512MB DDR SDRAM SO-DIMM

EBD52UD6ADSA-E (64M words × 64 bits, 2 Ranks)

Description

The EBD52UD6ADSA is 64M words × 64 bits, 2 ranks Double Data Rate (DDR) SDRAM Small Outline Dual In-line Memory Module, mounting 8 pieces of 512M bits DDR SDRAM sealed in TSOP package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- 200-pin socket type small outline dual in line memory module (SO-DIMM)
  - PCB height: 31.75mm
  - Lead pitch: 0.6mm
  - Lead-free
- 2.5V power supply
- Data rate: 333Mbps/266Mbps (max.)
- 2.5 V (SSTL_2 compatible) I/O
- Double Data Rate architecture; two data transfers per clock cycle
- Bi-directional, data strobe (DQS) is transmitted /received with data, to be used in capturing data at the receiver
- Data inputs, outputs and DM are synchronized with DQS
- 4 internal banks for concurrent operation (Components)
- DQS is edge aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data referenced to both edges of DQS
- Data mask (DM) for write data
- Auto precharge option for each burst access
- Programmable burst length: 2, 4, 8
- Programmable /CAS latency (CL): 2, 2.5
- Refresh cycles: (8192 refresh cycles /64ms)
  - 7.8μs maximum average periodic refresh interval
- 2 variations of refresh
  - Auto refresh
  - Self refresh

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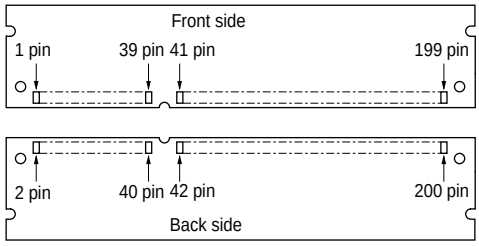
Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBD52UD6ADSA-6B-E	333	DDR333B (2.5-3-3)	200-pin SO-DIMM	Gold	EDD5116ADTA-6B-E
EBD52UD6ADSA-7A-E	266	DDR266A (2-3-3)	(lead-free)		EDD5116ADTA-6B/7A-E
EBD52UD6ADSA-7B-E	266	DDR266B (2.5-3-3)			EDD5116ADTA-6B/7A/7B-E

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	51	VSS	2	VREF	52	VSS
3	VSS	53	DQ19	4	VSS	54	DQ23
5	DQ0	55	DQ24	6	DQ4	56	DQ28
7	DQ1	57	VDD	8	DQ5	58	VDD
9	VDD	59	DQ25	10	VDD	60	DQ29
11	DQS0	61	DQS3	12	DM0	62	DM3
13	DQ2	63	VSS	14	DQ6	64	VSS
15	VSS	65	DQ26	16	VSS	66	DQ30
17	DQ3	67	DQ27	18	DQ7	68	DQ31
19	DQ8	69	VDD	20	DQ12	70	VDD
21	VDD	71	NC	22	VDD	72	NC
23	DQ9	73	NC	24	DQ13	74	NC
25	DQS1	75	VSS	26	DM1	76	VSS
27	VSS	77	NC	28	VSS	78	NC
29	DQ10	79	NC	30	DQ14	80	NC
31	DQ11	81	VDD	32	DQ15	82	VDD
33	VDD	83	NC	34	VDD	84	NC
35	CK0	85	NC	36	VDD	86	NC
37	/CK0	87	VSS	38	VSS	88	VSS
39	VSS	89	CK2	40	VSS	90	VSS
41	DQ16	91	/CK2	42	DQ20	92	VDD
43	DQ17	93	VDD	44	DQ21	94	VDD
45	VDD	95	CKE1	46	VDD	96	CKE0
47	DQS2	97	NC	48	DM2	98	NC
49	DQ18	99	A12	50	DQ22	100	A11
101	A9	151	DQ42	102	A8	152	DQ46
103	VSS	153	DQ43	104	VSS	154	DQ47
105	A7	155	VDD	106	A6	156	VDD

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
107	A5	157	VDD	108	A4	158	/CK1
109	A3	159	VSS	110	A2	160	CK1
111	A1	161	VSS	112	A0	162	VSS
113	VDD	163	DQ48	114	VDD	164	DQ52
115	A10/AP	165	DQ49	116	BA1	166	DQ53
117	BA0	167	VDD	118	/RAS	168	VDD
119	/WE	169	DQS6	120	/CAS	170	DM6
121	/CS0	171	DQ50	122	/CS1	172	DQ54
123	NC	173	VSS	124	NC	174	VSS
125	VSS	175	DQ51	126	VSS	176	DQ55
127	DQ32	177	DQ56	128	DQ36	178	DQ60
129	DQ33	179	VDD	130	DQ37	180	VDD
131	VDD	181	DQ57	132	VDD	182	DQ61
133	DQS4	183	DQS7	134	DM4	184	DM7
135	DQ34	185	VSS	136	DQ38	186	VSS
137	VSS	187	DQ58	138	VSS	188	DQ62
139	DQ35	189	DQ59	140	DQ39	190	DQ63
141	DQ40	191	VDD	142	DQ44	192	VDD
143	VDD	193	SDA	144	VDD	194	SA0
145	DQ41	195	SCL	146	DQ45	196	SA1
147	DQS5	197	VDDSPD	148	DM5	198	SA2
149	VSS	199	VDDID	150	VSS	200	NC

Pin Description

Pin name	Function
A0 to A12	Address input Row address A0 to A12 Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0, /CS1	Chip select
CKE0, CKE1	Clock enable
CK0 to CK2	Clock input
/CK0 to /CK2	Differential clock input
DQS0 to DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0 to SA2	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREF	Input reference voltage
VSS	Ground
VDDID	VDD identification flag
NC	No connection

Serial PD Matrix

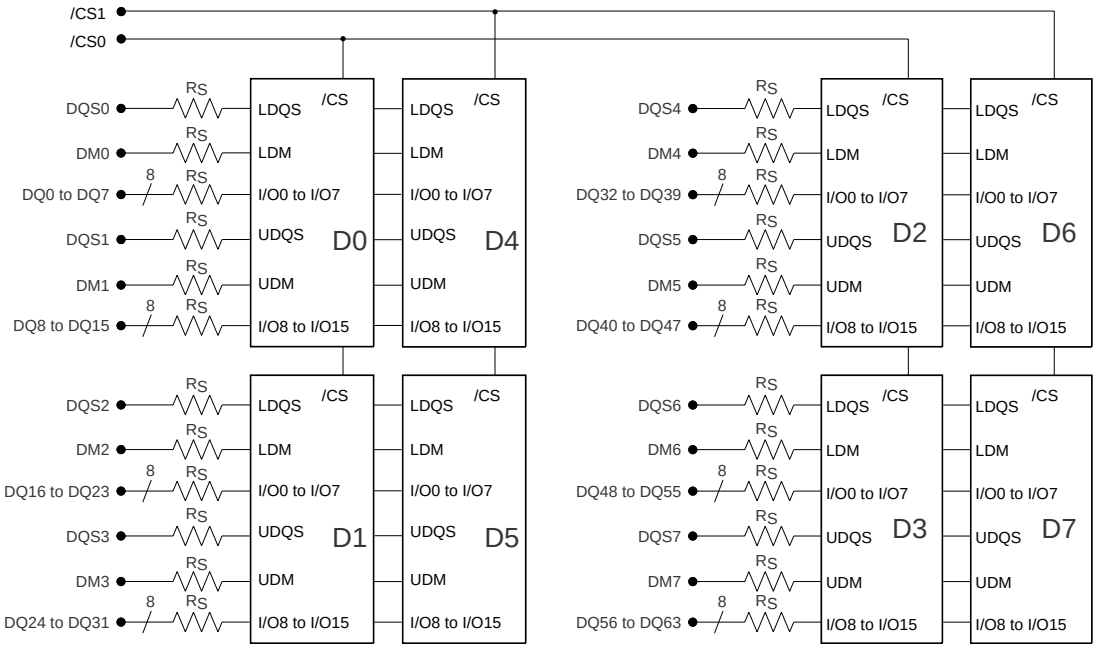
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80H	128 bytes
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	0	1	1	1	07H	DDR SDRAM
3	Number of row address	0	0	0	0	1	1	0	1	0DH	13
4	Number of column address	0	0	0	0	1	0	1	0	0AH	10
5	Number of DIMM ranks	0	0	0	0	0	0	1	0	02H	2
6	Module data width	0	1	0	0	0	0	0	0	40H	64 bits
7	Module data width continuation	0	0	0	0	0	0	0	0	00H	0
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04H	SSTL2
9	DDR SDRAM cycle time, CL = X -6B	0	1	1	0	0	0	0	0	60H	CL = 2.5*[1]
	-7A, -7B	0	1	1	1	0	1	0	1	75H	
10	SDRAM access from clock (tAC) -6B	0	1	1	1	0	0	0	0	70H	0.7ns*[1]
	-7A, -7B	0	1	1	1	0	1	0	1	75H	0.75ns*[1]
11	DIMM configuration type	0	0	0	0	0	0	0	0	00H	None
12	Refresh rate/type	1	0	0	0	0	0	1	0	82H	7.8µs Self refresh
13	Primary SDRAM width	0	0	0	1	0	0	0	0	10H	× 16
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00H	Not used
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01H	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0EH	2,4,8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04H	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	1	1	0	0	0CH	2, 2.5
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01H	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	1	0	02H	1
21	SDRAM module attributes	0	0	1	0	0	0	0	0	20H	Unbuffered
22	SDRAM device attributes: General	1	1	0	0	0	0	0	0	C0H	VDD ± 0.2V
23	Minimum clock cycle time at CL = X –0.5 -6B, -7A	0	1	1	1	0	1	0	1	75H	CL = 2*[1]
	-7B	1	0	1	0	0	0	0	0	A0H	
24	Maximum data access time (tAC) from clock at CL = X –0.5 -6B	0	1	1	1	0	0	0	0	70H	0.7ns*[1]
	-7A, -7B	0	1	1	1	0	1	0	1	75H	0.75ns*[1]
25 to 26		0	0	0	0	0	0	0	0	00H	
27	Minimum row precharge time (tRP) -6B	0	1	0	0	1	0	0	0	48H	18ns
	-7A, -7B	0	1	0	1	0	0	0	0	50H	20ns
28	Minimum row active to row active delay (tRRD) -6B	0	0	1	1	0	0	0	0	30H	12ns
	-7A, -7B	0	0	1	1	1	1	0	0	3CH	15ns

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
29	Minimum /RAS to /CAS delay (tRCD) -6B	0	1	0	0	1	0	0	0	48H	18ns
	-7A, -7B	0	1	0	1	0	0	0	0	50H	20ns
30	Minimum active to precharge time (tRAS) -6B	0	0	1	0	1	0	1	0	2AH	42ns
	-7A, -7B	0	0	1	0	1	1	0	1	2DH	45ns
31	Module rank density	0	1	0	0	0	0	0	0	40H	256M bytes × 2 ranks
32	Address and command setup time before clock (tIS) -6B	0	1	1	1	0	1	0	1	75H	0.75ns[*1]
	-7A, -7B	1	0	0	1	0	0	0	0	90H	0.9ns[*1]
33	Address and command hold time after clock (tIH) -6B	0	1	1	1	0	1	0	1	75H	0.75ns[*1]
	-7A, -7B	1	0	0	1	0	0	0	0	90H	0.9ns[*1]
34	Data input setup time before clock (tDS) -6B	0	1	0	0	0	1	0	1	45H	0.45ns[*1]
	-7A, -7B	0	1	0	1	0	0	0	0	50H	0.5ns[*1]
35	Data input hold time after clock (tDH) -6B	0	1	0	0	0	1	0	1	45H	0.45ns[*1]
	-7A, -7B	0	1	0	1	0	0	0	0	50H	0.5ns[*1]
36 to 40	Superset information	0	0	0	0	0	0	0	0	00H	Future use
41	Active command period (tRC) -6B	0	0	1	1	1	1	0	0	3CH	60ns[*1]
	-7A, -7B	0	1	0	0	0	0	0	1	41H	65ns[*1]
42	Auto refresh to active/ Auto refresh command cycle (tRFC) -6B	0	1	0	0	1	0	0	0	48H	72ns[*1]
	-7A, -7B	0	1	0	0	1	0	1	1	4BH	75ns[*1]
43	SDRAM tCK cycle max. (tCK max.)	0	0	1	1	0	0	0	0	30H	12ns*[1]
44	Dout to DQS skew -6B	0	0	1	0	1	1	0	1	2DH	0.45ns[*1]
	-7A, -7B	0	0	1	1	0	0	1	0	32H	0.5ns[*1]
45	Data hold skew (tQHS) -6B	0	1	0	1	0	1	0	1	55H	0.55ns[*1]
	-7A, -7B	0	1	1	1	0	1	0	1	75H	0.75ns[*1]
46 to 61	Superset information	0	0	0	0	0	0	0	0	00H	Future use
62	SPD Revision	0	0	0	0	0	0	0	0	00H	
63	Checksum for bytes 0 to 62 -6B	0	0	0	0	1	0	0	1	09H	
	-7A	1	1	0	0	0	0	0	0	C0H	
	-7B	1	1	1	0	1	0	1	1	EBH	
64 to 65	Manufacturer's JEDEC ID code	0	1	1	1	1	1	1	1	7FH	Continuation code
66	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
67 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	(ASCII-8bit code)
73	Module part number	0	1	0	0	0	1	0	1	45H	E
74	Module part number	0	1	0	0	0	0	1	0	42H	B

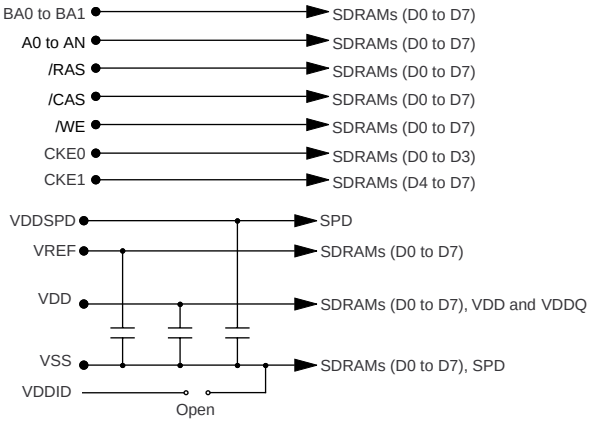
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
75	Module part number	0	1	0	0	0	1	0	0	44H	D
76	Module part number	0	0	1	1	0	1	0	1	35H	5
77	Module part number	0	0	1	1	0	0	1	0	32H	2
78	Module part number	0	1	0	1	0	1	0	1	55H	U
79	Module part number	0	1	0	0	0	1	0	0	44H	D
80	Module part number	0	0	1	1	0	1	1	0	36H	6
81	Module part number	0	1	0	0	0	0	0	1	41H	A
82	Module part number	0	1	0	0	0	1	0	0	44H	D
83	Module part number	0	1	0	1	0	0	1	1	53H	S
84	Module part number	0	1	0	0	0	0	0	1	41H	A
85	Module part number	0	0	1	0	1	1	0	1	2DH	—
86	Module part number -6B	0	0	1	1	0	1	1	0	36H	6
	-7A, -7B	0	0	1	1	0	1	1	1	37H	7
87	Module part number -6B, -7B	0	1	0	0	0	0	1	0	42H	B
	-7A	0	1	0	0	0	0	0	1	41H	A
88	Module part number	0	0	1	0	1	1	0	1	2DH	—
89	Module part number	0	1	0	0	0	1	0	1	45H	E
90	Module part number	0	0	1	0	0	0	0	0	20H	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30H	Initial
92	Revision code	0	0	1	0	0	0	0	0	20H	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (HEX)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (HEX)
95 to 98	Module serial number										
99 to 127	Manufacture specific data										

Note: These specifications are defined based on component specification, not module.

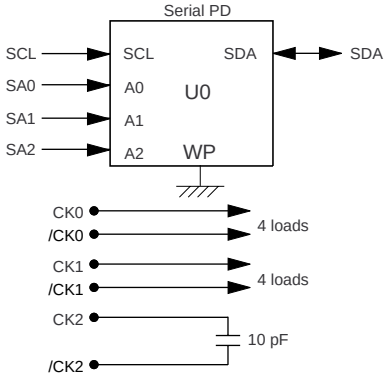
Block Diagram



* D0 to D7 : 512M bits DDR SDRAM
U0 : 2k bits EEPROM
Rs : 22Ω



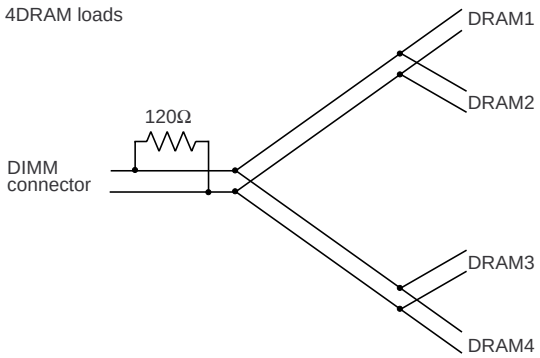
Serial PD



Notes :

1. DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
   VDDID strap connections:
   (for memory device VDD, VDDQ)
   Strap out (open): VDD = VDDQ
   Strap in (closed): VDD ≠ VDDQ
2. The SDA pull-up registor is reguired due to the open-drain/open-collector output.
3. The SCL pull-up registor is recommended, because of the normal SCL lime inactive "high" state.

Logical Clock Net Structure



Electrical Specifications

- All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–1.0 to +3.6	V	
Supply voltage relative to VSS	VDD	–1.0 to +3.6	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	8	W	
Operating ambient temperature	TA	0 to +70	°C	1
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. DDR SDRAM component specification.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Operating Conditions (TA = 0 to +70°C) (DDR SDRAM Component Specification)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	2.3	2.5	2.7	V	1
	VSS	0	0	0	V	
Input reference voltage	VREF	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	
Input high voltage	VIH (DC)	VREF + 0.15	—	VDDQ + 0.3	V	2
Input low voltage	VIL (DC)	–0.3	—	VREF – 0.15	V	3
Input voltage level, CK and /CK inputs	VIN (DC)	–0.3	—	VDDQ + 0.3	V	4
Input differential cross point voltage, CK and /CK inputs	VIX (DC)	0.5 × VDDQ – 0.2V	0.5 × VDDQ	0.5 × VDDQ + 0.2V	V	
Input differential voltage, CK and /CK inputs	VID (DC)	0.36	—	VDDQ + 0.6	V	5, 6

Notes: 1. VDDQ must be lower than or equal to VDD.
2. VIH is allowed to exceed VDD up to 3.6V for the period shorter than or equal to 5ns.
3. VIL is allowed to outreach below VSS down to –1.0V for the period shorter than or equal to 5ns.
4. VIN (DC) specifies the allowable DC execution of each differential input.
5. VID (DC) specifies the input differential voltage required for switching.
6. VIH (CK) min assumed over VREF + 0.18V, VIL (CK) max assumed under VREF – 0.18V if measurement.

DC Characteristics 1 (TA = 0 to +70°C, VDD = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current (ACTV-PRE)	IDD0	-6B -7A, -7B	860 760	mA	CKE ≥ VIH, tRC = tRC (min.)	1, 2, 9
Operating current (ACTV-READ-PRE)	IDD1	-6B -7A, -7B	1100 940	mA	CKE ≥ VIH, BL = 4, CL = 2.5, tRC = tRC (min.)	1, 2, 5
Idle power down standby current	IDD2P		24	mA	CKE ≤ VIL	4
Floating idle standby current	IDD2F	-6B -7A, -7B	240 200	mA	CKE ≥ VIH, /CS ≥ VIH, DQ, DQS, DM = VREF	4, 5
Quiet idle standby current	IDD2Q		160	mA	CKE ≥ VIH, /CS ≥ VIH, DQ, DQS, DM = VREF	4, 10
Active power down standby current	IDD3P		160	mA	CKE ≤ VIL	3
Active standby current	IDD3N	-6B -7A, -7B	520 440	mA	CKE ≥ VIH, /CS ≥ VIH tRAS = tRAS (max.)	3, 5, 6
Operating current (Burst read operation)	IDD4R	-6B -7A, -7B	1340 1140	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Operating current (Burst write operation)	IDD4W	-6B -7A, -7B	1340 1140	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Auto refresh current	IDD5	-6B -7A, -7B	1540 1420	mA	tRFC = tRFC (min.), Input ≤ VIL or ≥ VIH	
Self refresh current	IDD6		32	mA	Input ≥ VDD – 0.2 V Input ≤ 0.2 V	
Operating current (4 banks interleaving)	IDD7A	-6B -7A, -7B	2380 2020	mA	BL = 4	1, 5, 6, 7

Notes. 1. These IDD data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. DQ, DM, DQS transition twice per one cycle.
7. 4 banks active. Only one bank is running at tRC = tRC (min.)
8. The IDD data on this table are measured with regard to tCK = tCK (min.) in general.
9. Command/Address transition once every two clock cycles.
10. Command/Address stable at ≥ VIH or ≤ VIL.

DC Characteristics 2 (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Note
Input leakage current	ILI	–16	16	µA	VDD ≥ VIN ≥ VSS	
Output leakage current	ILO	–10	10	µA	VDD ≥ VOUT ≥ VSS	
Output high current	IOH	–15.2	—	mA	VOUT = 1.95V	1
Output low current	IOL	15.2	—	mA	VOUT = 0.35V	1

Note: 1. DDR SDRAM component specification.

Pin Capacitance (TA = 25°C, VDD = 2.5V ± 0.2V)

Parameter	Symbol	Pins	max.	Unit	Note
Input capacitance	CI1	Address, /RAS, /CAS, /WE	60	pF	
Input capacitance	CI2	CK, /CK, CKE, /CS	50	pF	
Data and DQS input/output capacitance	CO	DQ, DQS, DM	20	pF	

AC Characteristics (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)

(DDR SDRAM Component Specification)

		-6B		-7A		-7B			
Parameter	Symbol	min.	max.	min.	max.	min.	max	Unit	Notes
Clock cycle time (CL = 2)	tCK	7.5	12	7.5	12	10	12	ns	10
(CL = 2.5)	tCK	6	12	7.5	12	7.5	12	ns	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min (tCH, tCL)	—	min (tCH, tCL)	—	min (tCH, tCL)	—	tCK	
DQ output access time from CK, /CK	tAC	–0.7	0.7	–0.75	0.75	–0.75	0.75	ns	2, 11
DQS output access time from CK, /CK	tDQSCK	–0.6	0.6	–0.75	0.75	–0.75	0.75	ns	2, 11
DQS to DQ skew	tDQSQ	—	0.45	—	0.5	—	0.5	ns	3
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	tHP – tQHS	—	tHP – tQHS	—	ns	
Data hold skew factor	tQHS	—	0.55	—	0.75	—	0.75	ns	
Data-out high-impedance time from CK, /CK	tHZ	–0.7	0.7	–0.75	0.75	–0.75	0.75	ns	5, 11
Data-out low-impedance time from CK, /CK	tLZ	–0.7	0.7	–0.75	0.75	–0.75	0.75	ns	6, 11
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQ and DM input setup time	tDS	0.45	—	0.5	—	0.5	—	ns	8
DQ and DM input hold time	tDH	0.45	—	0.5	—	0.5	—	ns	8
DQ and DM input pulse width	tDIPW	1.75	—	1.75	—	1.75	—	ns	7
Write preamble setup time	tWPRES	0	—	0	—	0	—	ns	
Write preamble	tWPRE	0.25	—	0.25	—	0.25	—	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	9
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	0.2	—	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	0.2	—	0.2	—	tCK	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	0.35	—	tCK	
Address and control input setup time	tIS	0.75	—	0.9	—	0.9	—	ns	8
Address and control input hold time	tIH	0.75	—	0.9	—	0.9	—	ns	8
Address and control input pulse width	tIPW	2.2	—	2.2	—	2.2	—	ns	7

Parameter	Symbol	-6B min.	-6B max.	-7A min.	-7A max.	-7B min.	-7B max	Unit	Notes
Mode register set command cycle time	tMRD	2	—	2	—	2	—	tCK	
Active to Precharge command period	tRAS	42	120000	45	120000	45	120000	ns	
Active to Active/Auto refresh command period	tRC	60	—	65	—	65	—	ns	
Auto refresh to Active/Auto refresh command period	tRFC	72	—	75	—	75	—	ns	
Active to Read/Write delay	tRCD	18	—	20	—	20	—	ns	
Precharge to active command period	tRP	18	—	20	—	20	—	ns	
Active to Autoprecharge delay	tRAP	tRCD min.	—	tRCD min.	—	tRCD min.	—	ns	
Active to active command period	tRRD	12	—	15	—	15	—	ns	
Write recovery time	tWR	15	—	15	—	15	—	ns	
Auto precharge write recovery and precharge time	tDAL	(tWR/tCK)+ (tRP/tCK)	—	(tWR/tCK)+ (tRP/tCK)	—	(tWR/tCK)+ (tRP/tCK)	—	tCK	13
Internal write to Read command delay	tWTR	1	—	1	—	1	—	tCK	
Average periodic refresh interval	tREF	—	7.8	—	7.8	—	7.8	µs	

Notes: 1. All the AC parameters listed in this data sheet is component specifications. For AC testing conditions, refer to the corresponding component data sheet.

2. This parameter defines the signal transition delay from the cross point of CK and /CK. The signal transition is defined to occur when the signal level crossing VTT.
3. The timing reference level is VTT.
4. Output valid window is defined to be the period between two successive transition of data out or DQS (read) signals. The signal transition is defined to occur when the signal level crossing VTT.
5. tHZ is defined as DOUT transition delay from Low-Z to High-Z at the end of read burst operation. The timing reference is cross point of CK and /CK. This parameter is not referred to a specific DOUT voltage level, but specify when the device output stops driving.
6. tLZ is defined as DOUT transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is not referred to a specific DOUT voltage level, but specify when the device output begins driving.
7. Input valid windows is defined to be the period between two successive transition of data input or DQS (write) signals. The signal transition is defined to occur when the signal level crossing VREF.
8. The timing reference level is VREF.
9. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
10. tCK (max.) is determined by the lock range of the DLL. Beyond this lock range, the DLL operation is not assured.
11. tCK = tCK (min.) when these parameters are measured. Otherwise, absolute minimum values of these values are 10% of tCK.
12. VDD is assumed to be 2.5V ± 0.2V. VDD power supply variation per cycle expected to be less than 0.4V/400 cycle.
13. tDAL = (tWR/tCK)+(tRP/tCK)

    For each of the terms above, if not already an integer, round to the next highest integer.

    Example: For –7A Speed at CL = 2.5, tCK = 7.5ns, tWR = 15ns and tRP= 20ns,

    tDAL = (15ns/7.5ns) + (20ns/7.5ns) = (2) + (3)

    tDAL = 5 clocks

Timing Parameter Measured in Clock Cycle for unbuffered DIMM

		Number of clock cycle				
tCK		6ns		7.5ns		
Parameter	Symbol	min.	max.	min.	max.	Unit
Write to pre-charge command delay (same bank)	tWPD	4 + BL/2	—	3 + BL/2	—	tCK
Read to pre-charge command delay (same bank)	tRPD	BL/2	—	BL/2	—	tCK
Write to read command delay (to input all data)	tWRD	2 + BL/2	—	2 + BL/2	—	tCK
Burst stop command to write command delay (CL = 2)	tBSTW	—	—	2	—	tCK
(CL = 2.5)	tBSTW	3	—	3	—	tCK
Burst stop command to DQ High-Z (CL = 2)	tBSTZ	—	—	2	2	tCK
(CL = 2.5)	tBSTZ	2.5	2.5	2.5	2.5	tCK
Read command to write command delay (to output all data) (CL = 2)	tRWD	—	—	2 + BL/2	—	tCK
(CL = 2.5)	tRWD	3 + BL/2	—	3 + BL/2	—	tCK
Pre-charge command to High-Z (CL = 2)	tHZP	—	—	2	2	tCK
(CL = 2.5)	tHZP	2.5	2.5	2.5	2.5	tCK
Write command to data in latency	tWCD	1	1	1	1	tCK
Write recovery	tWR	3		2	—	tCK
DM to data in latency	tDMD	0	0	0	0	tCK
Mode register set command cycle time	tMRD	2	—	2	—	tCK
Self refresh exit to non-read command	tSNR	12	—	10	—	tCK
Self refresh exit to read command	tSRD	200	—	200	—	tCK
Power down entry	tPDEN	1	1	1	1	tCK
Power down exit to command input	tPDEX	1	—	1	—	tCK

Pin Functions

CK, /CK (input pin)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK.

/CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY9) is loaded via the A0 to the A9 at the cross point of the CK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are precharged. If A10 = low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = high when read or write command, auto-precharge function is enabled. While A10 = low, auto-precharge function is disabled.

BA0, BA1 (input pin)

BA0, BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven low and exited when it resumes to high.

The CKE level must be kept for 1 CK cycle at least, that is, if CKE changes at the cross point of the CK rising edge and the VREF level with proper setup time tIS, at the next CK rising edge CKE level must be kept with proper hold time tIH.

DQ (input and output pins)

Data are input to and output from these pins.

DQS (input and output pin)

DQS provide the read data strobes (as output) and the write data strobes (as input).

DM (input pins)
DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and VREF

VDD (power supply pins)
2.5V is applied (VDD is for the internal circuit).

VDDSPD (power supply pin)
2.5V is applied (For serial EEPROM).

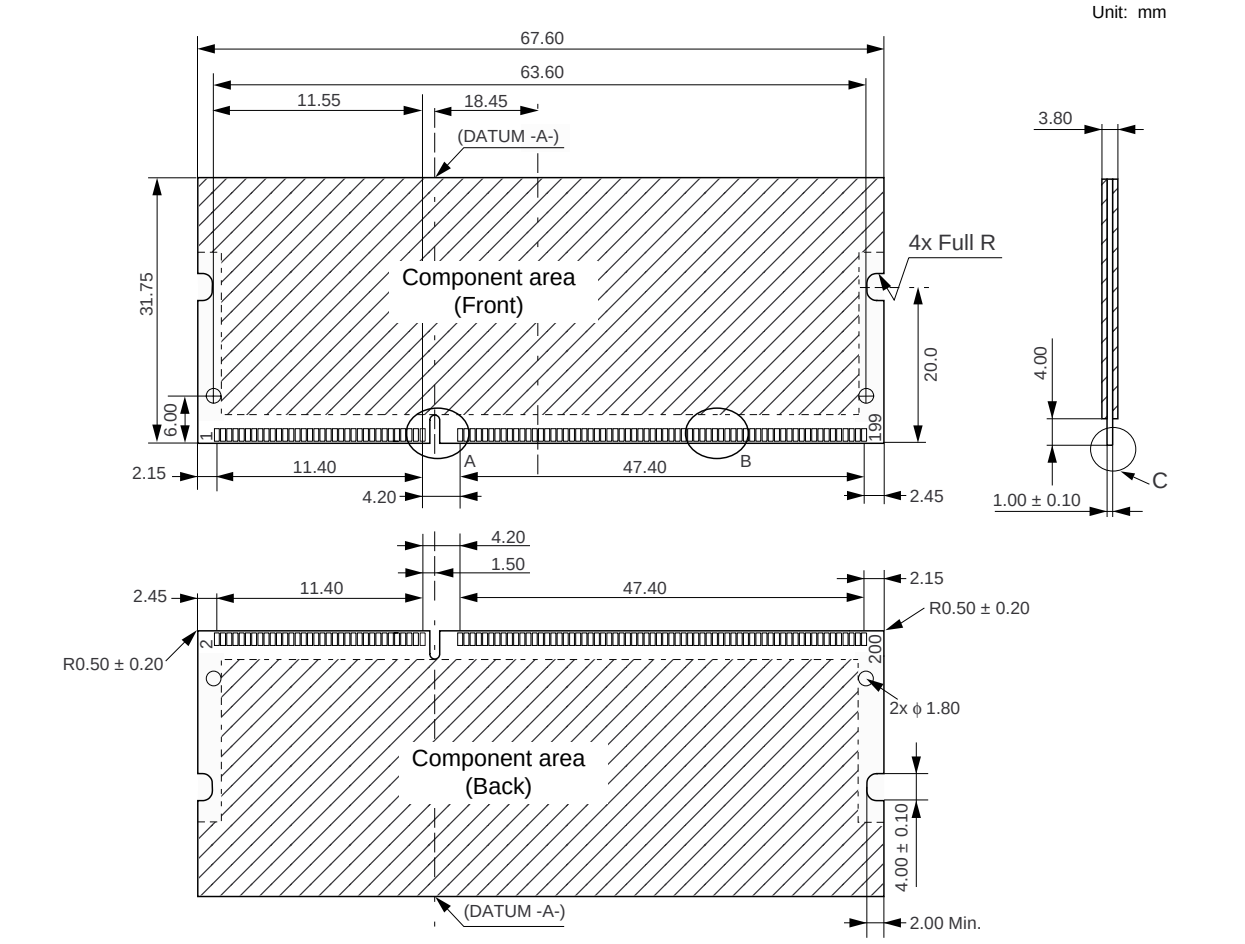
VSS (power supply pin)
Ground is connected.

Detailed Operation Part and Timing Waveforms

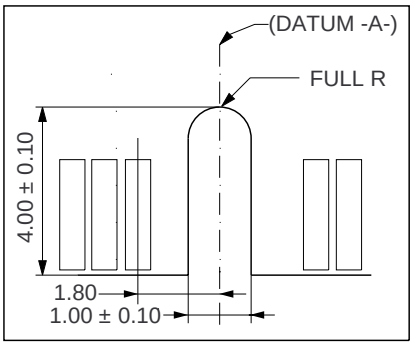
Refer to the EDD5104ADTA-E, EDD5108ADTA-E, EDD5116ADTA-E datasheet (E0501E).

Physical Outline

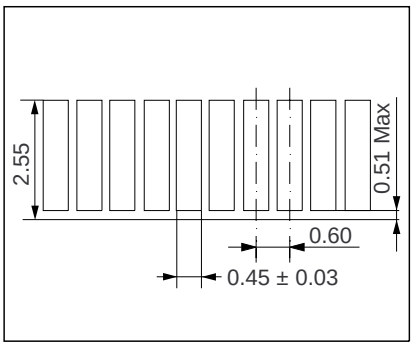
Unit: mm



Detail A



Detail B



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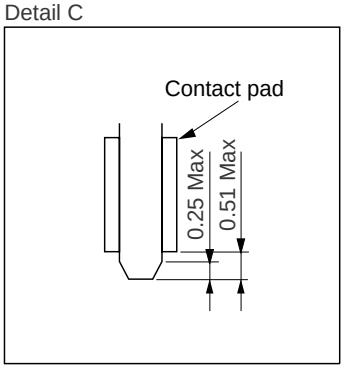

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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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