E3M0040120K

Silicon Carbide Power MOSFET
E-Series Automotive
N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

Benefits

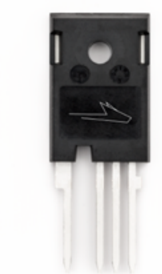
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

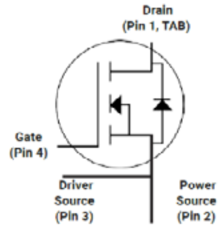
Typical Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

Package

Tab
Drain





Part Number	Package	Marking
E3M0040120K	TO-247-4L	E3M0040120K

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter		Value	Unit	Note
V_{DSmax}	Drain - Source Voltage		1200	V	
V_{GSmax}	Gate - Source Voltage		-8/+19	V	Note: 1
I_D	Continuous Drain Current, V_{GS} = 15 V	T_C = 25˚C	57	A	Fig. 19 Note: 2
		T_C = 100˚C	41		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_P limited by T_{jmax}		128	A	Fig. 22
P_D	Power Dissipation, T_C=25˚C, T_J = 175 ˚C		242	W	Fig. 20 Note: 2
T_J , T_{stg}	Operating Junction and Storage Temperature		-55 to +175	˚C	
T_L	Solder Temperature, 1.6mm (0.063”) from case for 10s		260	˚C	
M_d	Mounting Torque , M3 or 6-32 screw		1 8.8	Nm lbf-in	

Note (1): Recommended turn off / turn on gate voltage V_{GS} - 4V...0V / +15V
Note (2): Verified by design

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.7	3.6	V	V_{DS} = V_{GS}, I_D = 8.77 mA	Fig. 11
			2.2		V	V_{DS} = V_{GS}, I_D = 8.77 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		39	53	mΩ	V_{GS} = 15 V, I_D = 31.9 A	Fig. 4, 5, 6
			70			V_{GS} = 15 V, I_D = 31.9 A, T_J = 175ºC	
g_{fs}	Transconductance		22		S	V_{DS}= 20 V, I_{DS}= 31.9 A	Fig. 7
			20			V_{DS}= 20 V, I_{DS}= 31.9 A, T_J = 175ºC	
C_{iss}	Input Capacitance		2726		pF	V_{GS} = 0 V, V_{DS} = 0V to 1000 V F = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		100				
C_{rss}	Reverse Transfer Capacitance		6				
E_{oss}	C_{oss} Stored Energy		56		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		127		pF	V_{GS} = 0 V, V_{DS} = 0... 800V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		197		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		300		μJ	V_{DS}= 800 V, V_{GS}= -4 V/15 V, I_D= 31.9 A, $R_{G(ext)}$ = 2.5 Ω, L= 98 μH, T_J = 175ºC FWD = External SiC DIODE	Fig. 26, 28
E_{OFF}	Turn Off Switching Energy (External Diode)		73				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		658		μJ	V_{DS}= 800 V, V_{GS}= -4 V/15 V, I_D= 31.9 A, $R_{G(ext)}$ = 2.5 Ω, L= 98 μH, T_J = 175ºC FWD = Internal Body Diode	Fig. 26, 28
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		74				
$t_{d(on)}$	Turn-On Delay Time		13		ns	V_{DD} = 800 V, V_{GS} = -4 V/15 V I_D = 31.9 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		16				
$t_{d(off)}$	Turn-Off Delay Time		23				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		2.2		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		32		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 31.9 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		28				
Q_g	Total Gate Charge		94				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 800V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 800V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	V_{GS} = -4 V, I_{SD} = 15.95 A, T_J = 25 °C	Fig. 8, 9, 10
		4.3		V	V_{GS} = -4 V, I_{SD} = 15.95 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		43	A	V_{GS} = -4 V, T_C = 25˚C	
$I_{S, pulse}$	Diode pulse Current		128	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	18		ns	V_{GS} = -4 V, I_{SD} = 31.9 A, V_R = 800 V dif/dt = 8350 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	811		nC		
I_{rrm}	Peak Reverse Recovery Current	79		A		
t_{rr}	Reverse Recover time	32		ns	V_{GS} = -4 V, I_{SD} = 31.9 A, V_R = 800 V dif/dt = 2250 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	603		nC		
I_{rrm}	Peak Reverse Recovery Current	30		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.46	0.62	°C/W		Fig. 21

Typical Performance

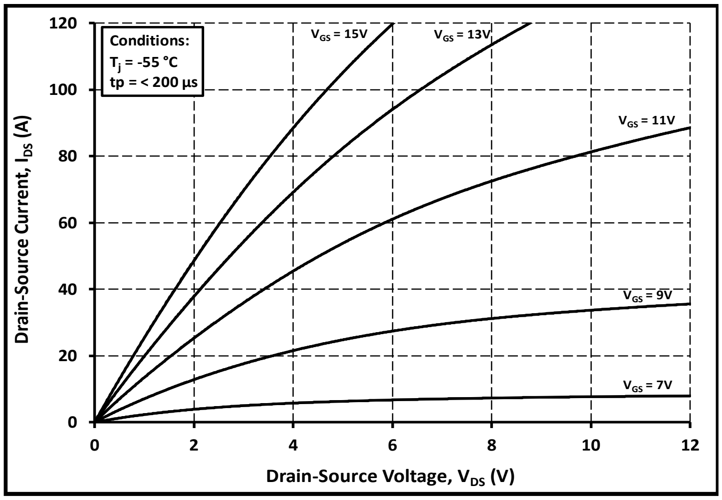


Figure 1. Output Characteristics T_J = -55 °C

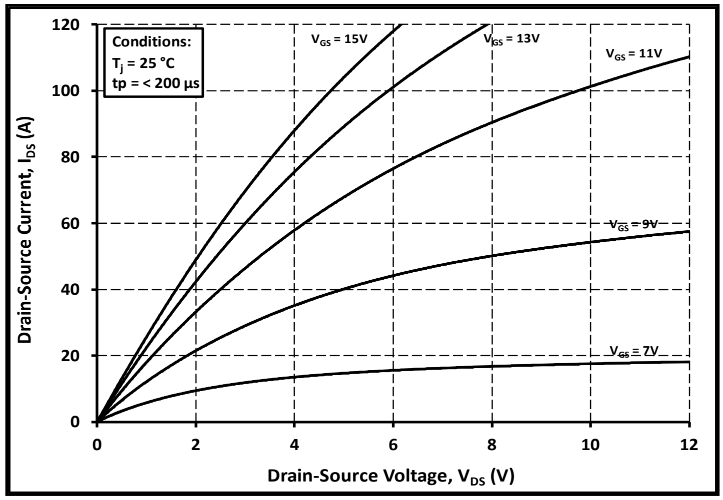


Figure 2. Output Characteristics T_J = 25 °C

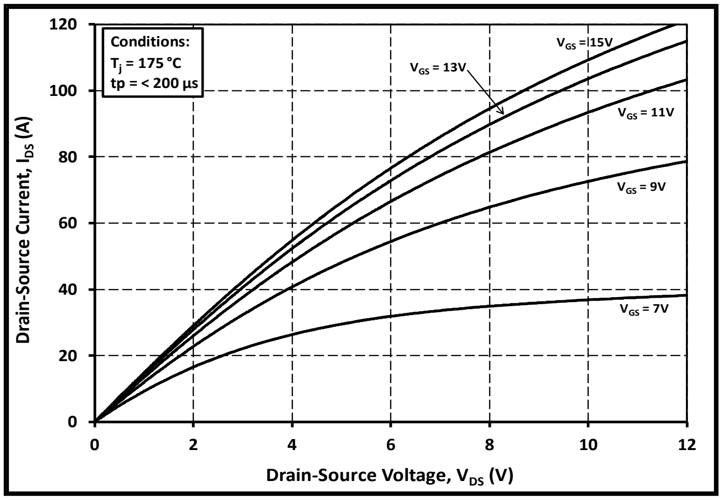


Figure 3. Output Characteristics T_J = 175 °C

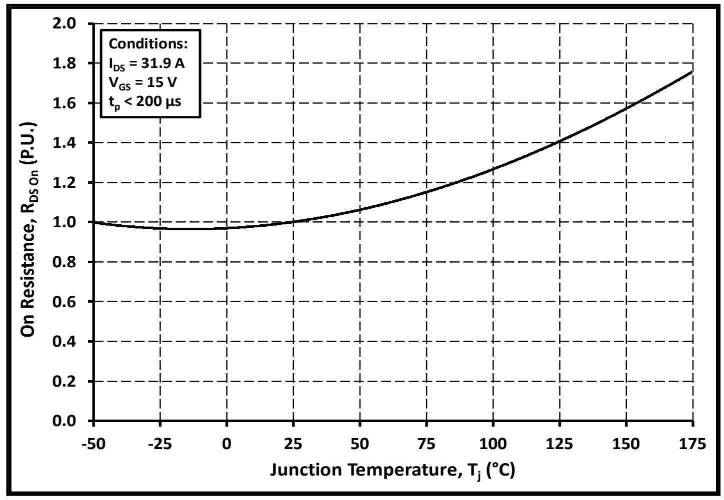


Figure 4. Normalized On-Resistance vs. Temperature

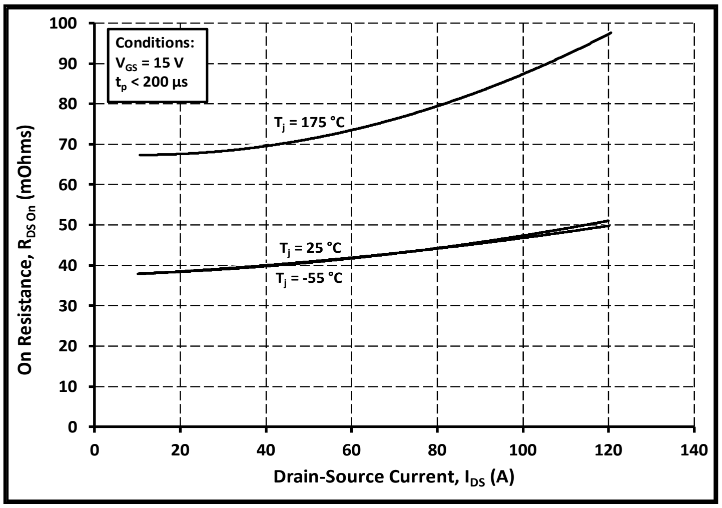


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

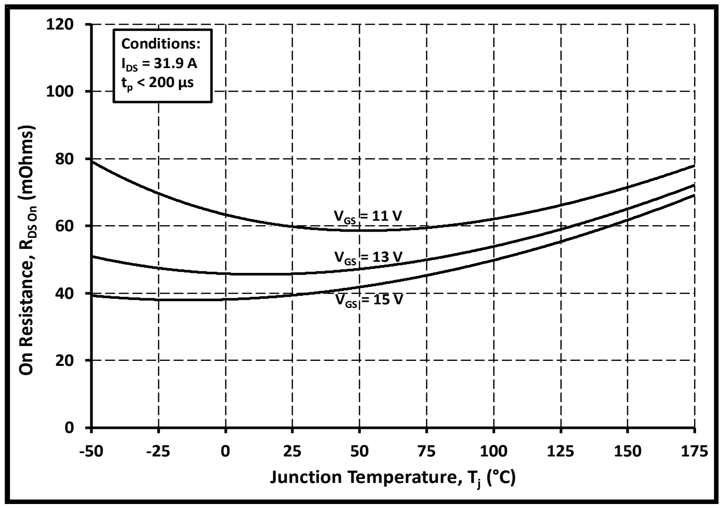


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

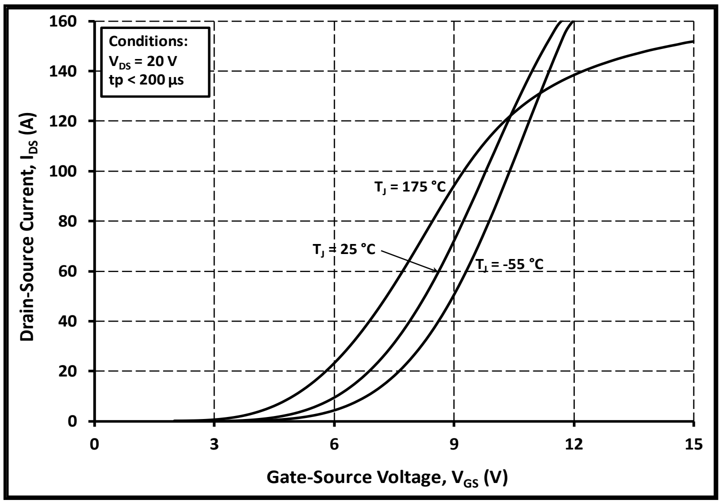


Figure 7. Transfer Characteristic for Various Junction Temperatures

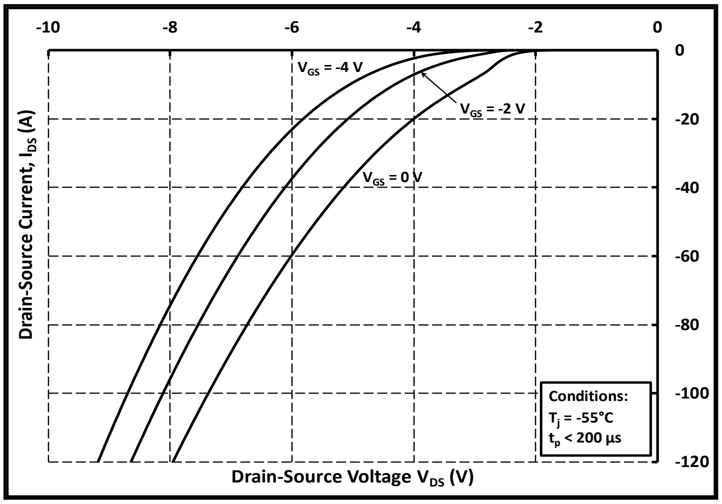


Figure 8. Body Diode Characteristic at -55 ºC

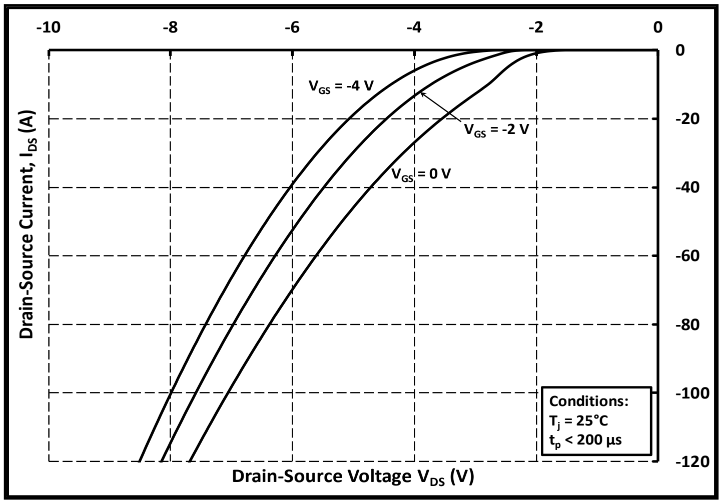


Figure 9. Body Diode Characteristic at 25 ºC

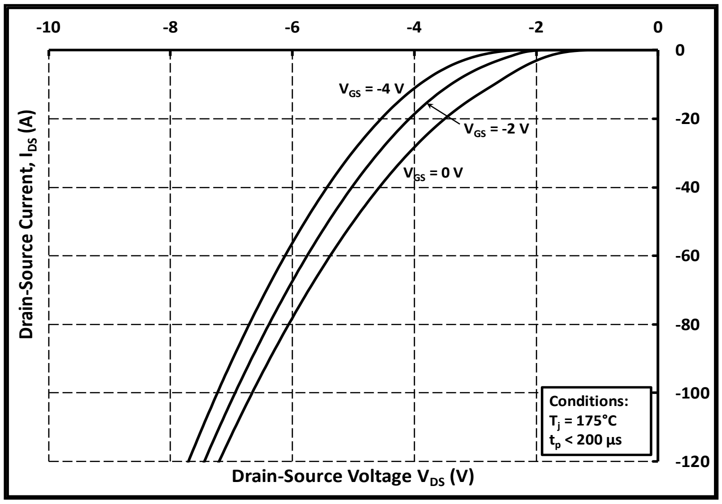


Figure 10. Body Diode Characteristic at 175 ºC

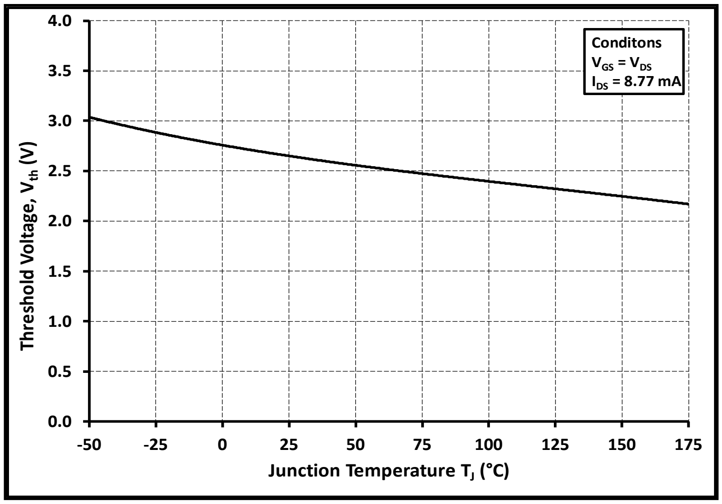


Figure 11. Threshold Voltage vs. Temperature

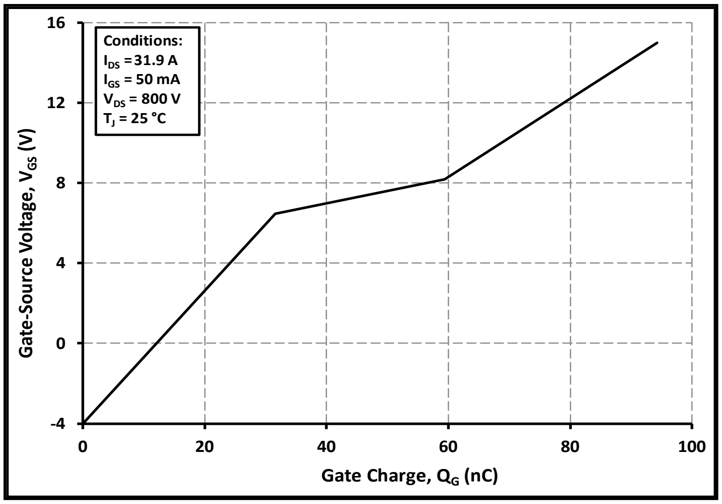


Figure 12. Gate Charge Characteristics

Typical Performance

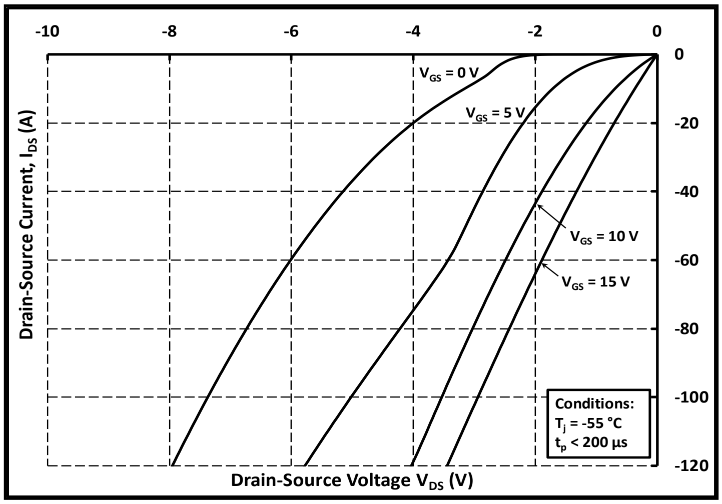


Figure 13. 3rd Quadrant Characteristic at -55 °C

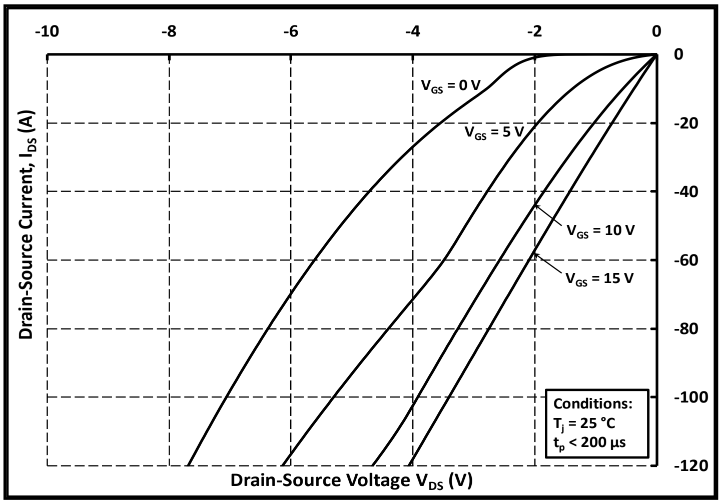


Figure 14. 3rd Quadrant Characteristic at 25 °C

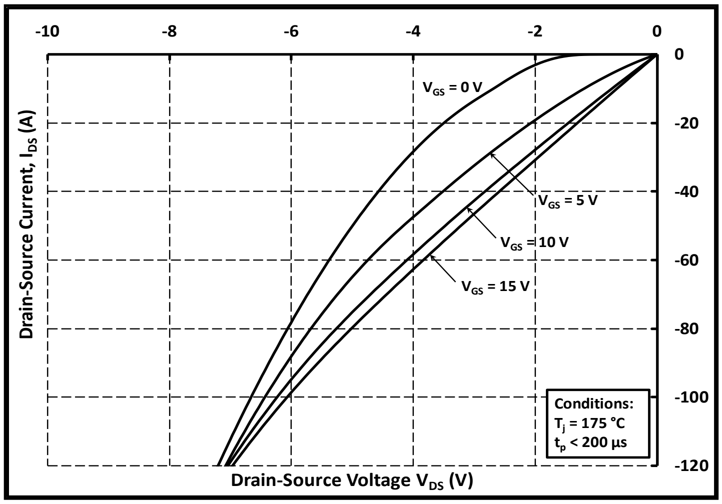


Figure 15. 3rd Quadrant Characteristic at 175 °C

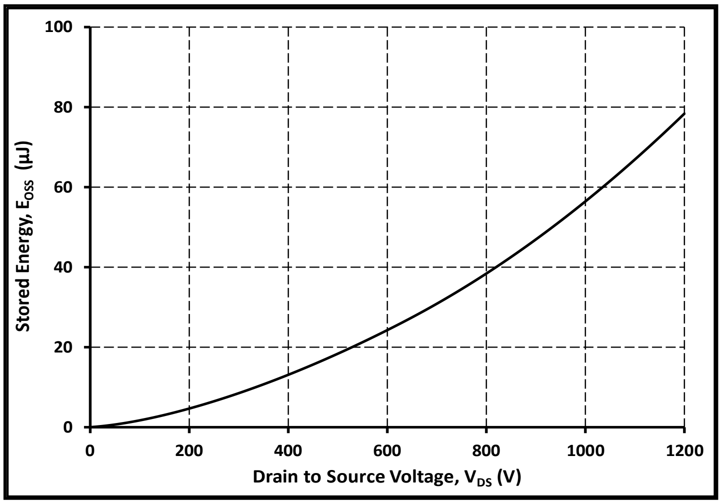


Figure 16. Output Capacitor Stored Energy

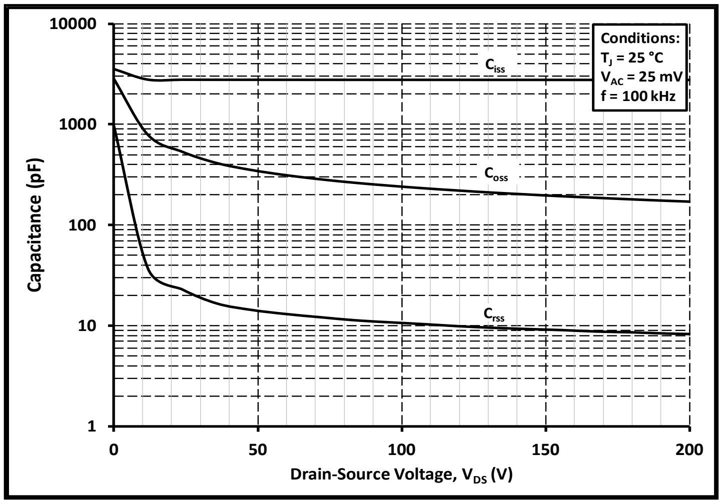


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

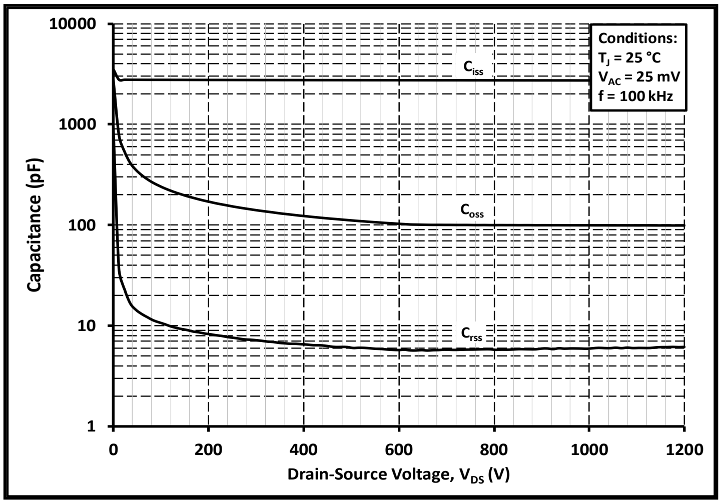


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

Typical Performance

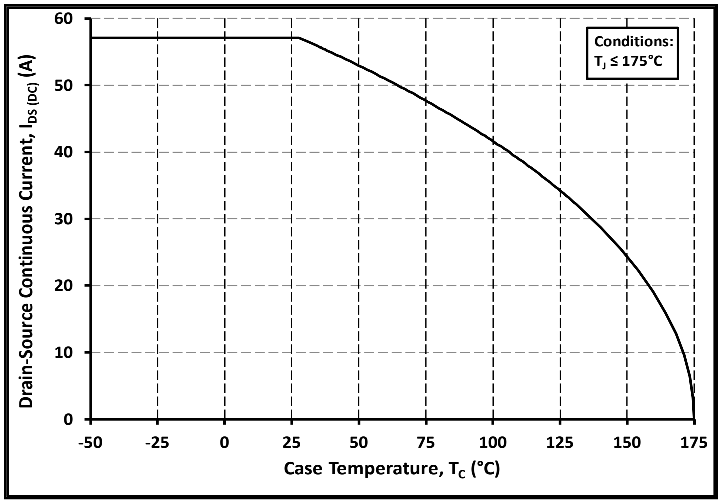


Figure 19. Continuous Drain Current Derating vs. Case Temperature

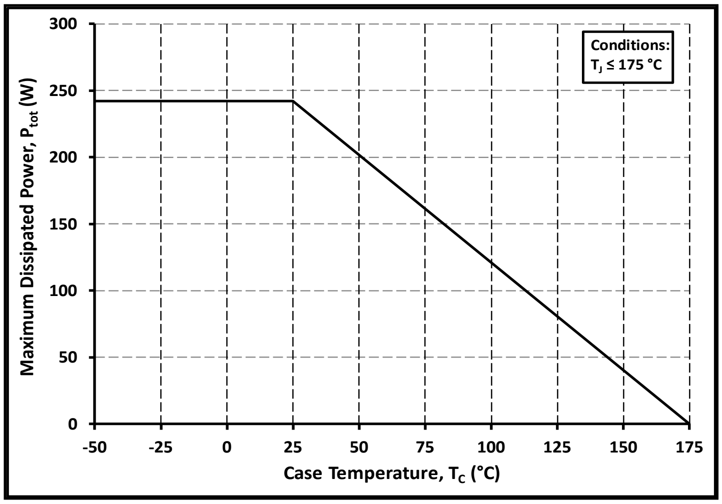


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

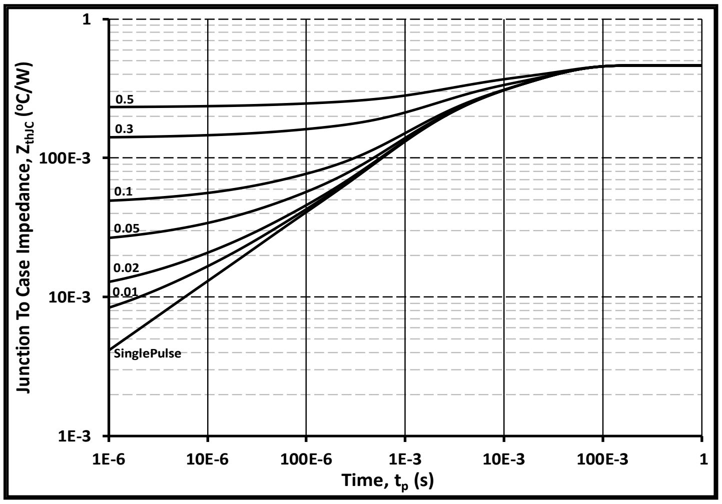


Figure 21. Transient Thermal Impedance (Junction - Case)

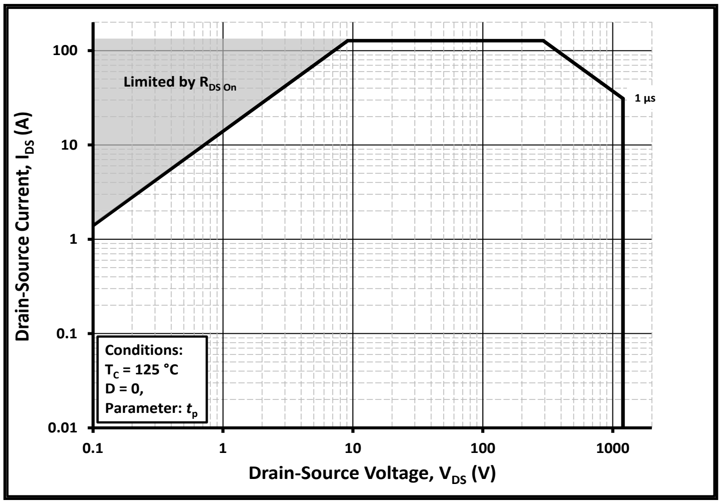


Figure 22. Safe Operating Area

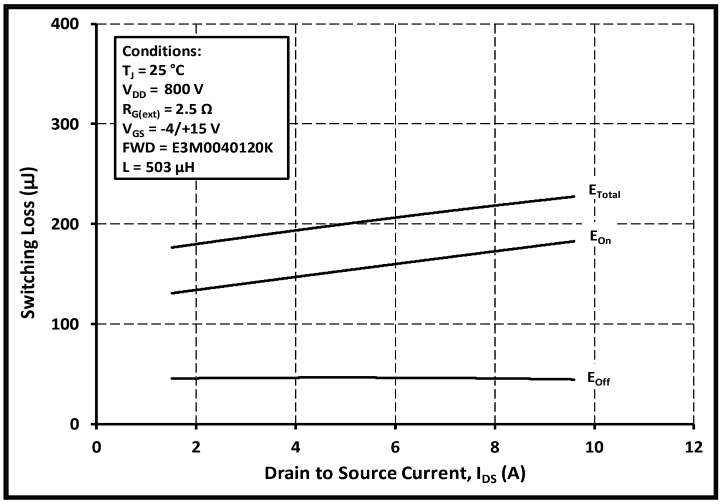


Figure 23. Clamped Inductive Switching Energy vs. Low Drain Current (V_{DD} = 800V)

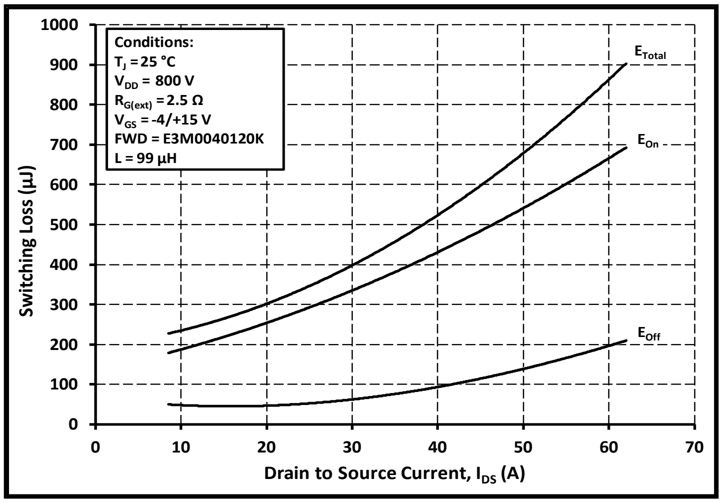


Figure 24. Clamped Inductive Switching Energy vs. High Drain Current (V_{DD} = 800V)

Typical Performance

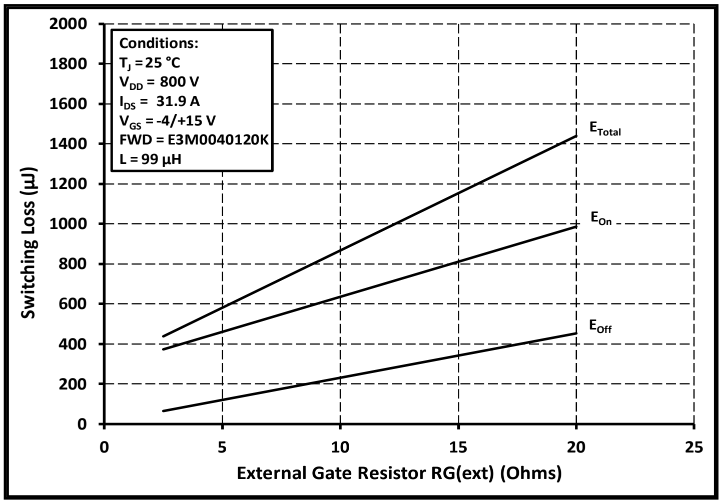


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

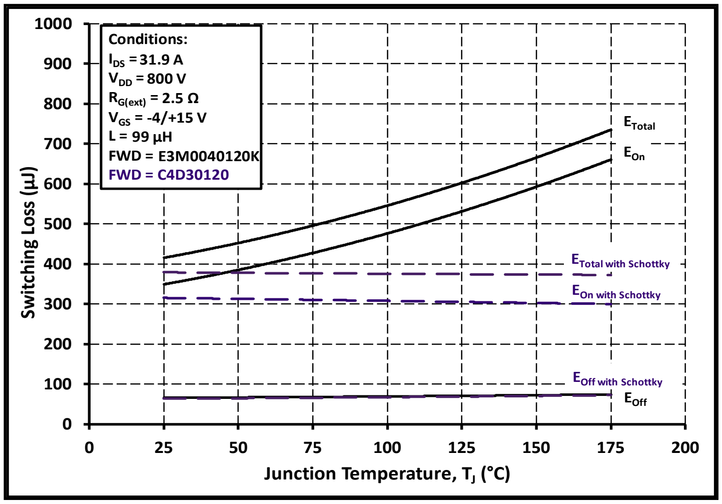


Figure 26. Clamped Inductive Switching Energy vs. Temperature

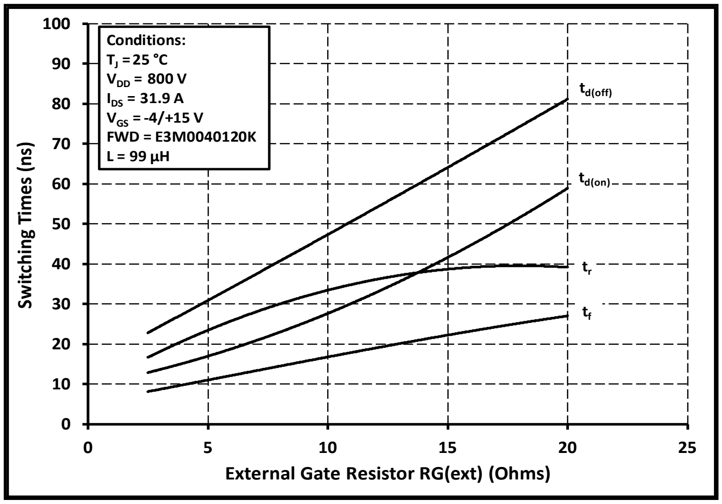


Figure 27. Switching Times vs. $R_{G(ext)}$

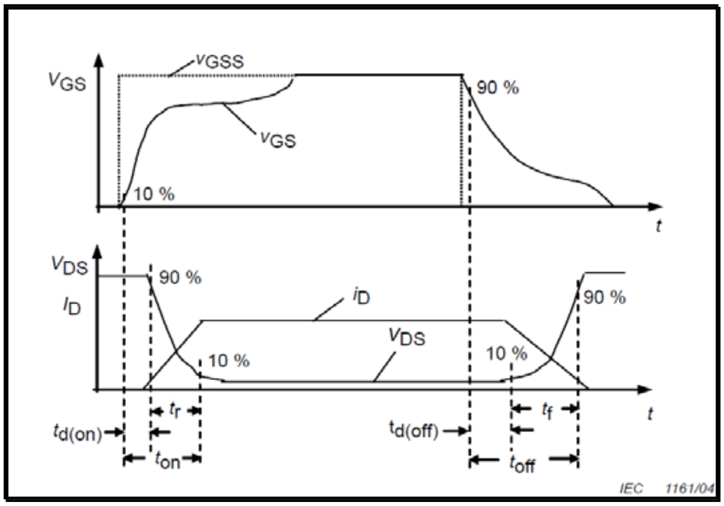


Figure 28. Switching Times Definition

Test Circuit Schematic

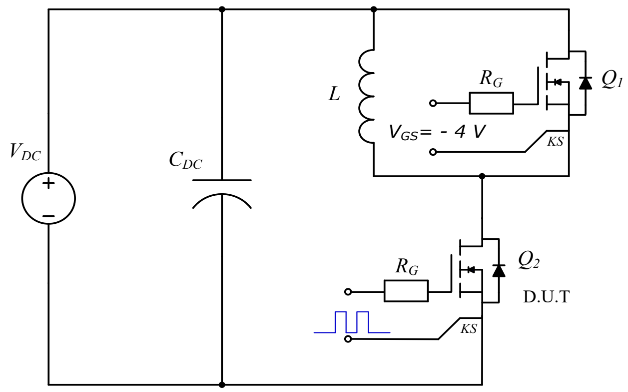


Figure 29. Clamped Inductive Switching Waveform Test Circuit

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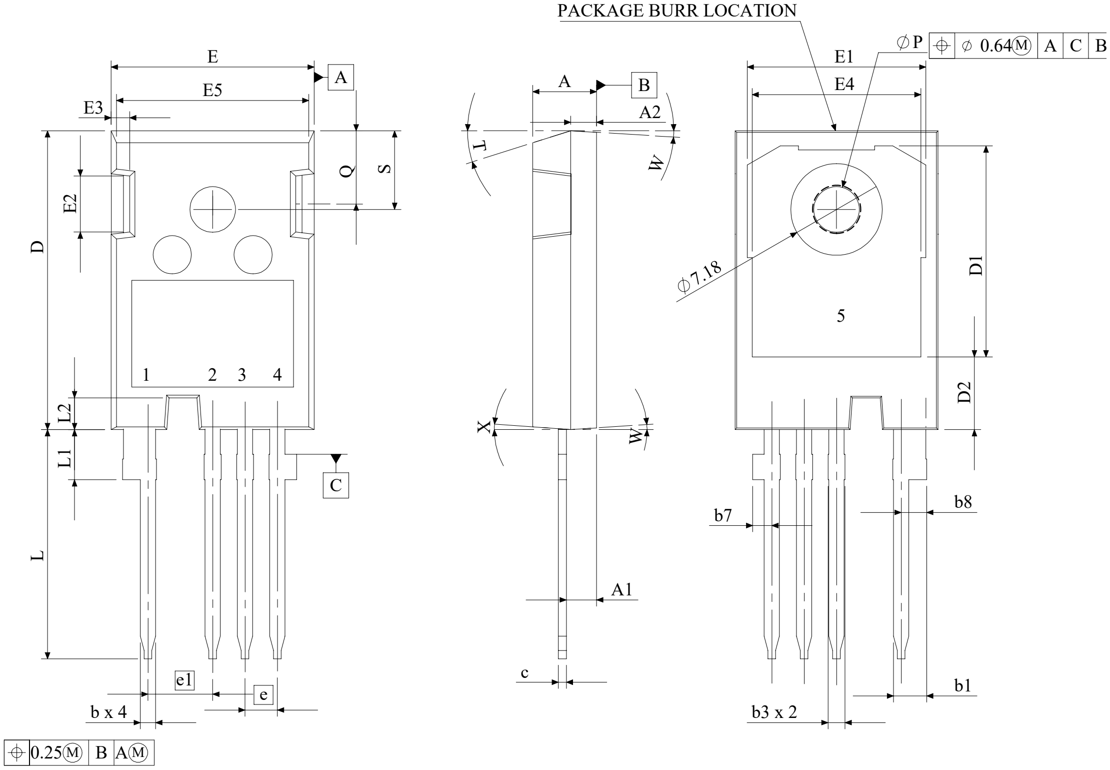
Package Dimensions

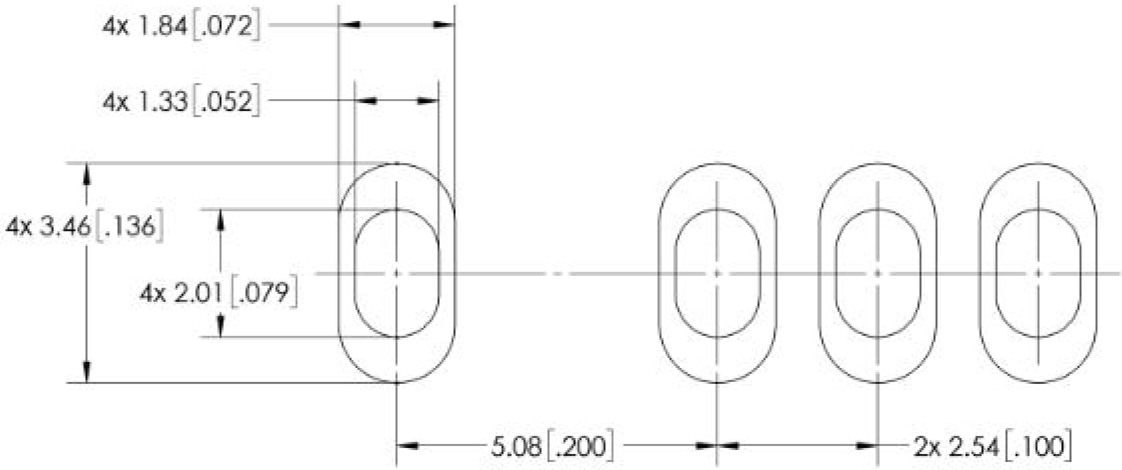


SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.23	2.54
A2	1.91	2.16
b	1.07	1.33
b1	2.39	2.94
b3	1.07	1.60
b7	1.30	1.70
b8	1.80	2.20
c	0.55	0.68
D	23.30	23.63
D1	16.25	17.65
D2	5.55	5.95
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
E5	14.65	15.05
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
∅P	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	DRIVER SOURCE
4	GATE
5	DRAIN

NOTE:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Recommended Solder Pad Layout



Revision history

Document Version	Date of release	Descriptiion of changes
1.0	November-2022	Initial datasheet
2	January - 2025	Legal Disclaimer Updated
3	March - 2025	Removed V_{AC} from $R_{G(int)}$ test condition Updated Fig 22

Notes & Disclaimer

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REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power

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