Digital Controlled Variable Gain Amplifier DVGA1-242PP+

50Ω 0.45 to 2.4 GHz
31.5 dB, 0.5 dB Step, 6 Bit Parallel Control

The Big Deal

- Integrated Amplifier and Digital Attenuator
- 30 dB Gain / 31.5 dB Gain Control
- High Output IP3, 34-37 dBm

CASE STYLE: DG1677

Product Overview

The DVGA1-242PP+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit parallel interface attenuator and 30dB gain using a E-PHEMT amplifier. Step attenuator used in DVGA1-242PP+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Key Features

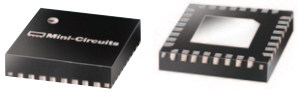
Feature	Advantages
31.5 dB attenuation in 0.5 dB step size	Combining high gain and a wide range of gain control makes the DVGA1-242PP+ an ideal building block for any RF chain where level setting control is required in fast speed of parallel control interface.
High Gain, 30 dB	Incorporating multiple stages of amplification, the DVGA1-242PP+ provides high gain reducing cost and PCB board space
High IP3, +34 dBm at 1.0 GHz Low Noise Figure, 2.5 dB at 1.0 GHz	Combining Low Noise and High IP3 makes this MMIC amplifier ideal for Low Noise Receiver Front End (RFE) giving the user advantages at both ends of the dynamic range: sensitivity & two-tone IM dynamic range.
Output Power, +23 dBm at 2.4 GHz	The DVGA1-242PP+ maintains consistent output power capability over the full operating temperature range making it ideal to be used in remote applications such as LNB's as the L Band driver stage.
MCLP Package	Low Inductance, repeatable transitions, excellent thermal pad.
Max Input Power, +24 dBm	Ruggedized design operates up to input powers often seen at Receiver inputs.
Attenuation Step size, 0.5 dB, accuracy 0.1 dB typ. Total attenuation, 31.5 dB	Enables precise control of gain in 0.5 dB steps up to 31.5 dB.
External Jumper	Customer access is provided between the digital attenuator and the RF amplifier to allow the user to integrate external circuit elements if desired.

Digital Controlled Variable Gain Amplifier 50Ω 450-2400 MHz

30 dB Gain, 0.5 dB Step, 31.5 dB Attenuation,
6 Bit Parallel Control

Product Features

- 31.5 dB Gain control 0.5dB step size
- Gain, 30 dB nominal at 0dB attenuation and 1 GHz
- Excellent accuracy, 0.1 dB typ
- Parallel control interface
- Small size 5.0 x 5.0 mm



DVGA1-242PP+

CASE STYLE: DG1677
PRICE: $6.95 ea. QTY. (20)

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Typical Applications

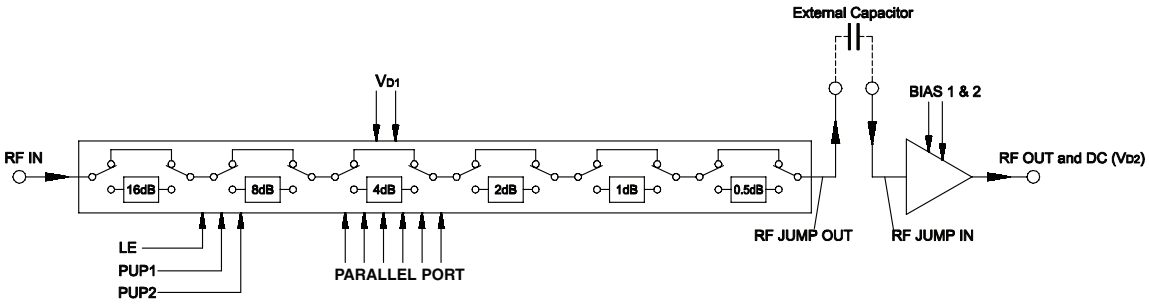
- Base Station Infrastructure
- GPS
- LTE
- WCDMA

General Description

The DVGA1-242PP+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit parallel interface attenuator and 30dB gain using a E-PHEMT amplifier. Step attenuator used in DVGA1-242PP+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic

(Refer to Table 1 for Pad description)



RF Electrical Specifications[1] at 25°C, 50Ω With V_{D1}=+3.0V, V_{D2}=+5V

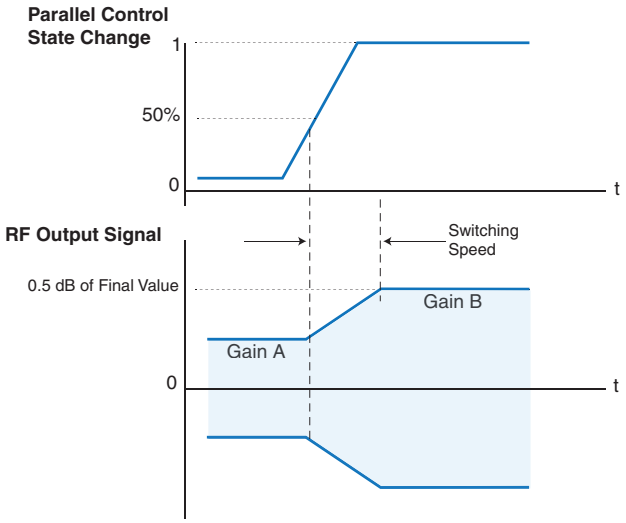
Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		0.45		2.4	GHz
Gain (at 0 dB attenuation)	.45	—	29.0	—	dB
	1.0	—	30.3	—	
	1.4	26.5	29.5	32.4	
	2.0	—	24.4	—	
	2.4	—	21.0	—	
Input Return Loss (all states)	.45	—	15.4	—	dB
	1.0	—	15.1	—	
	1.4	—	9.5	—	
	2.0	—	9.5	—	
	2.4	—	14	—	
Output Return Loss (all states)	.45	—	19.5	—	dB
	1.0	—	12	—	
	1.4	—	10.7	—	
	2.0	—	9.5	—	
	2.4	—	9.0	—	
Output Power @ 1 dB compression (at min and max attenuation)	.45	—	22.5	—	dBm
	1.0	—	22.8	—	
	1.4	20.0	23.2	—	
	2.0	—	23.2	—	
	2.4	—	23.0	—	
Output IP3 (all states)	.45	—	35.2	—	dBm
	1.0	—	34.5	—	
	1.4	—	35.7	—	
	2.0	—	37.0	—	
	2.4	—	37.0	—	
Noise Figure (at 0 dB attenuation)	.45	—	3.8	—	dB
	1.0	—	2.5	—	
	1.4	—	3.1	3.7	
	2.0	—	3.4	—	
	2.4	—	3.5	—	
Accuracy @ **0.5 dB** Attenuation Setting	.45 - 1.0	—	0.05	0.12	dB
	1.0 - 2.4	—	0.08	0.18	
Accuracy @ **1 dB** Attenuation Setting	.45 - 1.0	—	0.04	0.13	dB
	1.0 - 2.4	—	0.11	0.2	
Accuracy @ **2 dB** Attenuation Setting	.45 - 1.0	—	0.12	0.25	dB
	1.0 - 2.4	—	0.24	0.37	
Accuracy @ **4 dB** Attenuation Setting	.45 - 1.0	—	0.19	0.37	dB
	1.0 - 2.4	—	0.27	0.45	
Accuracy @ **8 dB** Attenuation Setting	.45 - 1.0	—	0.22	0.4	dB
	1.0 - 2.4	—	0.37	0.7	
Accuracy @ **16 dB** Attenuation Setting	.45 - 1.0	—	0.32	0.6	dB
	1.0 - 2.4	—	0.88	1.2	

1. Measured in Mini-Circuits characterization test board TB-681+. See characterization Test Circuit (Fig. 2)

Attenuation Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	µSec
Switching Rep Rate	—	—	25	KHz

Figure 1. Switching Speed



DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{D1}	2.7	3.0	3.3	V
V_{D2}	4.75	5.0	5.25	V
Supply Current, I_{D1}*	—	—	100*	µA
I_{D2}	—	154	186	mA
Control Input Low**	—	—	0.3xV_{D1}	V
Control Input High**	0.7xV_{D1}	—	—	V
Control Current**	—	—	1	µA

*During turn-on and transition between attenuation states I_{D1} may increase up to 2mA

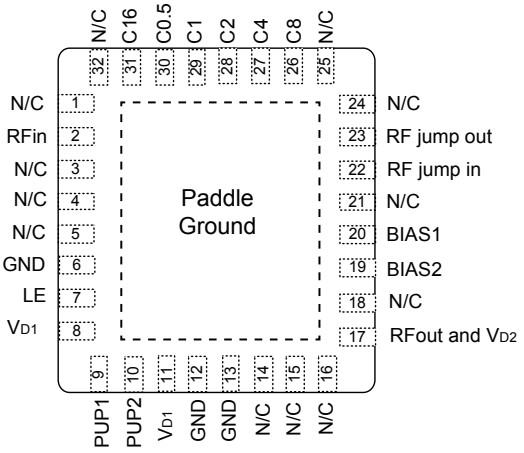
Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 150°C
V_{D1}	-0.3V Min., 4V Max.
V_{D2}	6.0V
Voltage on any control input**	-0.3V Min., V_{D1}+0.3V Max.
Input Power	+24dBm

**Data, clock or latch enable.
Permanent damage may occur if any of these limits are exceeded.

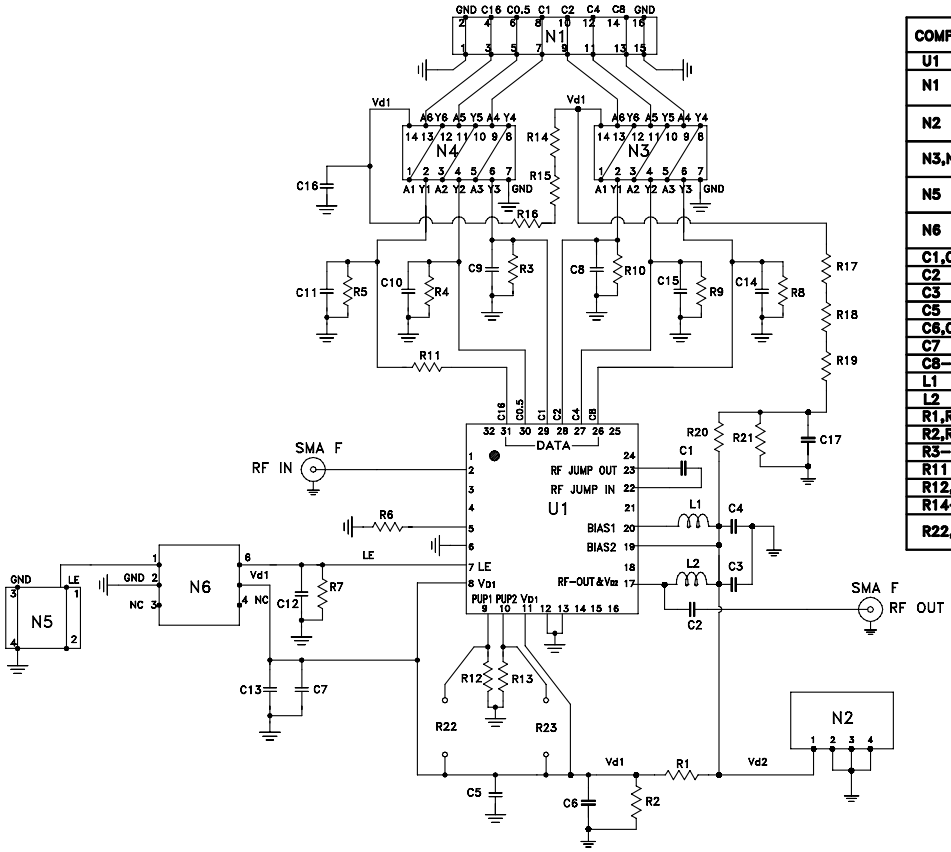
Table 1. Pad Description

Pin Number	Function	Description
1	N/C	Not Connected
2	RF IN	RF Input Port (Note 1)
3	N/C	Not Connected
4	N/C	Not Connected
5	N/C	Not Connected (Note 4)
6	GND	Ground
7	LE	Latch Enable Input (Note 2)
8	V_{D1}	V_{D1} Power Supply Input
9	PUP1	Power-up Selection
10	PUP2	Power-up Selection
11	V_{D1}	V_{D1} Power Supply Input
12	GND	Ground
13	GND	Ground
14	N/C	Not Connected
15	N/C	Not Connected
16	N/C	Not Connected
17	RF OUT &V_{D2}	RF output and V_{D2} on same pad (external Bias Tee) (Note1,6)
18	N/C	Not Connected
19	BIAS 2	Amplifier Bias 2 connects to V_{D2}
20	BIAS 1	Amplifier Bias 1 connects to V_{D2} via inductor(Note1,6)
21	N/C	Not Connected
22	RF JUMP IN	Interstage RF Jumper Input (Note 1)
23	RF JUMP OUT	Interstage RF Jumper Output (Note 1)
24	N/C	Not Connected
25	N/C	Not Connected
26	C8	Control for 8dB Att. Bit (Note 4)
27	C4	Control for 4dB Att. Bit (Note 4)
28	C2	Control for 2dB Att. Bit (Note 4)
29	C1	Control for 1dB Att. Bit (Note 4)
30	C0.5	Control for 0.5dB Att. Bit (Note 4)
31	C16	Control for 16dB Att. Bit (Note 3,4)
32	N/C	Not Connected
PADDLE	GND	Ground (Note5)



Notes:
1. All RF input and output ports shall be AC coupled with external blocking capacitor.
2. Latch Enable (LE) has an internal 100KΩ pull-up resistor to V_{D1}
3. Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance (see layout drawing PL-382).
4. Place a 10KΩ resistor to ground.
5. The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation
6. See application and characterization test circuit and layout drawing PL-382.

Application and Characterization Test Circuit

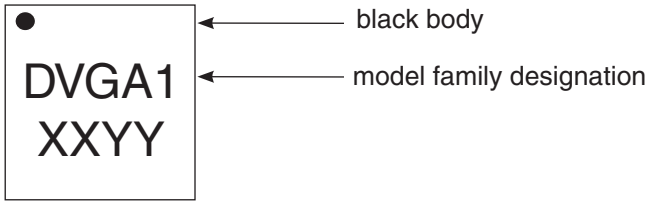


COMPONENT	VALUE/ PART NUMBER	SIZE
U1	DVGA1-242PP+	-
N1	CONNECTOR VERTICAL HEADER 16 POS	-
N2	CONNECTOR VERTICAL HEADER 4 POS	-
N3,N4	HEX INVERTING SCHMITT TRIGGER	-
N5	CONNECTOR VERTICAL HEADER 2 POS	-
N6	DUAL SCHMITT BUFFER/ INVERTER	-
C1,C4	100 pF	.04 X .02
C2	100 pF	.08 X .05
C3	1 uF	.08 X .05
C5	100 pF	.06 X .03
C6,C17	.47 uF	.06 X .03
C7	.1 uF	.08 X .05
C8-C16	100 pF	.06 X .03
L1	36 nH	.04 X .02
L2	47 nH	.04 X .02
R1,R20	475 Ohm	.06 X .03
R2,R21	681 Ohm	.06 X .03
R3-R10	10 KOhm	.06 X .03
R11	10 KOhm	.04 X .02
R12,R13	475 Ohm	.06 X .03
R14-R19	0 Ohm	.06 X .03
R22, R23	OPTIONAL PULL UP RESISTORS FOR PVP1 AND PVP2	.06 X .03

Conditions:
1. Gain: Pin=-25 dBm
2. Output IP3 (OIP3): two tones, spaced 1 MHz apart +5 dBm/ tone at output.
3. Schmitt trigger used in characterization circuit. Not required when application circuit includes recommended level settings.

Figure 2. Schematic of Test Circuit used for Characterization. (DUT soldered on Mini-Circuits Characterization Test Board TB-TBD+). Gain, output power at 1 dB compression (P1dB) Output IP3 (OIP3), Noise Figure are measured using Agilent's N5242A PNA-X Microwave Network Analyzer.

Product Marking



Simplified Schematic

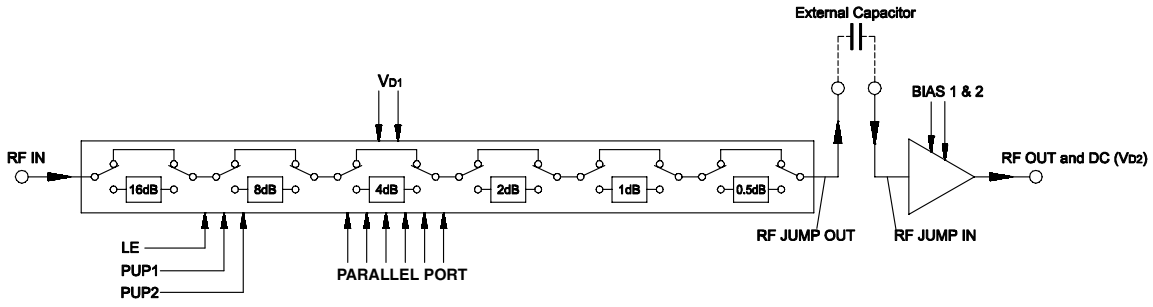


Figure 3. The DVGA1-242PP+ Parallel interface consists of 6 control bits that select the desired attenuation state, as shown in Table 2 Truth Table.

Table 2. Truth Table

Attenuation State	C16	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0	0
0.5 (dB)	0	0	0	0	0	1
1 (dB)	0	0	0	0	1	0
2 (dB)	0	0	0	1	0	0
4 (dB)	0	0	1	0	0	0
8 (dB)	0	1	0	0	0	0
16 (dB)	1	0	0	0	0	0
31.5 (dB)	1	1	1	1	1	1
Note: Not all 64 possible combinations of C0.5 - C16 are shown in table						

The parallel interface timing requirements are defined by Figure 4 (Parallel Interface Timing Diagram) and Table 3 (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

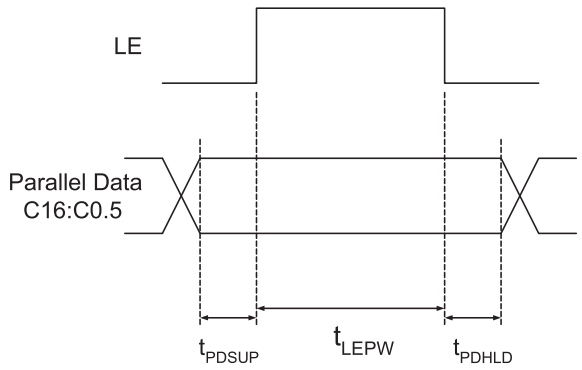


Figure 4. Parallel Interface Timing Diagram

Table 3. Parallel Interface AC Characteristics (V_{D1}=3V)

Symbol	Parameter	Min.	Max.	Units
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Parallel data set-up time before clock rising edge of LE	10		ns
t_{PDHLD}	Parallel data hold time after clock falling edge of LE	10		ns

Power-up Control Settings

The DVGA1-242PP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial parallel control word is provided. When the attenuator powers up with LE=0, the control bits are set to one of four possible values. These values are selected by the two power up control bits; PUP1 and PUP2, as shown in Table 4 (Power-Up Truth table, Parallel Mode)

Table 4 **Power-Up Truth Table, Parallel Mode**

Attenuation State	PUP1	PUP2	LE
Reference	0	0	0
8 (dB)	0	1	0
16 (dB)	1	0	0
31 (dB)	1	1	0
Defined by C0.5-C16 (See Table 1 - Truth Table)	X (Note 1)	X (Note1)	1

Note 1: PUP1 and PUP2 Connection may be 0, 1, GROUND, or No connection without effect on attenuation state.

Power-Up LE=1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active.

Additional Detailed Technical Information *additional information is available on our dash board. To access this information click here*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DG1677 *Plastic package, exposed paddle, lead finish: Ni/Pd/Au*
Tape & Reel **Standard quantities available on reel**	F68 *7" reels with 20,50,100,200, 500 or 1K devices* *13" reels with 2K devices*
Suggested Layout for PCB Design	PL-382
Evaluation Board	TB-681+
Environmental Ratings	ENV66

ESD Rating

Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1 - 2001

Machine Model (MM): Class M1 (40V) in accordance with ANSI/ESD STM5.2-1999

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart