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# P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
- 40	0.010 at V <sub>GS</sub> = - 10 V	- 16.1	33 nC			
- 40	0.014 at V <sub>GS</sub> = - 4.5 V	- 13.3	33110			

# **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



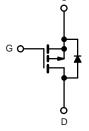
COMPLIANT HALOGEN FREE



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Top View



P-Channel MOSFET

### **APPLICATIONS**

- Load Switch
- POL

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	- 40	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
	T <sub>C</sub> = 25 °C		- 16.1		
Continuous Prais Current (T. 150 °C)	T <sub>C</sub> = 70 °C		- 12.9		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	- I <sub>D</sub>	- 10.2 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		- 8.2 <sup>b, c</sup>	^	
Pulsed Drain Current		I <sub>DM</sub>	- 50	A	
Continuo Source Drain Diade Current	T <sub>C</sub> = 25 °C		- 5.3		
Continous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	ls	- 2.1 <sup>b, c</sup>		
Single Pulse Avalanche Current	. 04!!	I <sub>AS</sub>	- 28		
Single Pulse Avalanche Energy	Avalanche Energy L = 0.1 mH		39	mJ	
	T <sub>C</sub> = 25 °C		6.3		
Manianum Danian Disaination	T <sub>C</sub> = 70 °C	Б.	4	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>		
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	37	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	16	20	C/VV		

### Notes:

- a. Based on T<sub>C</sub> = 25 °C.
  b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 85 °C/W.



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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static		,		•		•	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V, } I_D = -250  \mu\text{A}$	- 40			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 - 250		- 36		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = - 250 μA		5			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \mu A$	- 1.2		- 2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zarra Cata Valta va Basis Correct	I <sub>DSS</sub>	V <sub>DS</sub> = - 40 V, V <sub>GS</sub> = 0 V			- 1		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = - 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 25			Α	
	Б	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10.2 A	0.010				
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 8.4 A		0.014		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 10.2 A		37		S	
Dynamic <sup>b</sup>				l	l.		
Input Capacitance	C <sub>iss</sub>			3007			
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz		335		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			291			
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10.2 A		64	95		
Total Gate Charge	$Q_g$			33	50	nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10.2 \text{ A}$		9.8			
Gate-Drain Charge	Q <sub>gd</sub>			15.7			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.4	2	4	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			57	86		
Rise Time	t <sub>r</sub>	$V_{DD} = -20 \text{ V}, R_{L} = 2.4 \Omega$		50	75	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ - 8.2 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 1 $\Omega$		40	60		
Fall Time	t <sub>f</sub>			17	26		
Turn-On Delay Time	t <sub>d(on)</sub>			13	20		
Rise Time	t <sub>r</sub>	$V_{DD} = -20 \text{ V}, R_{L} = 2.4 \Omega$		11	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ - 8.2 A, $V_{GEN}$ = - 10 V, $R_g$ = 1 $\Omega$		45	68		
Fall Time	t <sub>f</sub>			9	18		
Drain-Source Body Diode Characteristic	cs			l	l.		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 5.3	_	
Pulse Diode Forward Current	I <sub>SM</sub>				- 50	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 8.2 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 8.2 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		36	54	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			41	62	nC	
Reverse Recovery Fall Time	t <sub>a</sub>			20			
Reverse Recovery Rise Time	t <sub>b</sub>	1		16		ns	

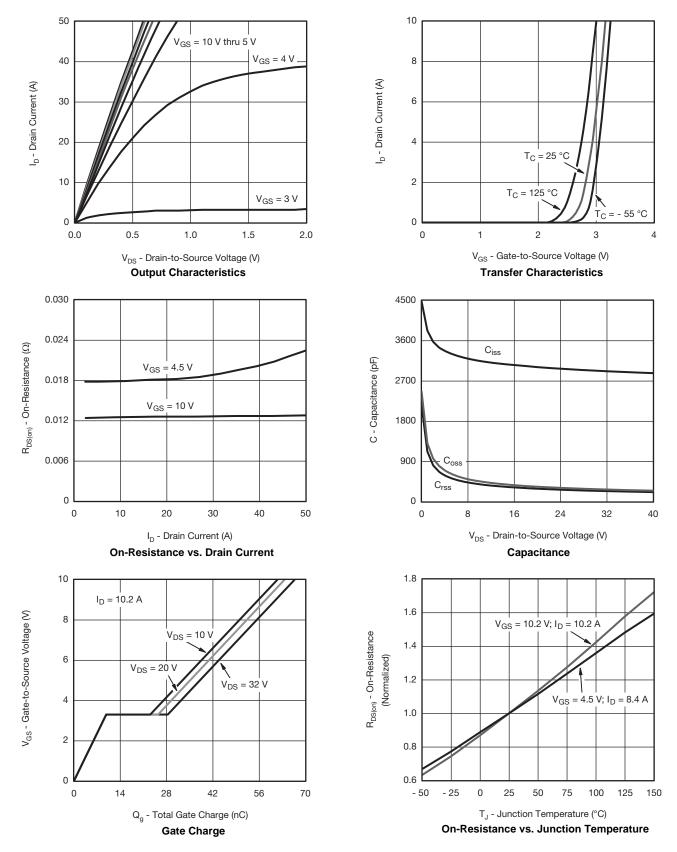
#### Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

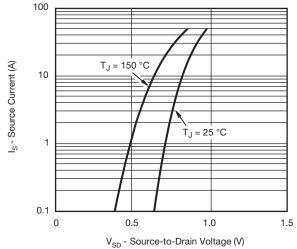
a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

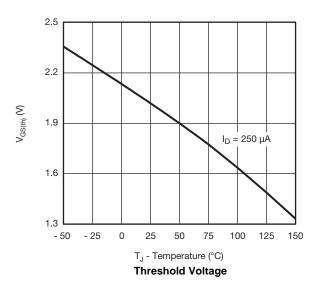


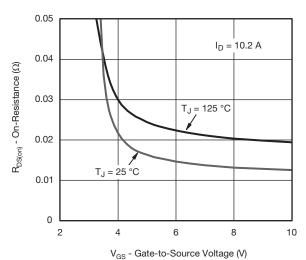




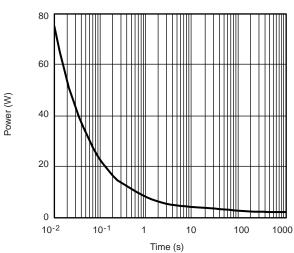


#### Source-Drain Diode Forward Voltage

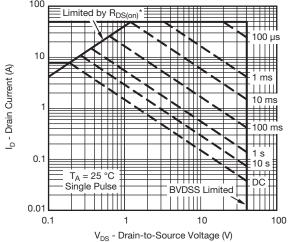




On-Resistance vs. Gate-to-Source Voltage



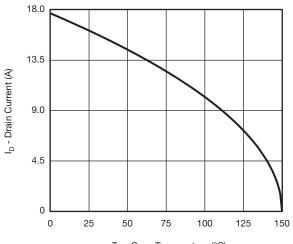
Single Pulse Power (Junction-to-Ambient)



 $^{*}V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

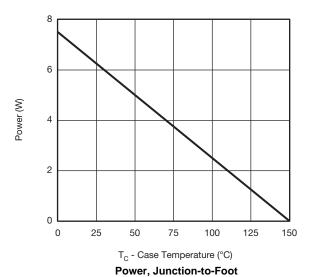
Safe Operating Area, Junction-to-Ambient

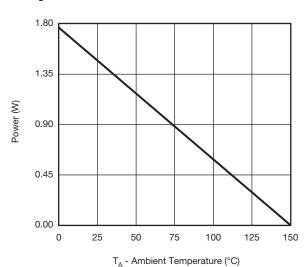




 $T_C$  - Case Temperature (°C)

#### **Current Derating\***

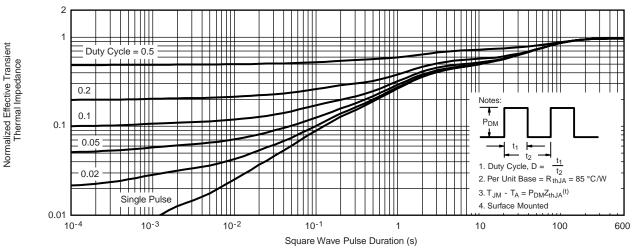




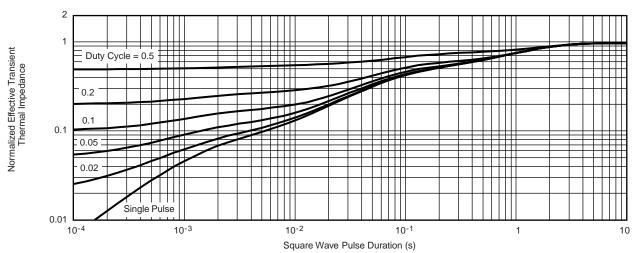
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient

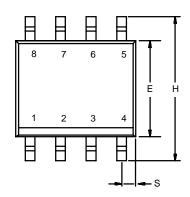


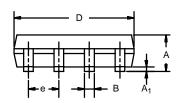
Normalized Thermal Transient Impedance, Junction-to-Foot

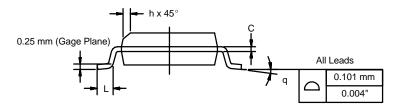




**SOIC (NARROW): 8-LEAD** JEDEC Part Number: MS-012







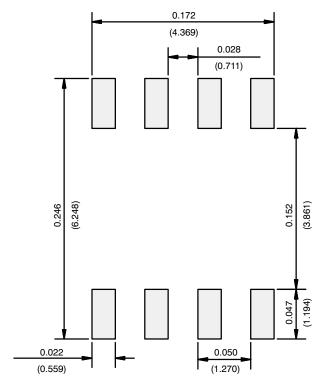
	MILLIM	IETERS	S INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev I 11-Sen-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



## **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)





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