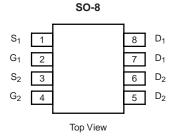


DTM4946 www.din-tek.jp

Dual N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)			
60	0.038 at V _{GS} = 10 V	7.0	9.2 nC			
	0.043 at V _{GS} = 4.5 V	5.8	9.2 110			



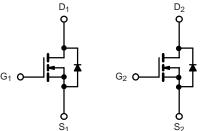
FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Power MOSFET
- 175 °C Maximum Junction Temperature
- 100 % R_q Tested
- Compliant to RoHS directive 2002/95/EC



Available

G₁ **0**—



N-Channel MOSFET

N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	± 20	V	
	T _C = 25 °C		7.0		
Continuous Droin Current (T = 150 °C)	T _C = 70 °C		5.5		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	5.3 ^{a, b}		
	T _A = 70 °C		4.4 ^{a, b}		
Pulsed Drain Current		I _{DM}	30	— A	
	T _C = 25 °C	1.	7.0		
Continuous Source Drain Diode Current	T _A = 25 °C	I _S	5.3 ^{a, b}		
Avalanche Current	L = 0.1 mH	I _{AS}	22		
Single-Pulse Avalanche Energy		E _{AS}	7.2	mJ	
	T _C = 25 °C		3.7		
Maximum Power Dissipation	T _C = 70 °C	р	2.6	w	
	T _A = 25 °C	P _D	2.4 ^{a, b}		
	T _A = 70 °C		1.7 ^{a, b}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, c}	$t \le 10 s$	R _{thJA}	50	62.5	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	33	41	C/W		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

d. Maximum under Steady State conditions is 110 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					1	1
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	60			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 250 0		53		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 6.7		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	1.0	2.4	3.0	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
		$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μA
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 V, V_{GS} = 10 V$	30			A
		V _{GS} = 10 V, I _D = 5.3 A		0.038	0.042	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.7 A	0.043		0.048	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.3 A		24		S
Dynamic ^b				I	I	I
Input Capacitance	C _{iss}			840		pF
Output Capacitance	C _{oss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		71		
Reverse Transfer Capacitance	C _{rss}			44		
-		$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5.3 \text{ A}$		17	25	nC
Total Gate Charge	Qg			9.2	12	
Gate-Source Charge	Q _{gs}	$V_{DS} = 30$ V, $V_{GS} = 5$ V, $I_{D} = 5.3$ A		3.3		
Gate-Drain Charge	Q _{gd}			3.7		
Gate Resistance	R _g	f = 1 MHz	3.1	6.5	9.5	Ω
Turn-On Delay Time	t _{d(on)}			20	30	-
Rise Time	t _r	V_{DD} = 30 V, R_{L} = 6.8 Ω		120	180	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 4.4 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		20	30	
Fall Time	t _f			30	45	
Turn-On Delay Time	t _{d(on)}			10	15	ns
Rise Time	t _r	V_{DD} = 30 V, R_L = 6.8 Ω		12	20	-
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 4.4 \text{ A}, V_{GEN} = 10 \text{ V}, \text{R}_g = 1 \Omega$		25	40	
Fall Time	t _f	~		10	15	1
Drain-Source Body Diode Characterist	ics					<u>,</u>
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			7.0	۸
Pulse Diode Forward Current ^a	I _{SM}				30	A
Body Diode Voltage	V _{SD}	I _S = 2 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			25	50	ns
Body Diode Reverse Recovery Charge	Q _{rr}			25	50	nC
Reverse Recovery Fall Time	t _a	I _F = 4.4 A, dl/dt = 100 A/μs, T _J = 25 °C		18		
Reverse Recovery Rise Time	t _b			7		ns

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

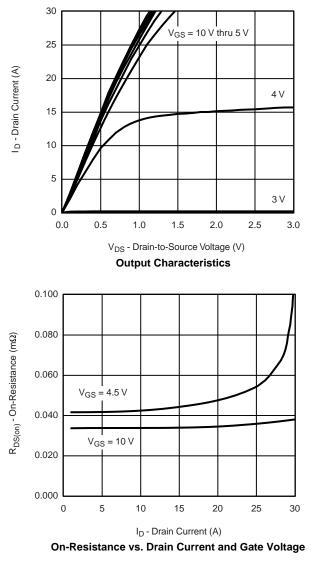
b. Guaranteed by design, not subject to production testing.

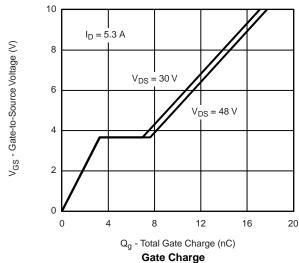
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

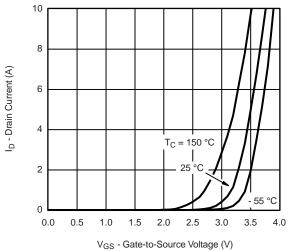


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

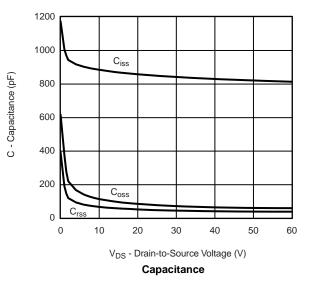
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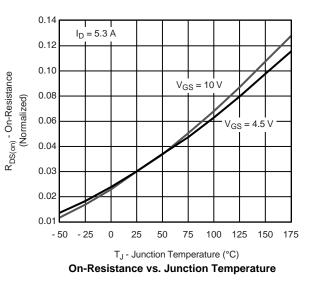






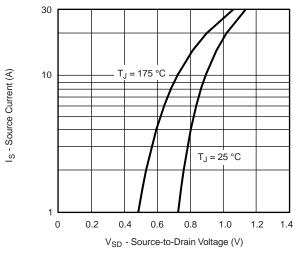
Transfer Characteristics

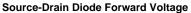


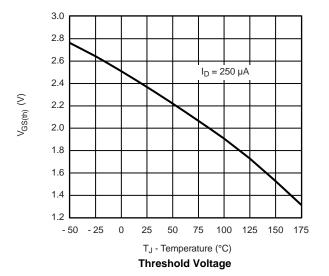


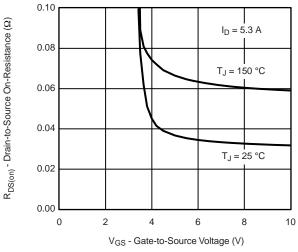
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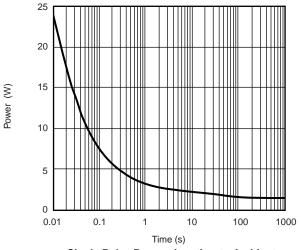




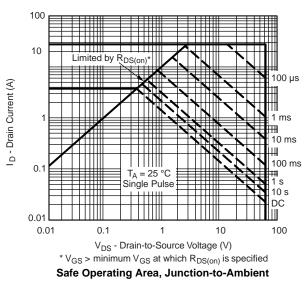




On-Resistance vs. Gate-to-Source Voltage



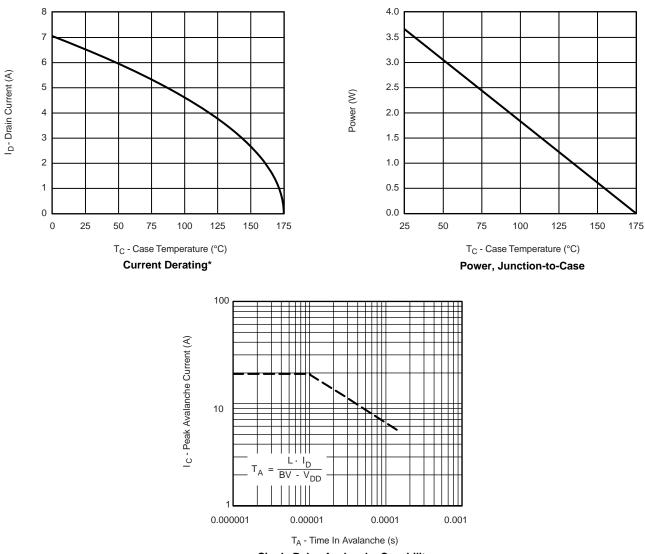






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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

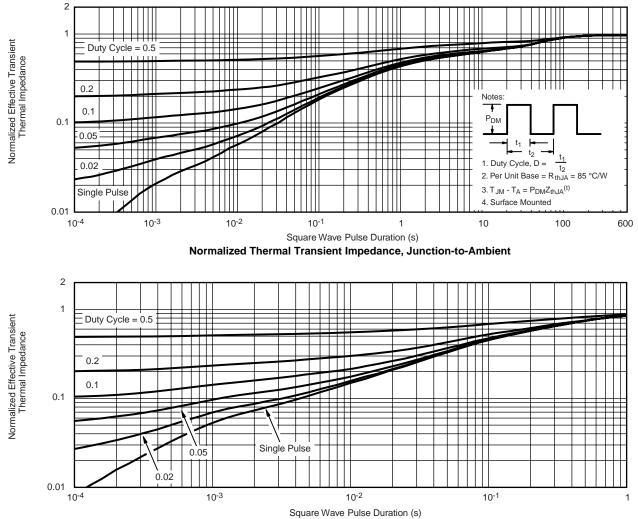


Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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Normalized Thermal Transient Impedance, Junction-to-Case

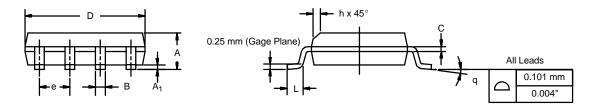


Package Information www.din-tek.jp

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

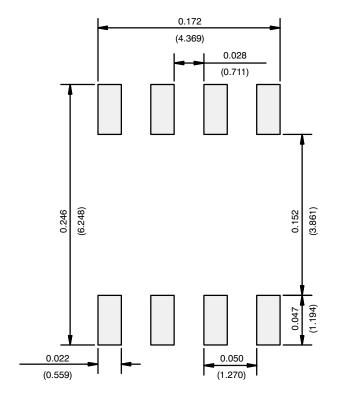




	MILLIM	IETERS	INCHES			
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	0.050 BSC		
н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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