

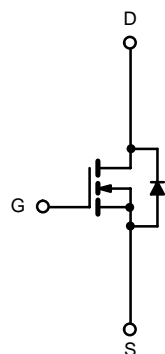
N-Channel 120 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
120	0.0075 at $V_{GS} = 10$ V	128 ^a

FEATURES

- TrenchFET® Power MOSFET
- New Package with Low Thermal Resistance
- 100 % R_g Tested


RoHS
 COMPLIANT


N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	128 ^a	A
		92 ^a	
Pulsed Drain Current	I_{DM}	410	
Avalanche Current	I_{AR}	75	mJ
Repetitive Avalanche Energy ^b	E_{AR}	280	
Maximum Power Dissipation ^b	P_D	375 ^c	W
		3.75	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.4	

Notes:

a. Package limited.

 b. Duty cycle ≤ 1 %.

c. See SOA curve for voltage derating.

d. When mounted on 1" square PCB (FR-4 material).

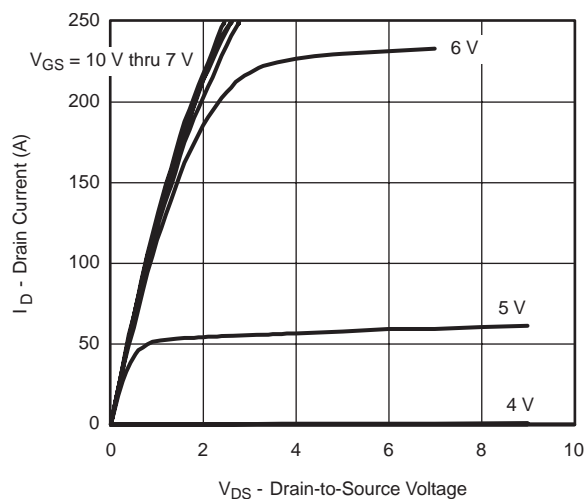
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	120			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^{\circ}\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		0.0075	0.009	Ω
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$			0.017	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$			0.025	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	25			S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		6200		pF
Output Capacitance	C_{oss}			930		
Reverse Transfer Capacitance	C_{rss}			420		
Total Gate Charge ^c	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 85\text{ A}$		130	160	nC
Gate-Source Charge ^c	Q_{gs}			24		
Gate-Drain Charge ^c	Q_{gd}			24		
Gate Resistance	R_g		1.0		6.2	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong 85\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		20	30	ns
Rise Time ^c	t_r			125	200	
Turn-Off Delay Time ^c	$t_{d(off)}$			55	85	
Fall Time ^c	t_f			130	195	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^{\circ}\text{C}$ ^b						
Continuous Current	I_S				110	A
Pulsed Current	I_{SM}				240	
Forward Voltage ^a	V_{SD}	$I_F = 85\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		70	140	ns
Peak Reverse Recovery Charge	$I_{RM(REC)}$			5.5	10	A
Reverse Recovery Charge	Q_{rr}			0.19	0.35	μC

Notes:

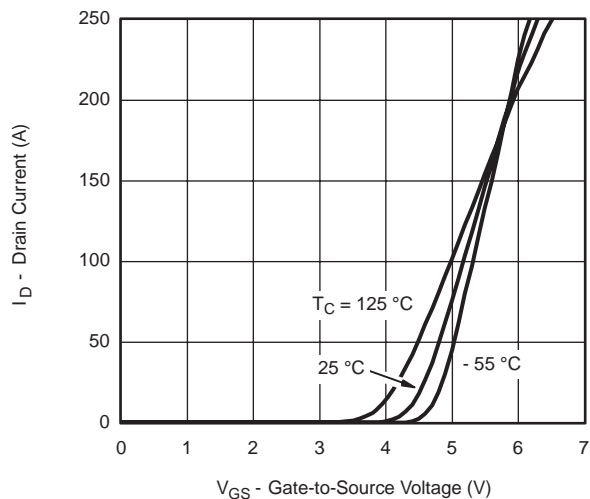
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

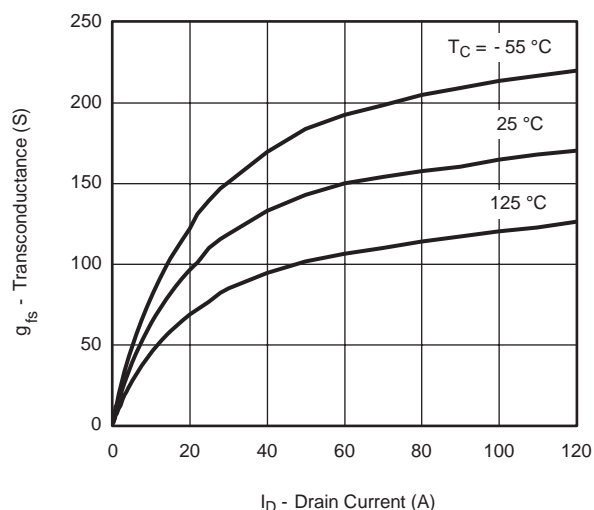
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



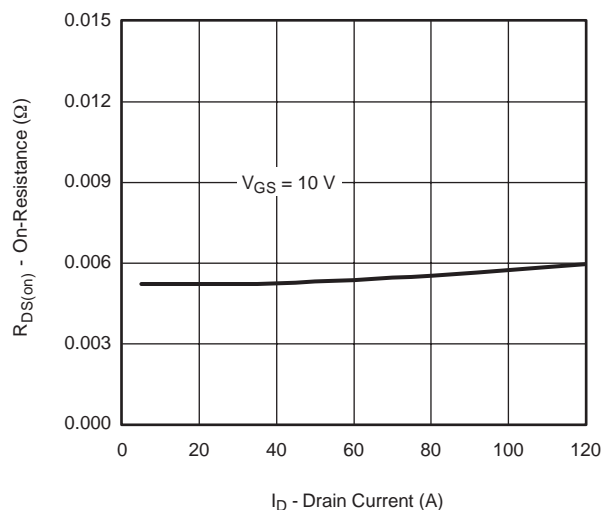
Output Characteristics



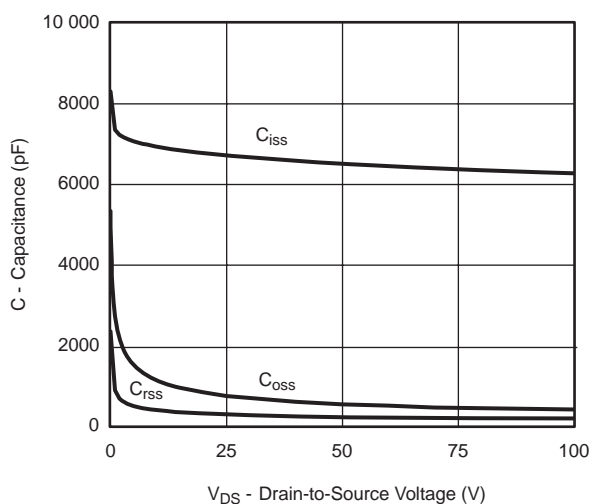
Transfer Characteristics



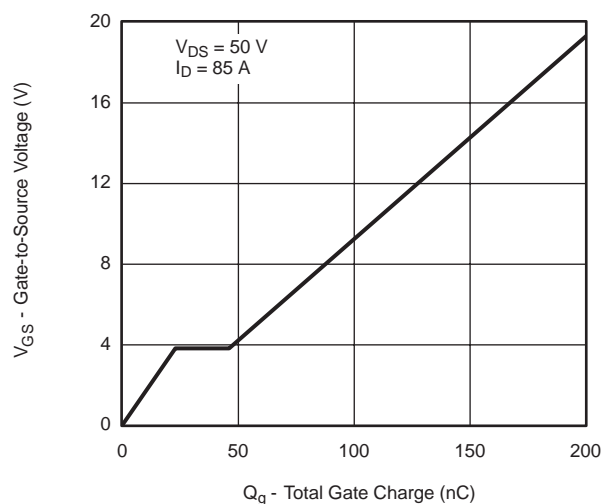
Transconductance



On-Resistance vs. Drain Current

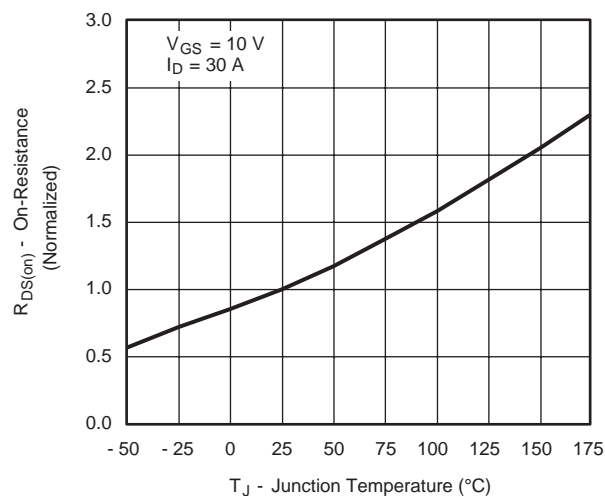


Capacitance

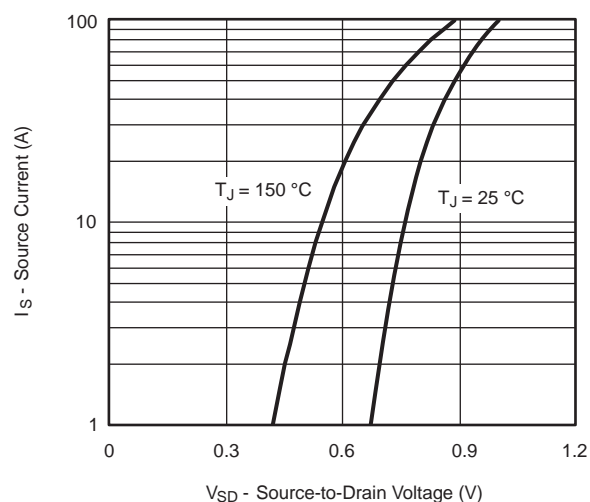


Gate Charge

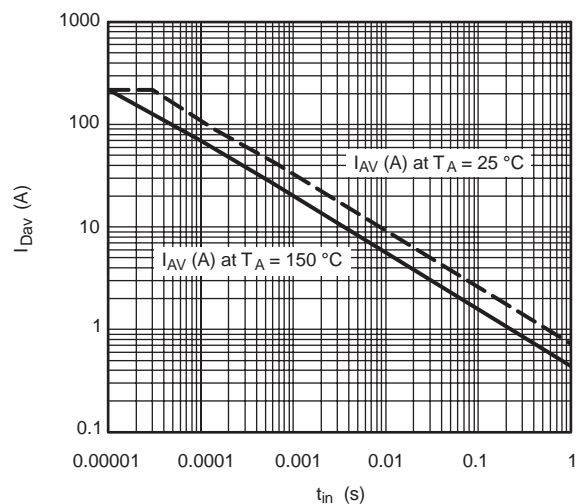
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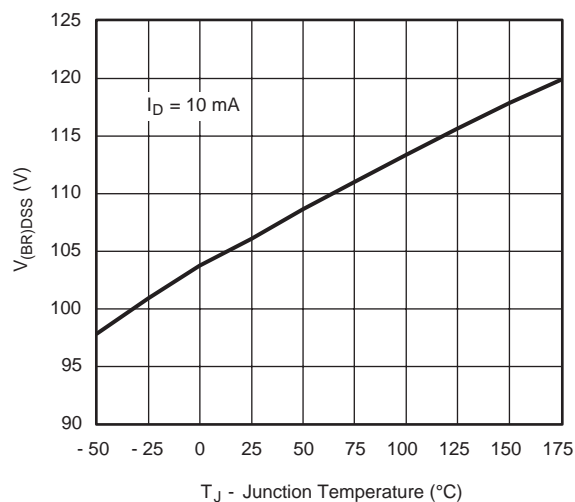
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

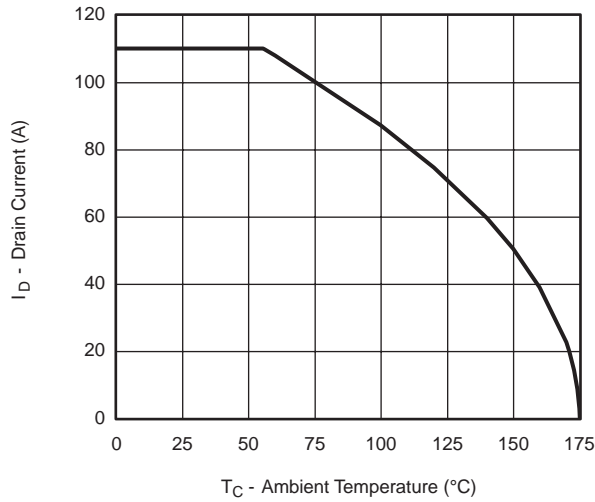


Avalanche Current vs. Time

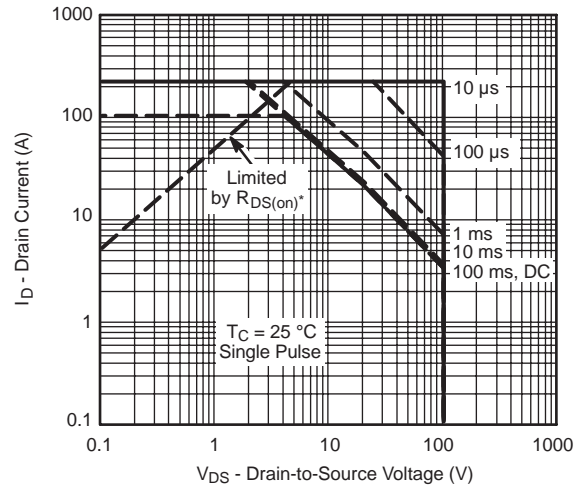


Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS

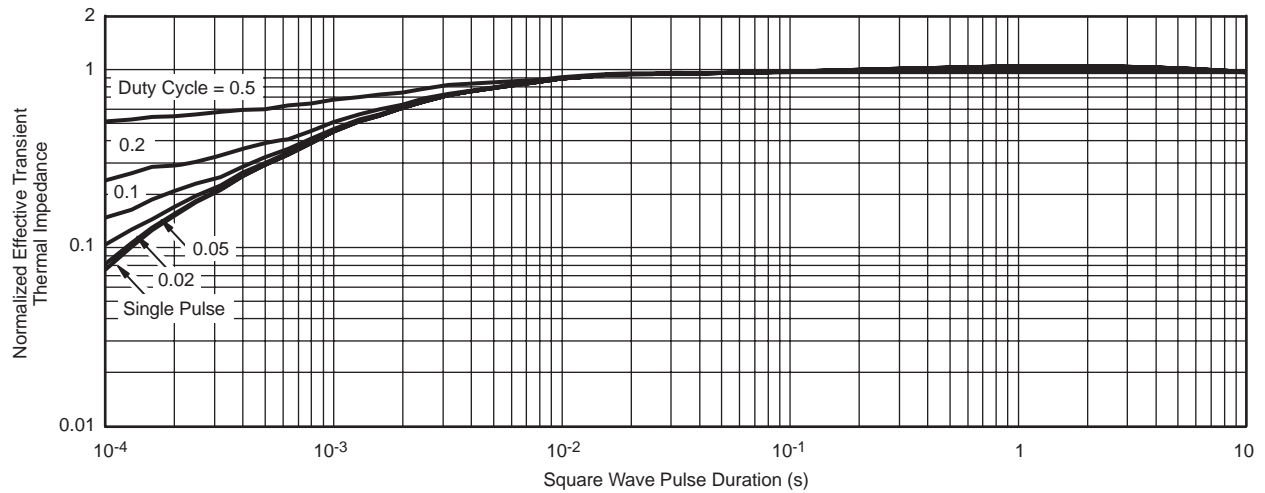


**Maximum Avalanche and Drain Current
vs. Case Temperature**



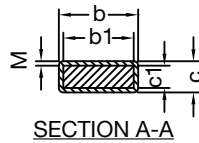
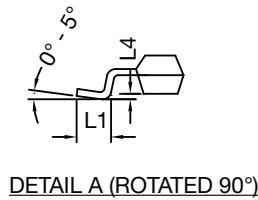
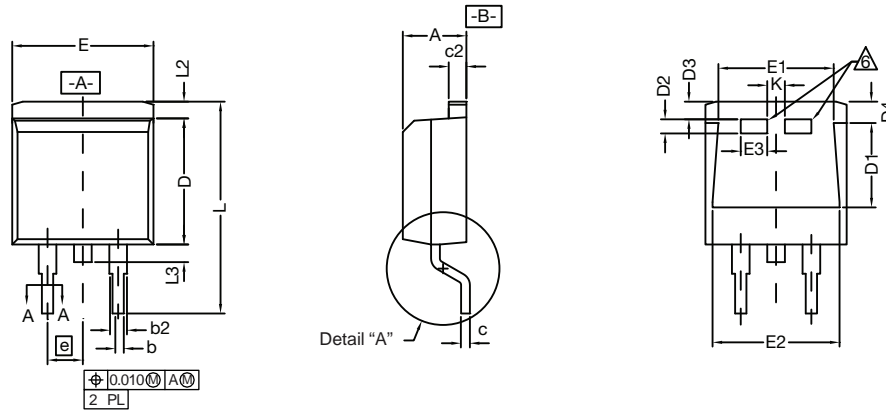
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-263 (D²PAK): 3-LEAD

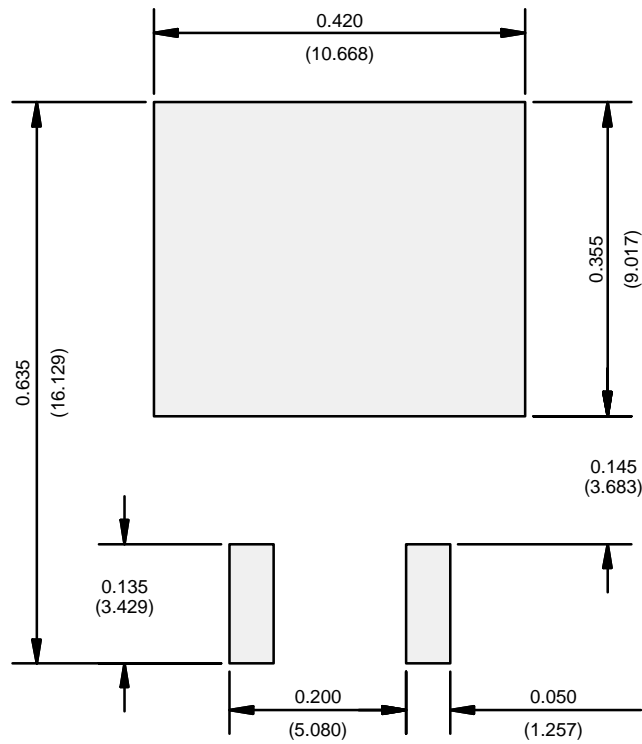


Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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