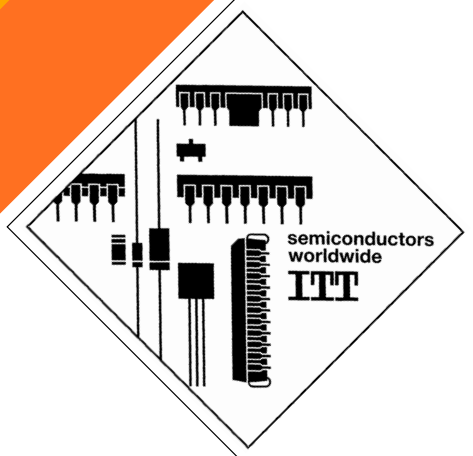


DTI 2260
Digital Transient Improvement Processor

Edition Dec. 2, 1994
6251-348-1DS

ITT Semiconductors

Contents

Digital Transient Improvement Processor

Note: If not otherwise designated, the pin numbers mentioned refer to the 40-pin DIL package.

1. Introduction

The DTI 2260 is a digital video processor for YUV picture data. It performs horizontal compression and zoom from 66% to 150% in 255 steps. This allows aspect ratio conversion in 16:9 TV environments, as well as the generation of square pixels in computer applications.

To enhance the sharpness of the chrominance signal, which is usually limited to around 1 MHz, the DTI 2260 provides a digital color transient improvement. Therefore, the U and V chrominance signals are interpolated from 4:1:1 to 4:2:2 and processed by a non-linear digital filter. This operation considerably enhances the picture quality of colored images.

Additionally, variable luminance and chrominance delay lines are implemented to match the processing delay of the DIGIT 2000 system to one horizontal line of video (64 µs), which is essential for synchronous RGB-overlay.

1.1. Block Diagram

The DTI 2260 is designed in NMOS technology. On one silicon chip, it contains mainly the following functional blocks (see Fig. 1–1):

– format processing for horizontal compression and zoom

– data orthogonalization/square pixel

– adjustable luma delay line (50 to 72 µs)

– adjustable chroma delay line (50 to 72 µs)

– digital 4:1:1 to 4:2:2 chrominance interpolation filter

– digital color transient improvement

– color saturation multiplier and hue correction

– 4:2:2 output for DIGIT 2000 applications

– orthogonal output format selectable between 4:1:1 or 4:2:2

– IM bus interface

Table 1–1 describes the major differences between the different versions of the well-known DTI family.

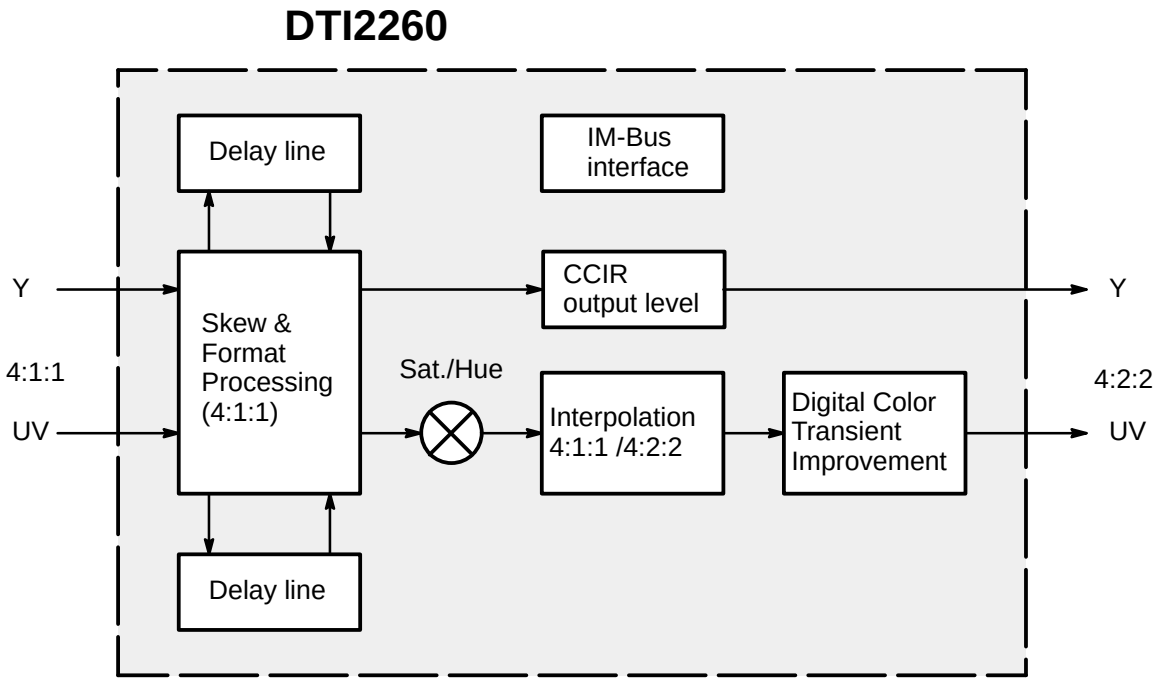


Fig. 1–1: Block Diagram of the DTI 2260 Digital Transient Improvement Processor

Table 1–1: Overview of the different versions of the DTI family

Function	DTI 2223	DTI 2251 / DTI 2250	DTI 2260
Compression	–	100% to 66%	100% to 66%
Zoom	–	100% to 150% (DTI2251 only)	100% to 150%
Data Orthogonalization/ Square Pixel	–	yes	yes
Delay	0 to 60 µs	50 to 72 µs	50 to 72 µs
Transient Improvement	Sample and Hold	Sample and Hold	digital Interpolation
Output format	4:1:1 DIGIT 2000	4:1:1 DIGIT 2000 4:1:1 orthogonal	4:2:2 DIGIT 2000 4:2:2 orthogonal 4:1:1 orthogonal
Color Saturation Multiplier	yes	yes	yes

1.2. Environment

Figs. 1–2 to 1–5 show how the DTI 2260 Digital Transient Improvement Processor fits into the DIGIT 2000 system of ITT. The digital luma and chroma signals provided by the color decoders for PAL/NTSC (PVPU2204, ACVP2205 or VSP2860), SECAM (SPU2243) or D/D2-MAC (DMA2281) are fed to the DTI 2260 Digital Transient Improvement Processor where they are further processed as described in section 2.

The output of the DTI 2260 can either be connected to a VDU 2146 to obtain the analog RGB signals, or be used in computer environments and multimedia applications (e.g. frame grabbers etc.).

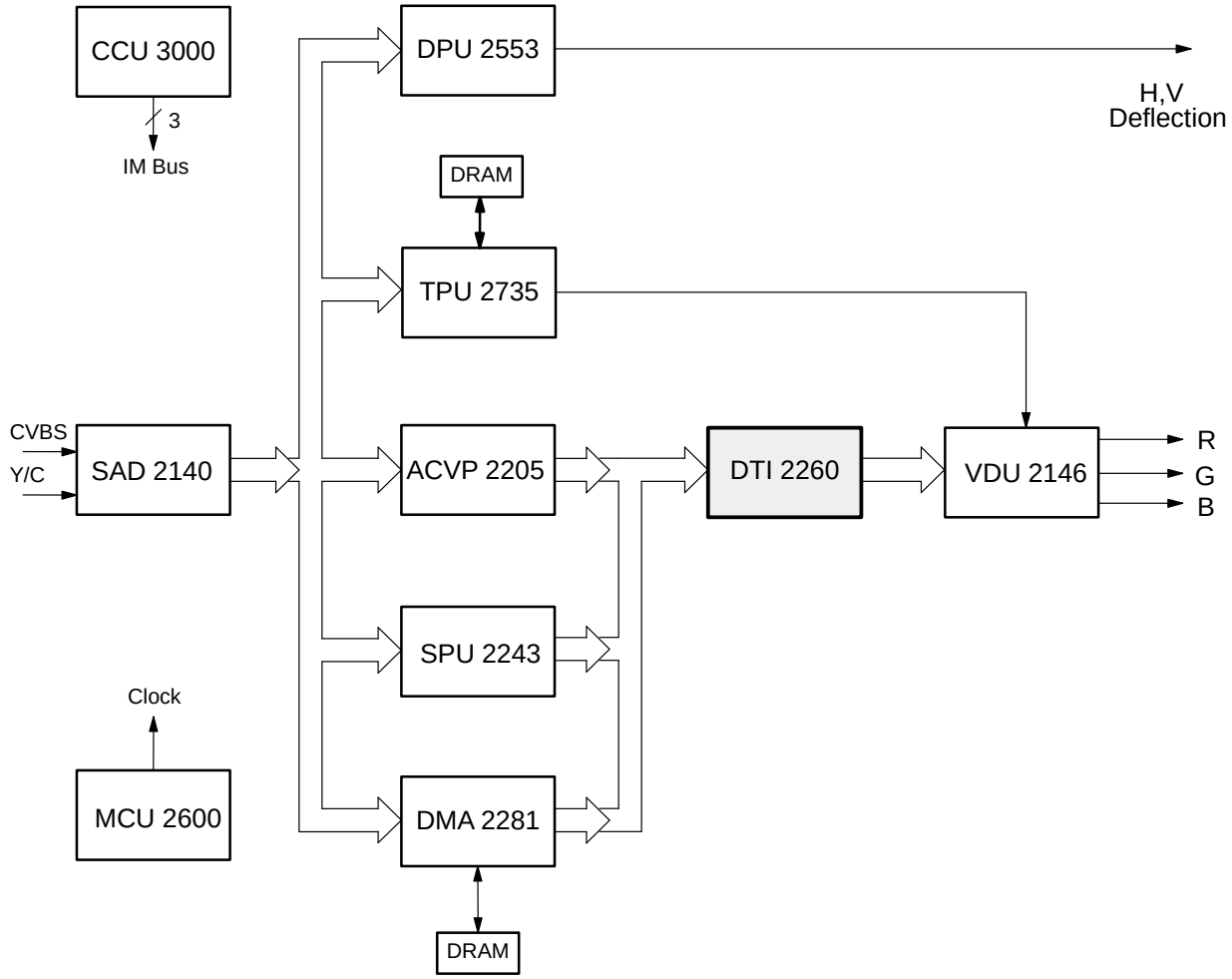


Fig. 1–2: DIGIT2000 with DTI 2260 in a multistandard and multiformat TV receiver

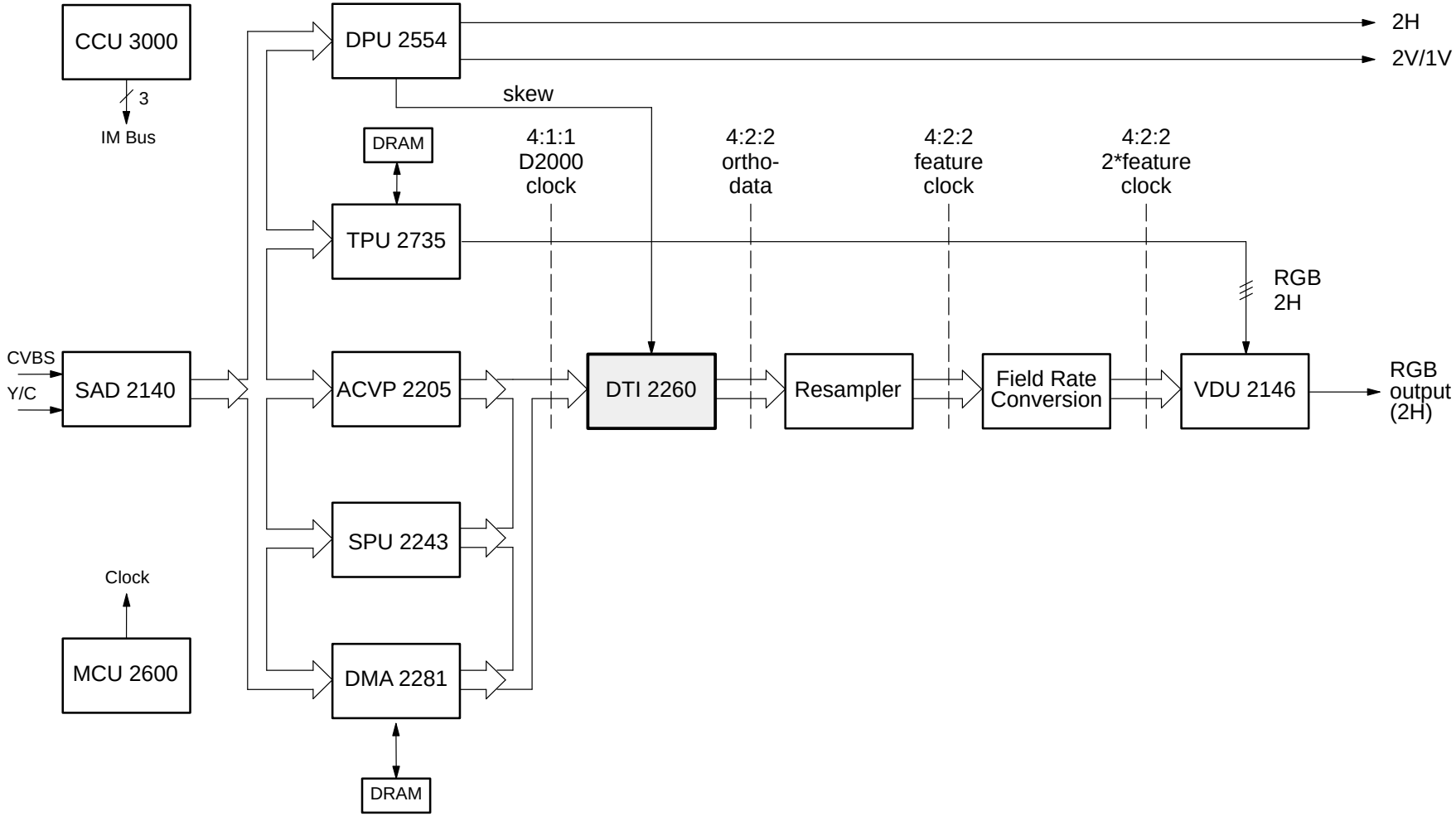


Fig. 1–3: DIGIT2000 with DTI 2260 in a scan rate conversion TV receiver

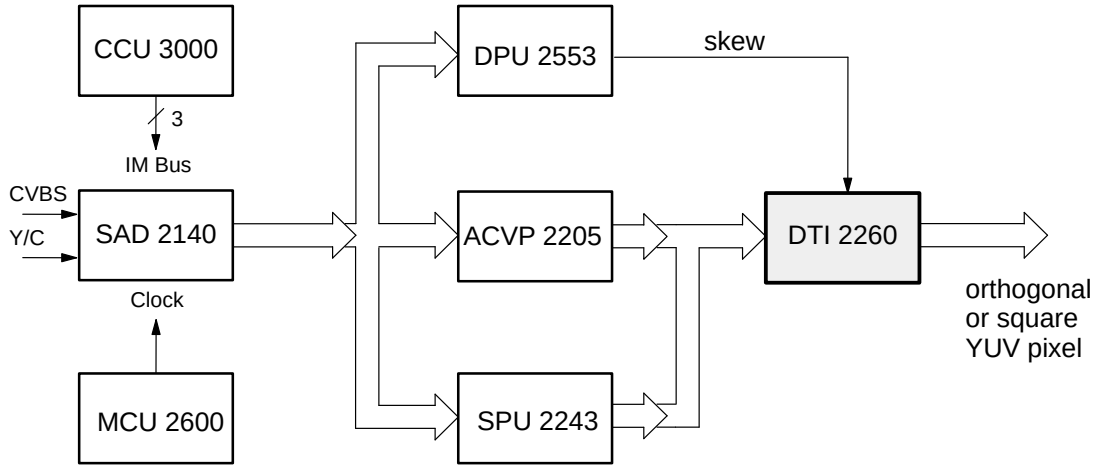


Fig. 1–4: DIGIT2000 with DTI 2260 as multistandard high quality square pixel decoder for multimedia applications

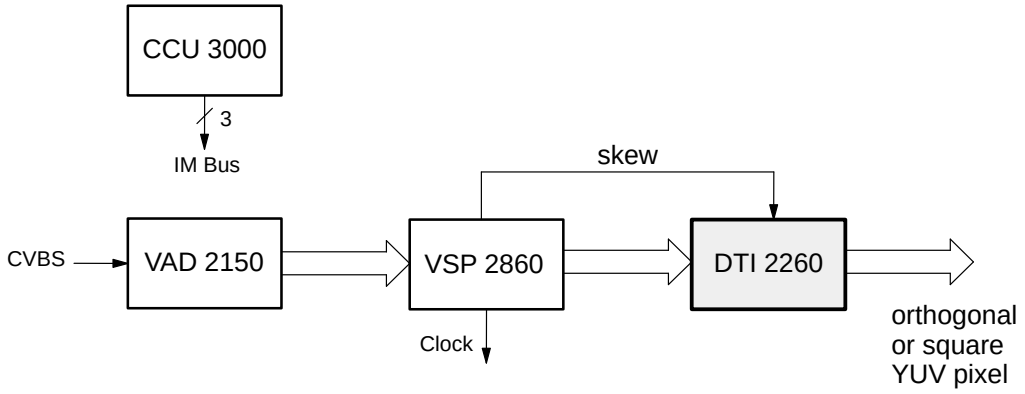


Fig. 1–5: VSP2860 with DTI 2260 as low-cost square pixel decoder

2. Functional Description

2.1. Format Processing

The process of zooming or compression is performed by interpolation and a FIFO-resampler (see Fig. 2–1). Note that the system clock is not changed whereas the local signal frequencies will increase (decrease) due to compression (zoom). In order to save memory, only active picture data is stored in the FIFO, while the12 µs horizontal blanking period is not stored. The FIFO balance is maintained by two counters, counting writes to and reads from the FIFO respectively. Read is continued until it reaches the previous number of writes. This controlling is essential for a stable picture in VCR mode.

The organization of the hardware and timing is different in zoom and compression mode. In zoom mode (enabled via the MSB of COMPR), the unprocessed data is stored in the FIFO. Resampling and interpolation is done at the FIFO output. In compression mode, the input data is immediately interpolated and resampled before writing it into the FIFO.

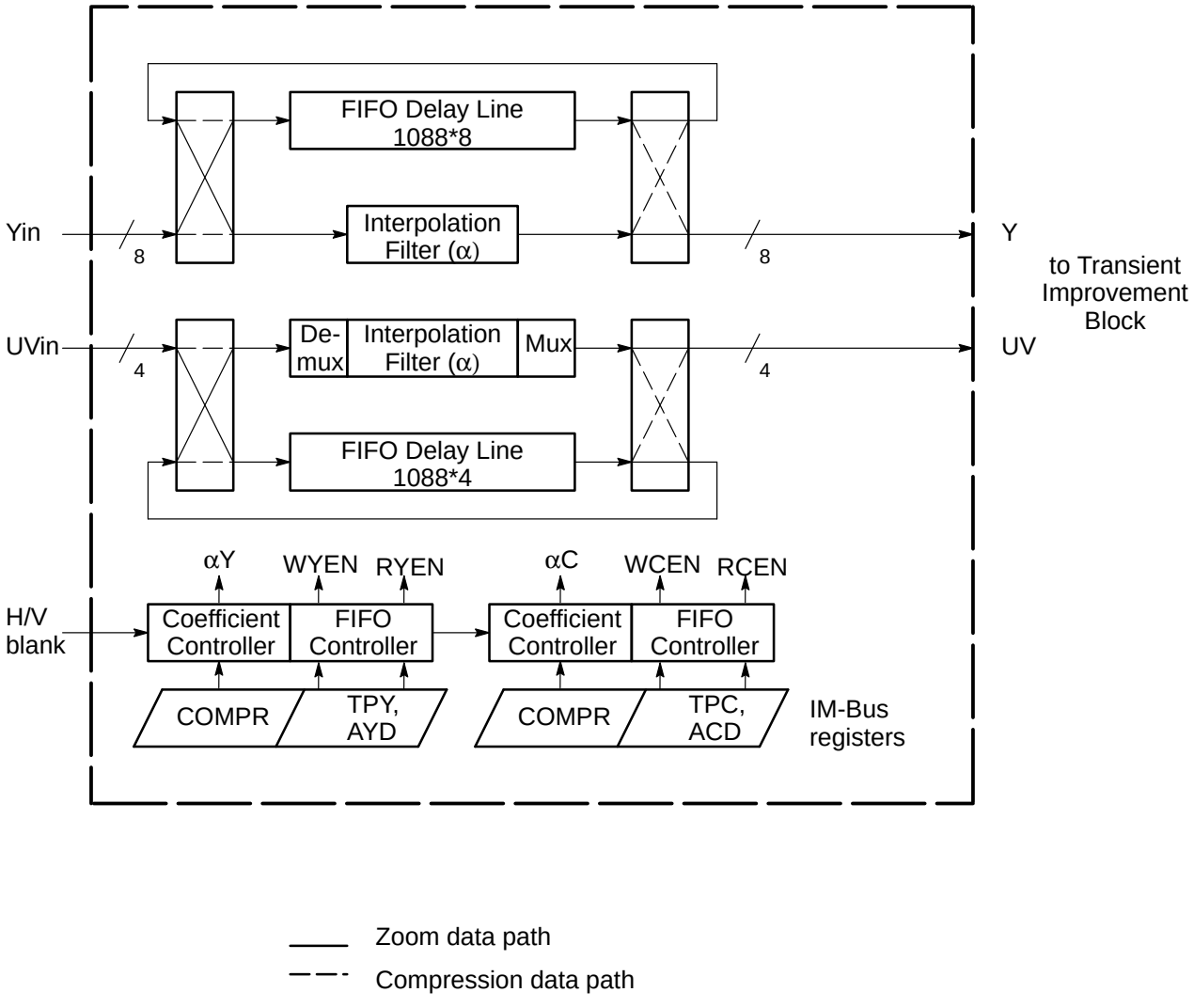


Fig. 2–1: Format Processing block diagram

2.1.1. Interpolation Filters

The Interpolation filters are designed as a 2*over-sampled linear interpolation. In total 4 samples are used to calculate one new output sample. The filters act as a variable time delay.

The luminance filter group delay can be varied from 0 to 1 clock in 32 steps, which is equivalent to ca. 1.5 ns resolution. The filters magnitude and group delay frequency responses are shown in Fig. 2–2.

The chroma filter uses the same interpolation technique. Due to the small chroma bandwidth of the color-difference signals, the group delay can be varied from 0 to 4 clocks in 4 steps only. The resolution is ca. 50 ns. The frequency responses are equivalent to those of the luminance filter, only the frequency axis is scaled by 1/4 (Fig. 2–3).

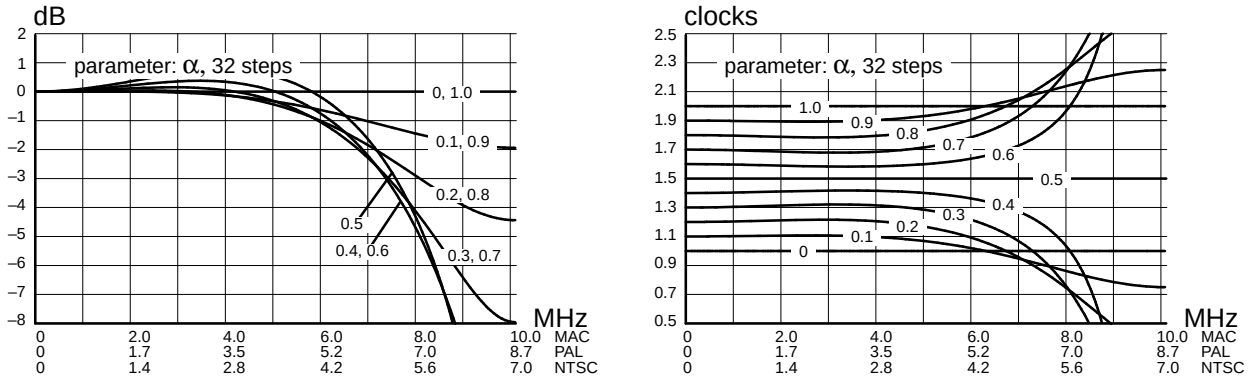


Fig. 2–2: Luminance interpolation filter magnitude and group-delay frequency responses

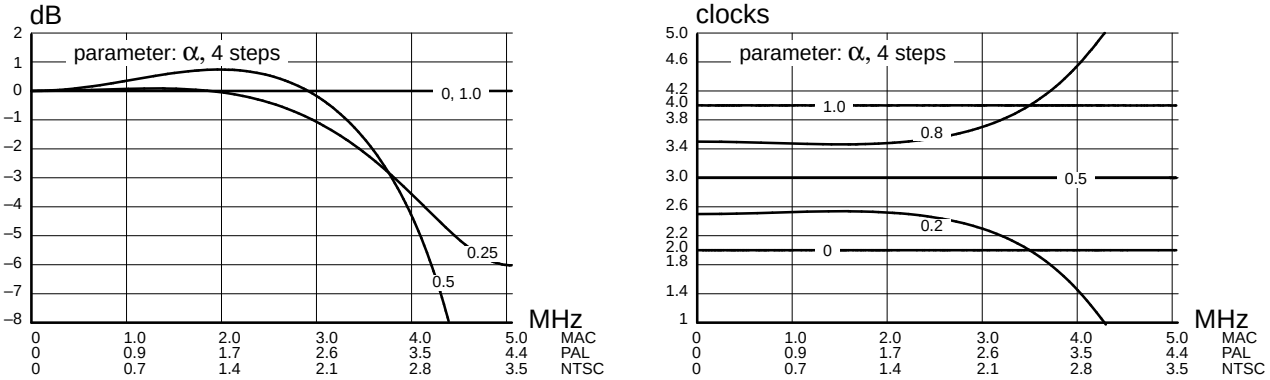


Fig. 2–3: Chrominance interpolation filter magnitude and group-delay frequency responses

2.1.2. Coefficient Controller

The desired format ratio “COMPR” must be transferred via IM bus. Two accumulators generate the coefficients for the interpolation filters and the timing signals for the FIFO controller. During horizontal blanking no compression is carried out.

During vertical blanking the entire chip is bypassed, including the color transient improver. The bypass period is identical to the external vertical blanking signal or 19 H-pulses (derived from an internal counter), whatever period is longer. The intention is to keep chroma-sync, 72-bit control data and VBI-text/VPS data unmodified.

In case of skew correction operation (e.g. computer applications), the skew data information from the deflection unit is loaded into the coefficient controller. This will cause the interpolation filters to compensate the skew value by delaying the YUV signals to an orthogonal structure. In this case the bit ‘SKEN’ must be set to ‘1’. If it is set to ‘0’, the skew value is ignored.

2.1.3. FIFO Controller

The FIFO controller has the task to acquire and resample data depending on zoom/compression rates and delay settings. It generates the write-enable and read-enable for the Luma and Chroma-FIFOs.

The FIFO controller is updated every horizontal blanking.

2.1.4. Sync Delay Circuit

The horizontal blanking signal connected to the DTI2260 is internally delayed to adapt to various signal processing delays in front of the DTI (e.g. ACVP, SPU, DMA). Two adjustable delay elements (TPY and TPC) generate 12 µs pulses that have to be placed at the blanking portion of the digital YUV-signals. The delays are adjustable in steps of four clocks from 0 to127 corresponding to approximately 0 to 28 µs.

The 12 µsec blanking period is generated internally by counting clocks. The ZN-register is decoded to know the actual system clock frequency. The individual counter decodes for the blanking are:
14.3 MHz: 168 clocks (11.7 µsec)
17.7 MHz: 214 clocks (12.1 µsec)
20.2 MHz: 243 clocks (12.0 µsec)

An internal delay of 804 clocks (NTSC: 536 clocks) is provided as a “negative” timing reference with respect to the undelayed horizontal blanking input. This is essential for the position or the acquisition of the compressed/zoomed image. The operation is shown in figures 2–5 to 2–7.

An extra sync delay of 396 clocks will applied to the horizontal sync input if the Bit “ISDE” is set to “1”. This mode is used in MAC applications where the phase of the horizontal sync provided by the MAC-decoder is out-of phase with the YUV picture data (e.g. BSYNC = burst sync).

2.1.5. The Luma and Chroma Delay Lines

In the DIGIT 2000 system, the digital signal processing time between analog input of the A/D input and RGB D/A output is about 4 to 12 µs, depending on the system configuration. This delay causes a timing mismatch, if external analog information, which has no delay, is intended to be “boxed in” via the RGB inputs of the VDU Video Display Unit.

To solve this problem, the digital luma/chroma signals must be additionally delayed to an overall delay of one horizontal line. Thus, the DTI 2260 offers two delay lines one for luma and one for chroma on chip. They are realized by two FIFOs. The luminance delay line is 8-bit wide. The chrominance delay line is 4-bit wide and contains the nibble-multiplexed UV-pairs.

Only active video is stored in the FIFOs. The amount of delay is adjustable in steps of four clock cycles each by means of the CCU, using IM bus address 157. The proper delay value is stored in the MDA 2062 or NVM 3060 EEPROM by the manufacturer during set production. The delays of Luma and Chroma can be adjusted independently. Delay=0 is decoded separately and obtained by bypassing the FIFO. Note: this bypass is enabled if one or both delay coefficients are set to zero. To have the FIFO work, be sure to have both coefficients AYD and ACD>0. The FIFOs are reset and initialized with the start of the vertical blanking.

The wide range of delay adjustment with the FIFOs is used to position the zoomed or compressed picture on the screen.

2.1.6. Abbreviations and Symbols

The abbreviations and symbols used in this data sheet are as follows:

fs	sampling frequency (system clock)
H	number of samples per line
HBL	internally generated hor. blanking pulse
IDEL	internal delay
Nmax	FIFO length
C	compression factor (1.5 to 0.66)
TA	number of samples written into FIFO per line
TAL, TAC	define number of samples written into FIFO per line in upsampling mode (SCO = 1)
TC	compression: number of samples taken out zoom: number of samples inserted (0 to 351)
COMPR	value to control the compression/zoom ratio
TPx	TPY or TPC for Luma or Chroma respect.
AxD	AYD or ACD for Luma or Chroma respect.

The following equations express the symbols and their relationships to one another:

Compression Mode:
TC = (1–C) x 52 µs x fs
COMPR = (1/C–1) x 256
C = 256/(COMPR+256)
TC = (COMPR/(COMPR+256)) x 52 µs x fs

Zoom Mode:
TC = (1–1/C) x 52 µs x fs
COMPR = (C–1) x 256+128
C = (COMPR+128)/256
TC = (1–256/(COMPR+128)) x 52 µs x fs

Upsampling Mode: (SCO = 1)
TA = TAL x 8
C = (COMPR + 128)/256
TA x C < 64 µs x fs (FIFO balance)

Table 2–1: System characteristics

Symbol	**Explanation**	**TV mode:**				**Unit**	**Condition**
		NTSC	PAL	SEC.	MAC		
fs	sampling frequency	14.3	17.7	17.7	20.25	MHz	
H	number of samples p. line	910	1135	1135	1296	–	
HBL	internal blanking pulse	172	212	212	244	–	
IDEL	internal delayed hor. ref.	536	804	804	804 396	–	ISDE = 0 ISDE = 1
Nmax	max. active FIFO length	1164	1164	1164	1164	–	
Nmin	min. active FIFO length	108	108	108	108	–	

Table 2–2: System parameters for COMPR = 0 ... 127 (compression mode, see Fig. 2–5)

Symbol	Explanation	TV mode:				Condition
		NTSC	PAL	SEC.	MAC	
TPY typ	typical TPY values	7	22	22	10	COMPR = 0 ...127
TPC typ	typical TPC values	11	27	46	14	COMPR = 0 ...127
AYD typ	typical AYD values	142	146	146	197	COMPR = 0
ACD typ	typical AYD values	130	134	134	185	COMPR = 0
AYD left mid right	typical AYD values	142 165 186	146 175 202	146 175 202	197 229 260	COMPR = 84 (75 %)
ACD left mid right	typical ACD values	129 152 174	133 161 189	134 162 190	185 217 248	COMPR = 84 (75 %)
AYD left mid right	typical AYD values	142 173 203	146 184 222	146 184 222	118 242 283	COMPR = 127 (66 %, max compress.)
ACD left mid right	typical ACD values	129 150 190	133 171 209	134 172 210	185 218 271	COMPR = 127 (66 %, max compress.)
AYD max	max. AYD due to timing	241 +TPY	196 +TPY	196 +TPY	210 +TPY	COMPR = 0
ACD max	max. ACD due to timing	241 +TPC	196 +TPC	196 +TPC	210 +TPC	COMPR = 0 < 231
AYD max	max. AYD due to FIFO	225	281	281	323	COMPR=127, TPY=0
ACD max	max. ACD due to FIFO	225	281	281	323	COMPR=127, TPC=0
AYD min	min. AYD due to FIFO	60	60	60	60	COMPR= 0...127,
ACD min	min. ACD due to FIFO	60	60	60	60	COMPR= 0...127,

Note: Tables 2–2, 2–3, and 2–4 contain typical values for the DTI 2260 under the following system configuration and conditions:

– DIGIT 2000 system with SAD 2140, VDU 2146, DPU 2553, ACVP 2205, SPU 2243, DMA 2281, and TPU 2735
– SCART input is used (not tuner)
– Undelayed horizontal blanking is input to pin 38
(also in case of D2-MAC)
– BP(DPU) and BPE(DPU) are both = 0
(blanking in phase with input video)
– DFS(DTI) = 0 narrow chroma filter selected

Table 2–3: System parameters for COMPR = 128 ... 255 (zoom mode, see Fig. 2–7)

Symbol	Explanation	TV mode:				Condition
		NTSC	PAL	SEC.	MAC	
TPY typ	typical TPY values	99	87	87	126	COMPR = 128 ... 255
TPC typ	typical TPC values	80	69	70	111	COMPR = 128 ... 255
AYD typ	typical AYD values	58	69	69	64	COMPR = 128
ACD typ	typical ACD values	58	69	90	64	COMPR = 128
AYD left mid right	typical AYD values	58 85 112	69 97 126	69 98 127	64 96 130	COMPR = 212 (133 %)
ACD left mid right	typical ACD values	58 85 112	69 97 126	90 119 148	64 96 130	COMPR = 212 (133 %)
AYD left mid right	typical AYD values	58 92 122	69 107 145	69 108 146	64 107 151	COMPR = 255 (150 %, max. zoom)
ACD left mid right	typical ACD values	58 92 122	69 107 145	90 129 167	64 107 151	COMPR = 255 (150 %, max. zoom)
AYD max	max. AYD due to timing	131 +TPY	198 +TPY	198 +TPY	198 +TPY	COMPR = 128
ACD max	max. ACD due to timing	131 +TPC	198 +TPC	198 +TPC	198 +TPC	COMPR = 128
AYD max	max. AYD due to FIFO	225	281	281	323	COMPR=255, TPY=0
ACD max	max. ACD due to FIFO	225	281	281	323	COMPR=255, TPC=0

Table 2–4: System parameters for upsampling mode (SCO = 1, COMPR = 128 ... 255)

Symbol	Explanation	TV mode:				Condition
		NTSC	PAL	SEC.	MAC	
TPY typ	typical TPY values	99	87	87	126	COMPR = 128 ... 255
TPC typ	typical TPC values	80	69	70	111	COMPR = 128 ... 255
AYD typ	typical AYD values	58	69	69	64	COMPR = 128
ACD typ	typical ACD values	58	69	90	64	COMPR = 128
TAL max TAC max	max TAL, max TAC due to timing	93 93	141 141	141 141	131 131	COMPR = 128
TAL max TAC max	max TAL, max TAC due to timing	85 85	107 107	107 107	121 121	COMPR = 212
TAL max TAC max	max TAL, max TAC due to timing	76 76	94 94	94 94	107 107	COMPR = 255

2.2. Compression

In the following example (Fig. 2–4), a 75% compression will generate 3 output samples out of 4 input samples. To simplify the model, a linear interpolation filter between two samples is used for explanation. Due to compression the number of active pixels will decrease to 75%. The remaining 25% pixels will be set blanked.

The range of active video input data with reference to the horizontal blanking input is defined by the registers TPY and TPC (see Fig 2–5). An internal window of 12 µs is shifted by 4 x TPx clock cycles. Only data outside this window will be processed and stored in the FIFO. Using the registers AYD and ACD (luma/chroma delay adjust), the total processing delay of the compressed data is programmable in a range of roughly 50 to 72 µs with increments of 4 clock cycles. This allows an arbitrary picture position, without touching the deflection parameters.

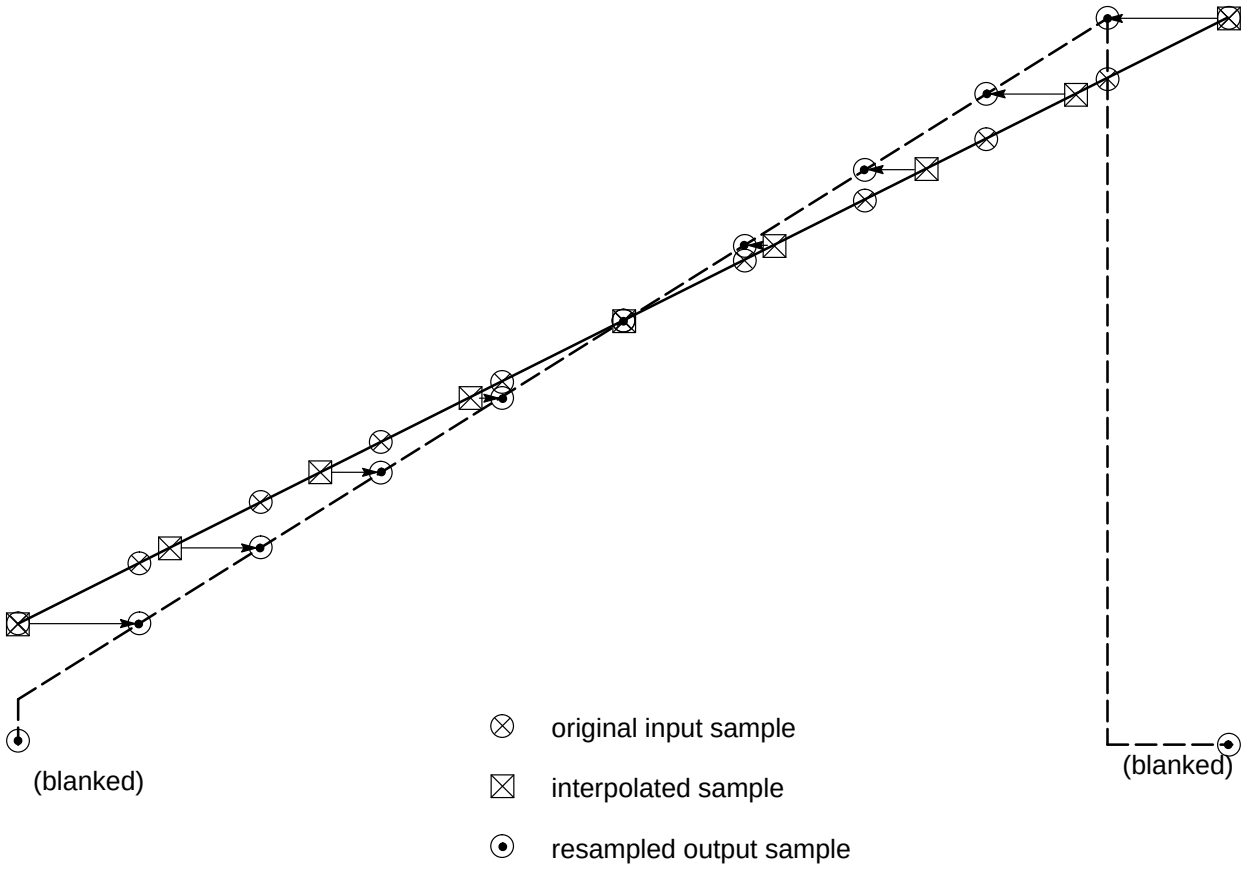
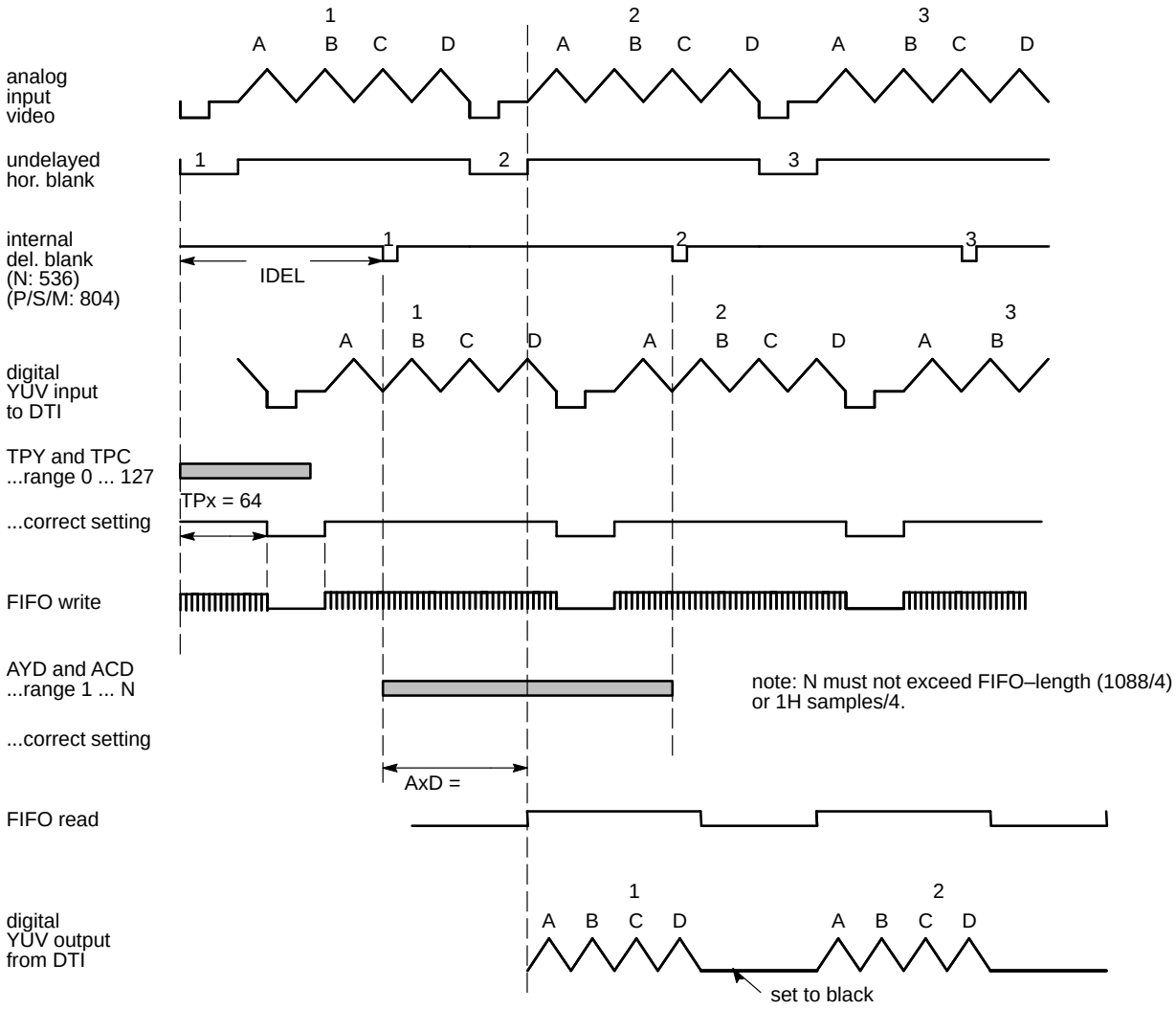


Fig. 2–4: Example: 4:3 Compression



TPY and TPC control the acquisition of active video data (fixed values)
AYD and ACD control the position of the processed picture (user adjustable).

Fig. 2–5: Video and timing signals in 75% compression mode

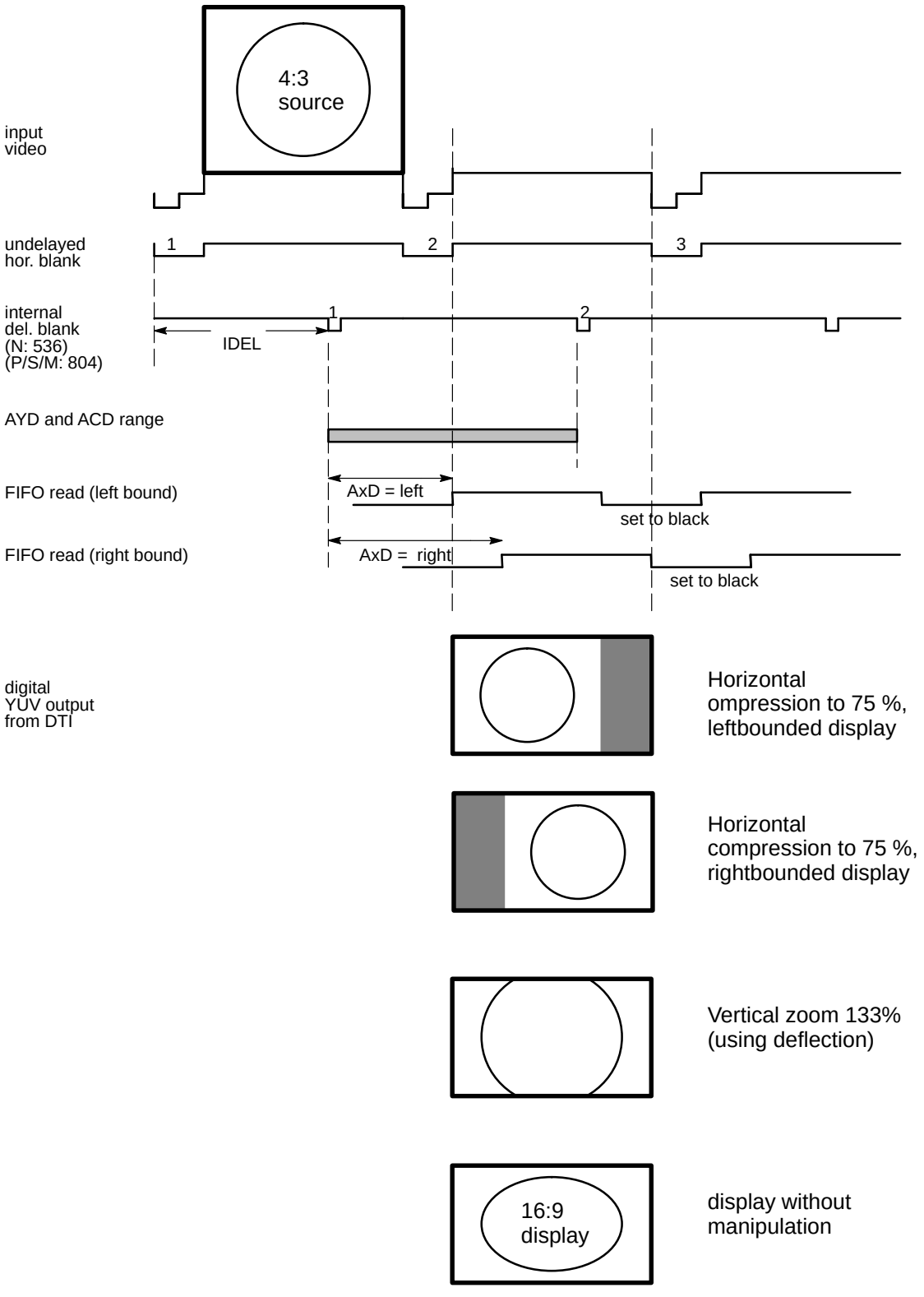


Fig. 2–6: Conversion options 4:3 source → 16:9 display

2.3. Zoom

Zooming an image will increase the number of pixels. Due to constant clock and timing conditions, only a portion of the original image can be displayed. The area of the input image to be zoomed can be selected using the registers AYD and ACD. The range exceeds the leftmost and rightmost edge of the image which allows panning to both sides. The processed data is delayed to 1H to be in phase with the analog input video signal. The range of delay is adjustable by the registers TPY and TPC covering 50 to 78 µs (see Fig. 2–7).

2.4. Orthogonalization & Square Pixel for Computer Application

Some applications such as comp frame memories or multidimensional video processing require an orthogonal data structure. In adjacent lines pixels have to be vertically aligned. In DIGIT 2000 the clock system is subcarrier-locked or free running, resulting in an arbitrary phase between sampling structure and video signal. This so-called skew error is measured in the sync processing circuit of the DPU or VSP and transferred to the DTI 2260 via the skew data input. Inside the DTI 2260 the skew error is compensated using digital interpolation techniques. The frequency response of the luma and chroma filters are shown in Figures 2–2 and 2–3. To enable the skew interpolation, the bit 'SKEN' must be set to '1'. If it is set to '0', the skew value is ignored.

The combination of compressing and orthogonalizing the data may be used to generate square pixel data in an arbitrary decoder clock system, e.g.

NTSC:
decoding with 14.3 MHz = 744 active samples/line.
compressing to 86%, 640 active samples/line.

PAL/SECAM:
decoding with17.7 MHz = 922 active samples/line.
compression to 83%, 766 active samples/line.

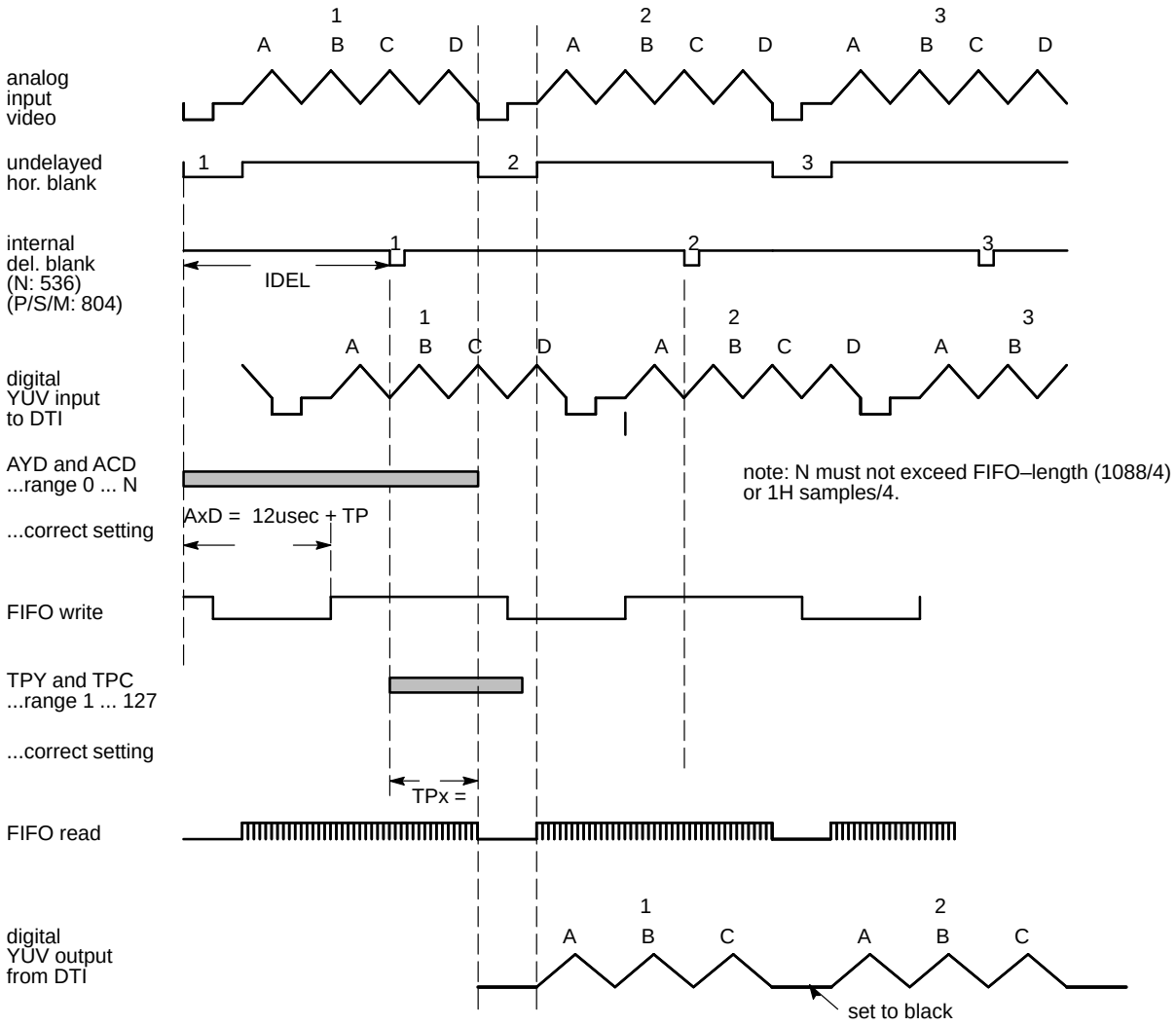
MAC:
decoding with20.25 MHz = 1056 active samples/line.
compression to 72%, 766 active samples/line.

2.5. Sample Rate Conversion

In normal zoom operation, the horizontal start position of the part of the picture to be displayed is defined by the settings of AYD, ACD (see section 2.3), while the number of pixels stored in the FIFO is being calculated automatically depending on the zoom setting (COMPR). This calculation is based on a display of 52 µs active video at a fixed clock frequency and a blanking period of 12 µs always.

In applications with external memory, different clock frequencies for memory write and memory read operation offer the possibility of a sample rate conversion. If the write clock frequency is less than the read clock frequency (upsampling), the number of pixels to be displayed for one line of video increases. Therefore all active video pixel have to be stored inside the DTI's FIFO. The 52 µs limitation (including the 12 µs blanking period) has to be disabled.

In upsampling mode, the timing window for calculating active video pixels can be expanded to a max. of one line of video (64 µs). The length of the data acquisition window is software adjustable in steps of 8. The upsampling mode can be enabled via the SCO bit. For correct adjustments see Table 2–4, section 2.1.6..



AYD, ACD control the acquisition of active video data (user adjustable).
TPY and TPC control the position of the processed picutre (fixed values).

Fig. 2–7: Video and timing signals in 133% zoom mode

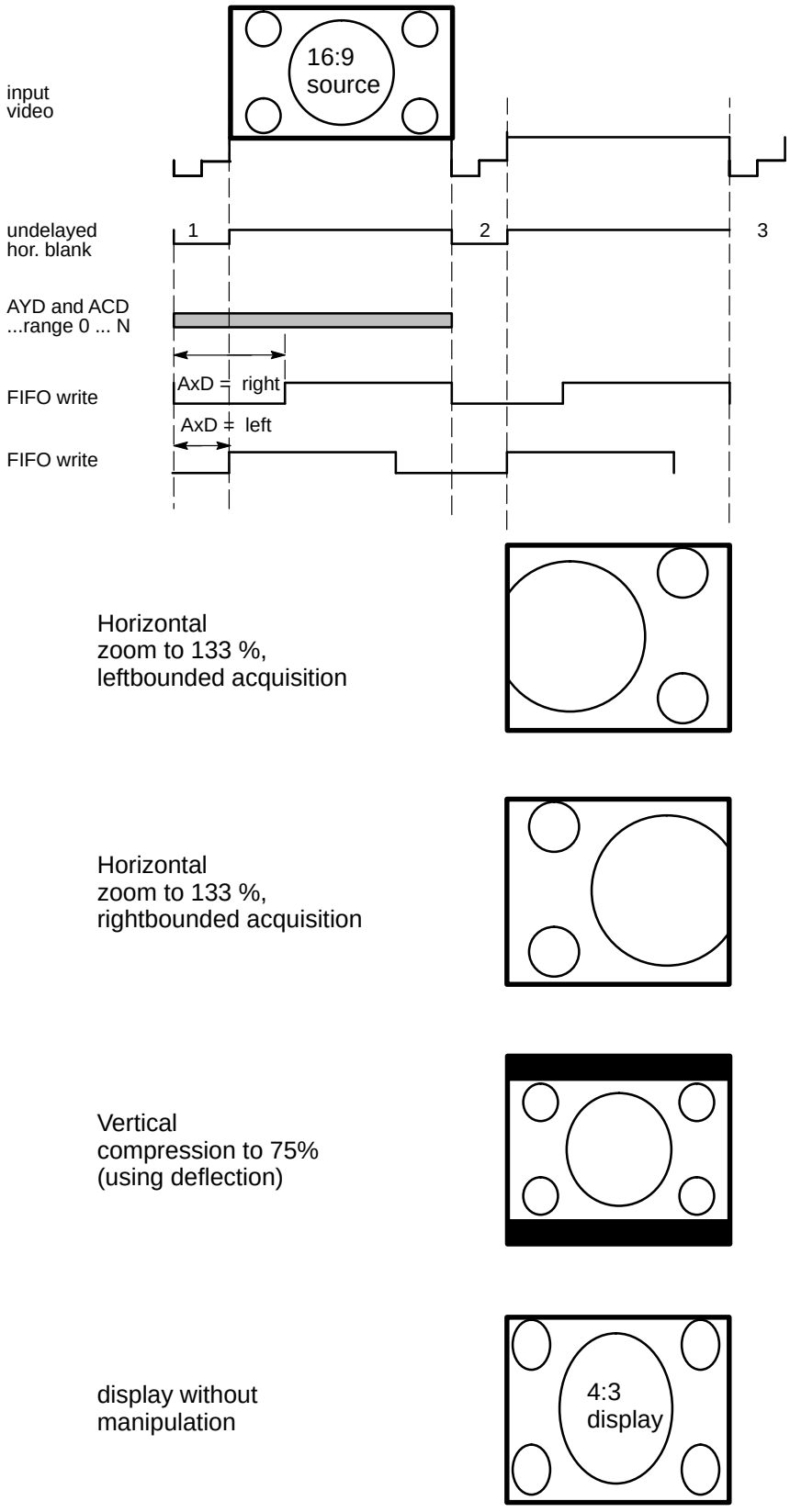


Fig. 2–8: Conversion options 16:9 source → 4:3 display

2.6. Digital Color Transient Improvement

Due to the limited chrominance bandwidth, which is about 1 MHz only in todays TV transmission systems, the sharpness of color transients is visibly reduced, especially if the accompanying luminance transient is small.

The digital color transient improvement circuitry of the DTI 2260 enhances the sharpness of the color transient considerably (see Fig 2–9). After the adjustment of amplitude and phase, the U and V chrominance signals are upsampled from 4:1:1 to 4:2:2. In case of a chrominance transient, the transient improvement circuitry increases the sharpness by calculating a correction signal, which is added to the original signal. In case of a flat chrominance signal, noise can be reduced by a non-linear filter. The luminance and chrominance outputs of the DTI 2260 are converted to analog RGB by the backend IC VDU 2146.

2.6.1. Color Saturation Multiplier and Hue Correction

Usually the adjustment of saturation and hue is done in the color decoding IC of the DIGIT 2000 system. If the DTI 2260 the used, the color saturation multiplier and hue correction circuit of these ICs have to be set to 1, while the adjustments are done in the DTI 2260 (circuitry is identical to the circuitry in the ACVP 2205) .

The color saturation multiplier adjusts the amplitude of the chrominance signal, while the hue correction is done by a rotation of the U and V axles of this signal. The color saturation multiplier works according to the formula

$$V' = V \cdot sat \cdot \cos \alpha - U \cdot sat \cdot \sin \alpha$$

$$U' = V \cdot sat \cdot \sin \alpha + U \cdot sat \cdot \cos \alpha$$

where α is the angle of the rotation and sat is the saturation. The resolution of α is 3° per step. The multiplication of $(sat \cdot \cos \alpha)$ and $(sat \cdot \sin \alpha)$ is done in the CCU.

For $\alpha = 0$, the adjustment range of the color saturation multiplier is 7 bits (128 steps) and the gain is sat/128. For $\alpha \neq 0$, the MSB indicates the sign of the angle (two's complement code).

The color saturation multiplier includes a limiter. Thus the output is limited to +127 or –128 respectively. For a saturation greater than times 1, the reference value of the ACC in the color decoding IC can be increased.

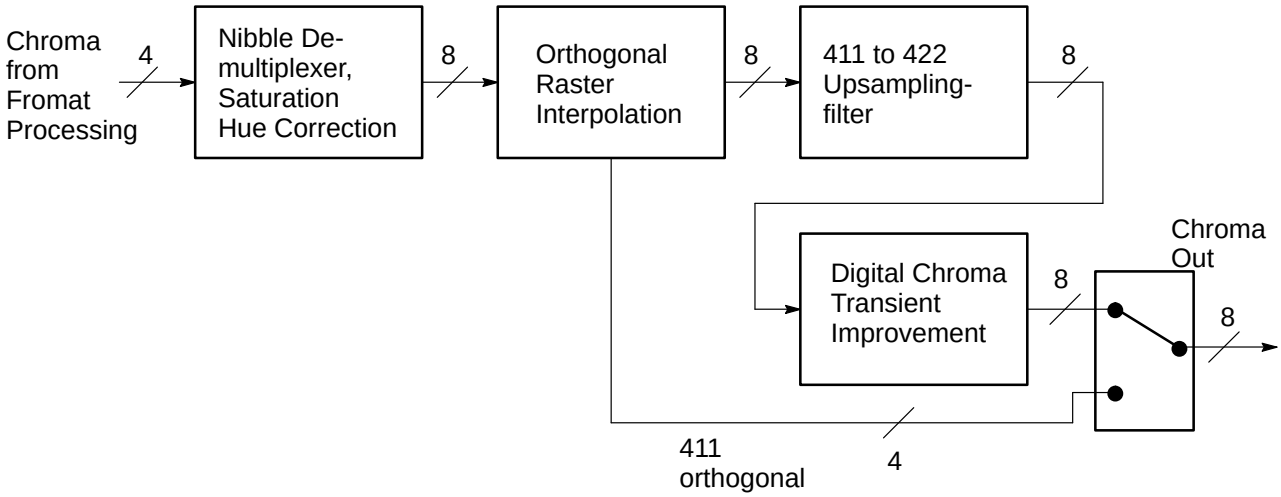


Fig. 2–9: Color Transient improvement block diagram

2.6.2. 4:1:1 to 4:2:2 Interpolation Filters

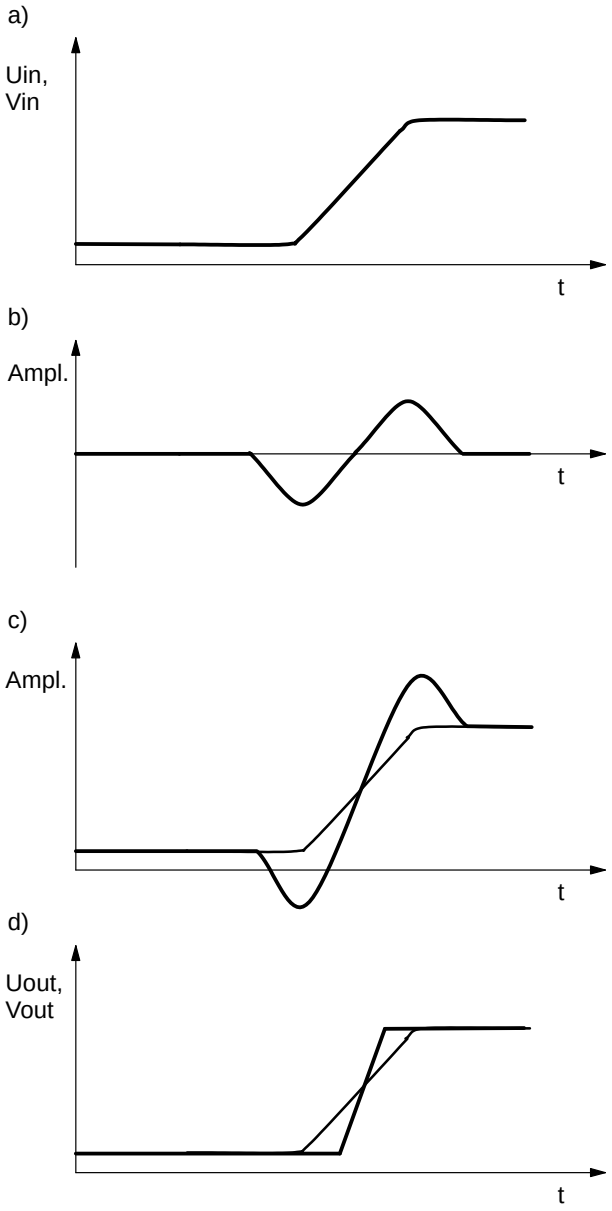
After being adjusted in the saturation and hue correction circuitry, the chrominance signals are upsampled from 4:1:1 to 4:2:2 by a linear phase FIR interpolation filter. The overall frequency characteristic of the interpolation and transient improvement filter is shown in Fig 2–11. This interpolation calculates additional chrominance pixel in between the original samples to enhance the performance of the digital transient improvement.

2.6.3. Digital Chroma Transient Improvement

The digital chroma transient improver is separated into a circuitry for enhancing (sharpening) a chroma transient and the reduction of noise in flat chroma areas.

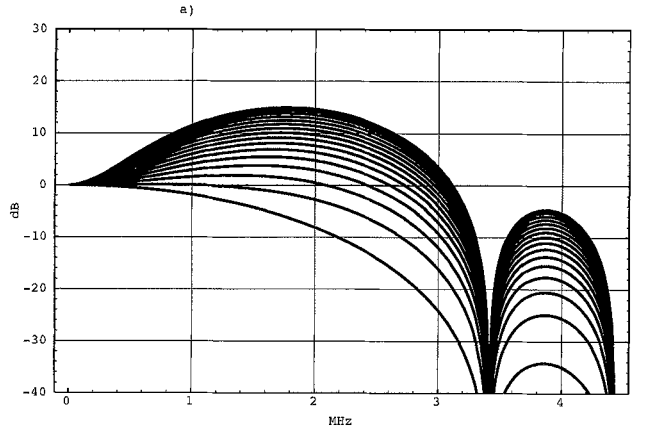
To enhance a chroma transient, a correction signal is calculated by a differentiation of the original chroma signal (see Fig 2–10). Depending on the bandwidth of the input signal, which is different e.g. between PAL and MAC, two filters are selectable via software (DFS bit). These filters determine the frequency characteristic of the correction signal. It's amplitude is adjustable between 0 and +24 dB in 31 steps and independent for U and V samples. Small noise amplitudes in the correction signal are suppressed by an adjustable coring circuitry, before the original signal and the correction signal are added. To eliminate "wrong colors", which are caused by the over- and undershoots, the sharpend chroma signal is limited to a proper value automatically.

In flat chroma areas (no transitions), the signal is improved by a non-linear filter, suppressing peak noise amplitudes. The selection of the non-linear filter or the transient improvement is controlled by the size of the chrominance amplitude step. A software adjustable threshold DTHR selects the transient improvement, when the amplitude step is larger than 2*DTHR. All amplitudes less than 2*DTHR are non-linear filtered.

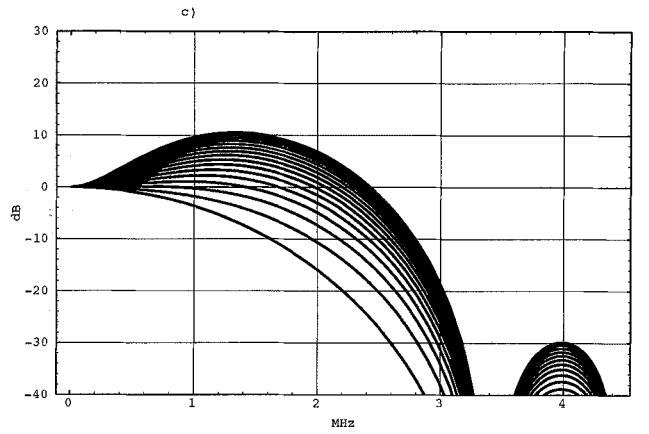


a) U,V input of DTI
b) U,V Correction signal
c) U,V input + Correction signal
d) sharpend and limited U,V

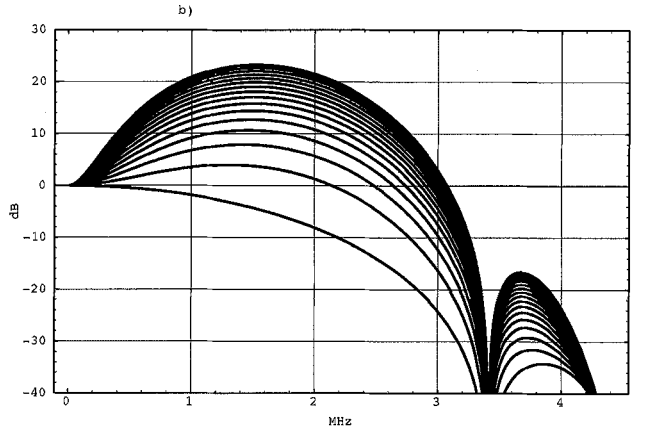
Fig. 2–10: Digital Color Transient Improvement



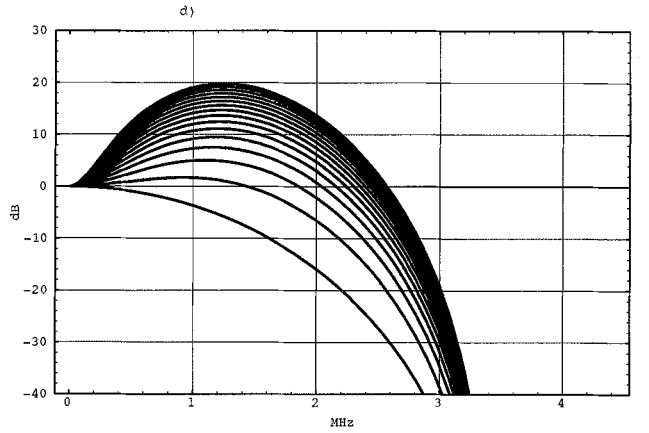
DFS	RS	IRS
1	0	0



DFS	RS	IRS
1	1	1



DFS	RS	IRS
0	0	0



DFS	RS	IRS
0	1	1

Fig. 2–11: Frequency characteristics of the chrominance processing

2.7. Selectable YUV Output Formats

The U and V chrominance samples are transmitted in multiplex operation. Depending on the application, the DTI 2260 provides the following different output formats of the YUV signals (selectable via IM-Bus):

– 4:2:2 output format for standard DIGIT 2000 applications including zoom/compression features, upsampling from 4:1:1 to 4:2:2 and digital color transient improvement

– 4:2:2 orthogonal output format for multimedia applications including zoom/compression features, upsampling from 4:1:1 to 4:2:2 and digital color transient improvement

– 4:1:1 orthogonal output format for multimedia applications including zoom/compression features, but without upsampling and without digital color transient improvement

Additionally the DTI 2260 provides DIGIT2000 and CCIR YUV output levels, which are selectable via software.

A programmable two-dimensional active video signal (AVO) allows the write control of external video memory directly. The characteristic of the YUV and AVO outputs is selectable between open-drain or push-pull.

2.7.1. 4:2:2 DIGIT 2000 Output Format

In the 4:2:2 DIGIT 2000 output format, the U and V samples are non orthogonal (calculated from adjacent pixel, e. g. line n starts with a V pixel and line (n+1) starts with a U pixel (see Table 2–5)

Table 2–5: 4:2:2 DIGIT 2000 output format

Luma Chroma	Y_1	Y_2	Y_3	Y_4
C_7	V_2^7	U_1^7	V_4^7	U_3^7
C_6	V_2^6	U_1^6	V_4^6	U_3^6
C_5	V_2^5	U_1^5	V_4^5	U_3^5
C_4	V_2^4	U_1^4	V_4^4	U_3^4
C_3	V_2^3	U_1^3	V_4^3	U_3^3
C_2	V_2^2	U_1^2	V_4^2	U_3^2
C_1	V_2^1	U_1^1	V_4^1	U_3^1
C_0	V_2^0	U_1^0	V_4^0	U_3^0

note: U_x^Y x = pixel number and y = bit number

2.7.2. 4:2:2 Orthogonal Output Format

The 4:2:2 orthogonal output format is compatible to the industry standard. The U and V samples are skew corrected and interpolated to an orthogonal sampling raster, e.g. every line starts with the current U pixel (see Table 2–6).

Table 2–6: 4:2:2 orthogonal output format

Luma Chroma	Y_1	Y_2	Y_3	Y_4
C_7	U_1^7	V_1^7	U_3^7	V_3^7
C_6	U_1^6	V_1^6	U_3^6	V_3^6
C_5	U_1^5	V_1^5	U_3^5	V_3^5
C_4	U_1^4	V_1^4	U_3^4	V_3^4
C_3	U_1^3	V_1^3	U_3^3	V_3^3
C_2	U_1^2	V_1^2	U_3^2	V_3^2
C_1	U_1^1	V_1^1	U_3^1	V_3^1
C_0	U_1^0	V_1^0	U_3^0	V_3^0

note: U_x^Y x = pixel number and y = bit number

2.7.3. 4:1:1 Orthogonal Output Format

The 4:1:1 orthogonal output format is compatible to the industry standard. The U and V samples are skew corrected and interpolated to an orthogonal sampling raster (see Table 2–7).

Table 2–7: 4:1:1 orthogonal output format

Luma Chroma	Y_1	Y_2	Y_3	Y_4
C_3	U_1^7	U_1^5	U_1^3	U_1^1
C_2	U_1^6	U_1^4	U_1^2	U_1^0
C_1	V_1^7	V_1^5	V_1^3	V_1^1
C_0	V_1^6	V_1^4	V_1^2	V_1^0

note: U_x^Y x = pixel number and y = bit number

2.7.4. YUV Output Levels

The YUV output levels of the DTI 2260 are selectable between DIGIT2000 or CCIR YUV output levels via software. In DIGIT2000 operation, the black level for luma is 32 and the white level is 127 (contrast setting times 1) and the U and V samples are represented in two's complement code. In CCIR operation, the black level for luma is 16 and the white level is 240 (contrast setting has to be set to times 1) and the U and V samples are represented in binary offset code.

2.8. Active Video Output

For external memory control, the DTI 2260 generates the active video output (AVO) signal. It defines a two-dimensional active video window for writing the YUV output data of the DTI 2260 into an external memory. Start and length of this signal in horizontal and vertical direction are adjustable via IM-Bus (see Fig. 2–12). In vertical direction the active video signal is adjustable in steps of 2 video lines, while in horizontal direction it is adjustable in steps of 8 clock cycles.

In horizontal direction, the start position of the AVO signal is software adjustable in reference to the start position of the active YUV data. Depending on the specification of the WRITE ENABLE signal of the external memory, the AVO start is adjustable between 0 and –3 delays in 4 steps.

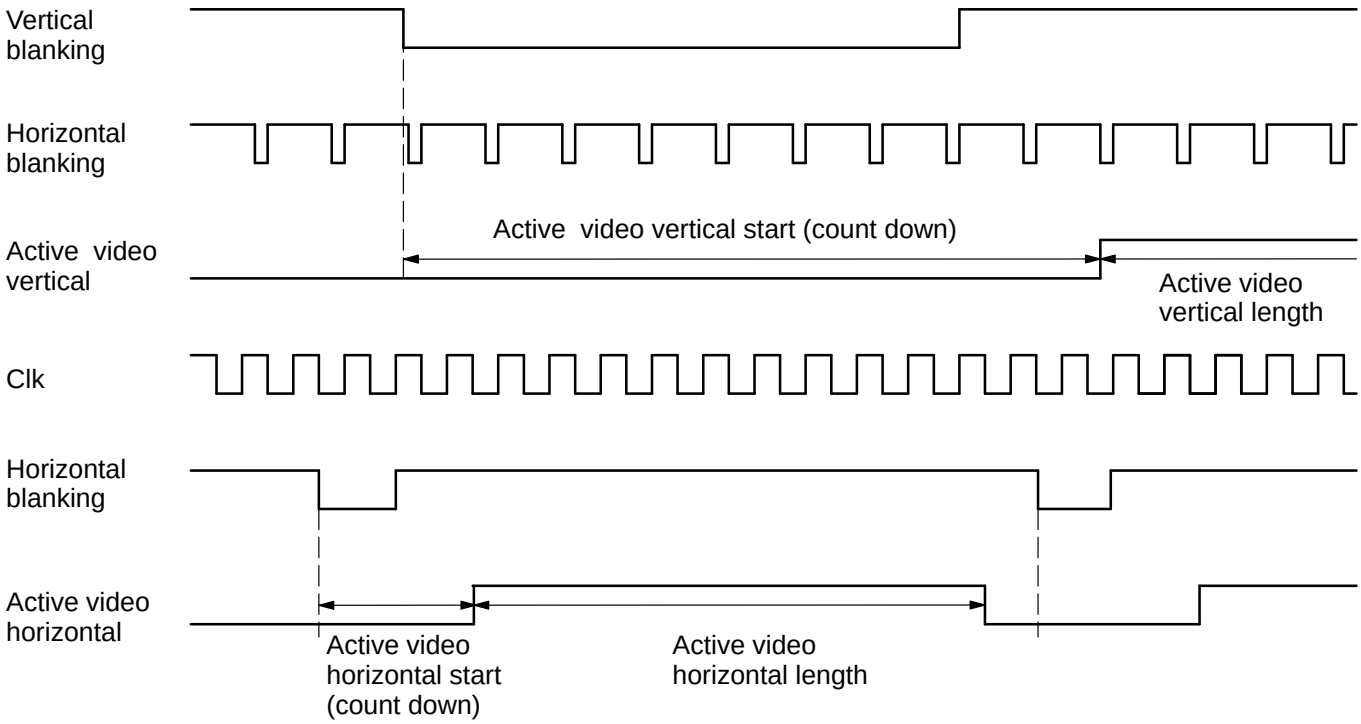


Fig. 2–12: Active video adjustment in horizontal and vertical direction

2.9. Chip Select

Depending on the application, more than one DTI 2260 will be used. Therefore, a chip select function is implemented, which allows to address up to three DTI 2260 ICs independent from each other.

The level (+5V, ground, open) on the CS chip-select pin (pin 18 DIL package) determines the address of the DTI IC. By writing the correct address into the CS-Bits of IM-Bus register 156, the DTI will be active, until a different address is written via the IM-Bus. Table 2–8 shows how to activate the DTI depending on the adjusted level on the CS pin.

Table 2–8: Chip select

CS pin	Value of CS bits
connected to ground	1
open	2
connected to +5 V	3
don't care	0

2.10. Description of the IM Bus

The IM Bus has been designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master, whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, data is bidirectional. Bidirectionality is achieved by using open-drain outputs with On-resistances of 150 Ohm maximum. The 2.5 kOhm pull-up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 3–9 and in section 3.5.2. In the non-operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicting an address transmission, and sets the CL signal to Low level as well, to switch the first bit on the Data line. Thereafter eight address bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two bytes of data are written into the address IC or read out from it, beginning with the LSB.

The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

For future software compatibility, the CCU must write a zero into all bits not used at present. Reading undefined or unused bits, the CCU must adopt “don’t care” behavior.

2.11. Addresses and Commands of the DTI 2260

By means of the IM bus the DTI 2260 communicates with the CCU. From here, the DTI 2260 receives the corresponding commands for the user-activated settings and for alignment values. All addresses and commands are shown in Tables 2–9 and 2–10.

Table 2–9: The IM-bus addresses of the DTI 2260

Bit No. / Param. Address	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
32															ZN Horizontal Standard	
															2	
44	TAL Time active luma														TAC Time active chroma	
	x														x	
45	SAVV Start of active video window veritcal														SAVH Start of acive video window horizontal	
	x														x	
46	LAVV Length of active video window vertical														LAVH Lenght of active video window horizontal	
	x														x	
151	COMPR Compression ratio								SCO Scan Conv.	⊠						
	x								0							
152	⊠			IRS Invers Raster Shift	DFS DTI Filter Select	DTHR DTI Thresold									DCOR DTI Coring	
				1	0	3									1	
153	DPKU DTI Peaking Value for U					DPKV DTI Peaking Value for V					RS Raster Shift	⊠				
	31					31					1	0				
154	SATC Hue Correction times Saturation (sat · cosα)										SATS Hue Correction times Saturation (sat · sinα)					
	127										0					
155	DTIE DTI Enable	TRI Output Disable	SKEN Skew Enable	ISDE Int. Sync Delay Enable	M411 411 Output Enable	OPS Output Select	CCIR CCIR Output Levels	AVOD Adjsutable AVO Delay	⊠							
	1	0	0	0	0	0	0	0								
156	⊠								CS Chip Select	⊠						
									0							
157	AYD Active Luma Delay										TPY Start of acive luma					
	x										x					
158	ACD Active chroma Delay										TPC Start of active chroma					
	x										x					

⊠ = Bits must be set to zero.

Table 2–10: IM-Bus operation

Parameter Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
32	ZN	0,1	2	–	System clock frequency 0 = currently not used 1 = NTSC 14.318 MHz 2 = PAL 17.734 MHz 3 = MAC 20.25 MHz
44	TAL	15–8	159	0	Length of active luma data written into FIFO / read from FIFO
44	TAC	7–0	159	0	Length of active chroma data written into FIFO / read from FIFO
45	SAVV	15–8	0	0	Start of vertical active video window (adjustable in steps of 2 lines)
45	SAVH	7–0	0	0	Start of horizontal active video window (adjustable in steps of 8 pixel)
46	LAVV	15–8	0	0	Length of vertical active video window (adjustable in steps of 2 lines)
46	LAVH	7–0	0	0	Length of horizontal active video window (adjustable in steps of 8 pixel)
151	COMPR	15–8	0	0	Compression / Zoom value adjustable from 0 to 255 0 ... 127 Compression between 100% ... 66% 128 ... 255 Zoom between 100% ... 150%
151	SCO	7	0	0	Sample rate conversion enable 0 = data of reg. 44 not used 1 = data of reg. 44 used
152	IRS	12	0	1	Second additional interpolation filter for PAL
152	DFS	11	0	1	DTI Filter Select 0 = narrow filter selected 1 = broad filter selected
152	DTHR	10–4	0	3	DTI Threshold adjustable from 0 to 127 All chroma amplitudes below 2*DTHR are filtered by the non-linear filter for noise reduction, all amplitudes above are sharpend
152	DCOR	3–0	0	1	DTI Coring adjustable from 0 to 15
153	DPKU	15–11	0	31	DTI Peaking value for U samples
153	DPKV	10–6	0	31	DTI Peaking value for V samples
153	RS	5	0	0	First additional interpolation filter for PAL
154	SATC	15–8	64	–	Saturation and tint (sat · cos (a))
154	SATS	7–0	64	–	Saturation and tint (sat · sin (a))

Table 2–10, continued

Parameter Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
155	DTIE	15	0	1	DTI Enable 0 = DTI disabled 1 = DTI enabled
155	TRI	14	0	0	Tri-state DTI outputs 0 = outputs active 1 = outputs tri-state
155	SKEN	13	0	0	Orthogonal output format enable 0 = DIGIT 2000 output format 1 = Orthogonal output format
155	ISDE	12	0	0	Internal Sync Delay Enable 0 = disabled 1 = enabled
155	M411	11	0	0	4:1:1 output mode (for orthogonal output format only) 0 = 4:2:2 output format 1 = 4:1:1 output format Note: If M411 = 1, DFS has to be set to 1 !
155	OPS	10	0	0	Output Select for Luma/Chroma and AVO 0 = open drain outputs 1 = push-pull outputs
155	CCIR	9	0	0	CCIR Output Level for luma and chroma 0 = DIGIT2000 output levels 1 = CCIR output levels
155	AVOD	8–7	0	0	Adjustable delay between horizontal start of AVO and start of active YUV data 0 = 0 delay between AVO and YUV 1 = –1 delay between AVO and YUV 2 = –2 delays between AVO and YUV 3 = –3 delays between AVO and YUV Note: ”–1 delay” means AVO starts 1 delay before YUV data !
156	CS	7–6	0	0	Chip Select 0 = don’t care 1 = CS pin connected to ground 2 = CS pin open 3 = CS pin connected to +5 V
157	AYD	15–7	0	–	Adjustable luma delay (in steps of 4)
157	TPY	6–0	0	–	Delay of the horizontal blanking to luma data (in steps of 4)
158	ACD	15–7	0	–	Adjustable chroma delay (in steps of 4)
158	TPC	6–0	0	–	Delay of the horizontal blanking to chroma data (in steps of 4)

3. Specifications

3.1. Outline Dimensions

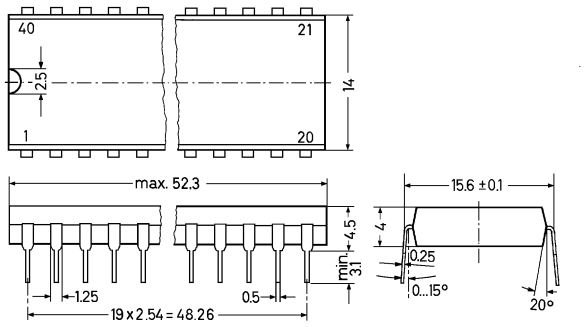


Fig. 3–1: DTI 2260 in 40-Pin DIL Plastic Package
Weight approx. 6 g, Dimensions in mm

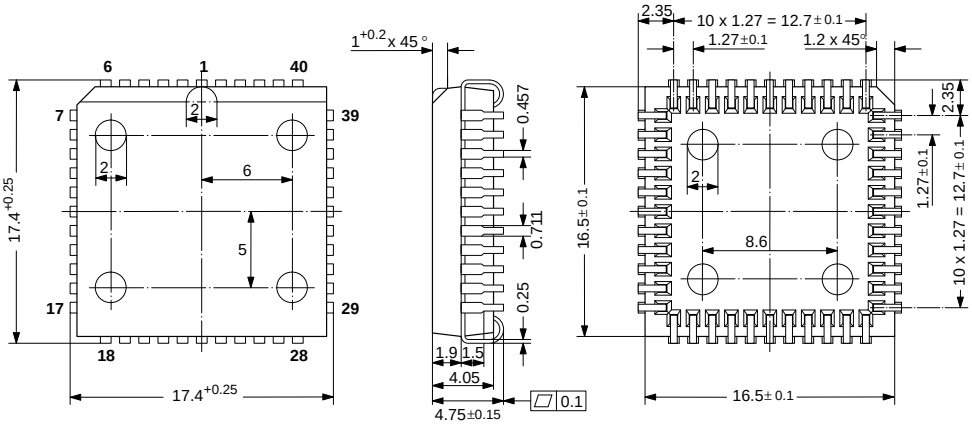


Fig. 3–2: DTI 2260 in 44-Pin PLCC Package
Weight approximately 2.5 g Dimensions in mm

3.2. Pin Connections

3.2.1. 40-Pin DIL Package

1	VSUPD Digital Supply Voltage +5 V
2	MCLK Main Clock Input
3	IMD IM Bus Data Input
4	IMI IM Bus Ident Input
5	IMC IM Bus Clock Input
6	L7 Luma Input (MSB)
7	L6 Luma Input
8	L5 Luma Input
9	L4 Luma Input
10	L3 Luma Input
11	L2 Luma Input
12	L1 Luma Input
13	L0 Luma Input (LSB)
14	C1 Chroma Input
15	C2 Chroma Input
16	C3 Chroma Input (MSB)
17	C0 Chroma Input (LSB)
18	CS Chip Select

19 C7 Chroma Output (MSB in case of 4:2:2 output)

20 C6 Chroma Output

21 C5 Chroma Output

22 C4 Chroma Output

23 C3 Chroma Output (MSB in case of 4:1:1 output)

24 C2 Chroma Output

25 C1 Chroma Output

26 C0 Chroma Output (LSB)

27 L0 Luma Output (LSB)

28 L1 Luma Output

29 L2 Luma Output

30 L3 Luma Output

31 L4 Luma Output

32 L5 Luma Output

33 L6 Luma Output

34 L7 Luma Output (MSB)

35 ACO Active Video Output

36 ODI Outputs Disable Input

37 RESQ $\overline{\text{Reset}}$ Input

38 HU $\overline{\text{Horizontal Blanking}}$ Pulse Input **or** Skew Data Input

39 VBL $\overline{\text{Vertical Blanking}}$ Pulse Input

40 GNDD Digital Ground

3.2.2. 44-Pin PLCC Package

1 VSUPD Supply Voltage +5 V

2 MCLK Main Clock Input

3 IMD IM Bus Data Input

4 IMI IM Bus Ident Input

5 Leave Vacant

6 Leave Vacant

7 IMC IM Bus Clock Input

8 L7 Luma Input (MSB)

9 L6 Luma Input

10 L5 Luma Input

11 L4 Luma Input

12 L3 Luma Input

13 L2 Luma Input

14 L1 Luma Input

15 L0 Luma Input (LSB)

16 C1 Chroma Input

17 C2 Chroma Input

18 C3 Chroma Input (MSB)

19 C0 Chroma Input (LSB)

20 CS Chip Select

21 C7 Chroma Output (MSB in case of 4:2:2 output)

22 C6 Chroma Output

23 Leave Vacant

24 C5 Chroma Output

25 C4 Chroma Output

26 C3 Chroma Output (MSB in case of 4:1:1 output)

27 C2 Chroma Output

28 C1 Chroma Output

29 C0 Chroma Output (LSB)

30 L0 Luma Output (LSB)

31 L1 Luma Output

32 L2 Luma Output

33 L3 Luma Output

34 Leave Vacant

35 L4 Luma Output

36 L5 Luma Output

37 L6 Luma Output

38 L7 Luma Output (MSB)

39 ACO Active Video Output

40 ODI Outputs Disable Input

41 RESQ $\overline{\text{Reset}}$ Input

42 HU $\overline{\text{Horizontal Blanking}}$ Pulse Input **or** Skew Data Input

43 VBL $\overline{\text{Vertical Blanking}}$ Pulse Input

44 GNDD Digital Ground

3.3. Pin Descriptions (pin numbers for 40-pin DIL package)

Pin 1 –VSUPD Supply Voltage +5 V
Pin 1 has to be connected to the +5V digital supply voltage.

Pin 2 – MCLK Main Clock Input (Fig. 3–3)
Via this input, the DTI 2260 receives the required clock signal of 14.3 to 20.3 MHz from the MCU 2600 Clock Generator IC.

Pins 3 to 5 – IM Bus Inputs (Fig. 3–5)
For software control, the DTI 2260 is connected to the CCU Central Control Unit. Pin 3 is the data input, pin 4 is the ident input and pin 5 is clock input.

Pins 6 to 13 and 14 to 17 – Luma and Chroma Inputs (Fig. 3–6)
Via these pins the DTI 2260 receives the digital luma and chroma signals from the YUV bus, i.e. from the luma and chroma outputs of the ACVP 2205 Adaptive Combfilter Video Processor, the SPU 2243 SECAM Processor or the DMA 2271 D2-MAC Decoder.

Pin 18 – CS Chip Select (Fig. 3–8)
The level on this pin (connected to +5 V, ground or open) determines the address of the IC (see section 2.10). If the chip select function is not used, it is recommended to connect pin 18 to ground.

Pins 19 to 26 and 27 to 34 – Chroma and Luma Outputs (Fig. 3–7)
Via these pins the DTI 2260 supplies the processed chroma and luma signals to the VDU 2146.The output operation mode is selectable between open-drain (DIGIT 2000 application) and push-pull via software.

Pin 35 AVO Active Video Output (Fig. 3–7)
Via this the DTI 2260 supplies an active video signal for external memory control. The signal is software programmable (see section 2.9) and active high.

Pin 36 – ODI Outputs Disable Input (Fig. 3–4)
This input serves for fast switchover of the luma and chroma outputs from the active, to the high-impedance state and vice versa. Pin 36 Low means outputs active, and pin 36 High means outputs disabled. If pin 36 is not used, it should be connected to ground (pin 40).

Pin 37 – RESQ $\overline{\text{Reset}}$ Input (Fig. 3–5)
This pin is used for hardware reset. Reset is active at Low level, and at High level the DTI 2260 is ready for operation.

Pin 38 – HU $\overline{\text{Horizontal Blanking}}$ Pulse or Skew Data Input (Fig. 3–5)
This input receives the horizontal blanking pulses from the DPU 25.. Deflection Processor. Instead of $\overline{\text{Horizontal Blanking}}$ also the Skew Data pulse may be used. The skew value has to be connected in order to obtain orthogonal output data.

Pin 39 – VBL $\overline{\text{Vertical Blanking}}$ Pulse Input (Fig. 3–5)
This input receives the vertical blanking pulses from the DPU 25.. Deflection Processor.

Pin 40 – GNDD Digital Ground
This pin has to be be connected to digital ground.

3.4. Pin Circuits

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter “E” means enhancement, the letter “D” depletion.

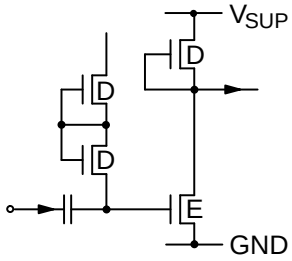


Fig. 3–3: Input Pin 2

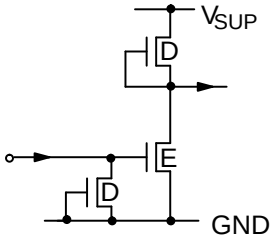


Fig. 3–4: Input Pin 36

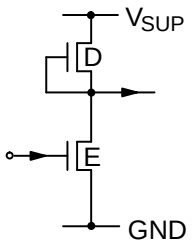


Fig. 3–5:
Input Pins 3 to 5 and 37 to 39

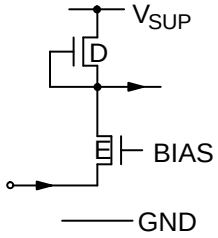


Fig. 3–6:
Input Pins 6 to 13 and 14 to 17

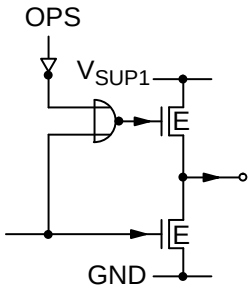


Fig. 3–7:
Output Pins 19 to 35 (open drain or push-pull)

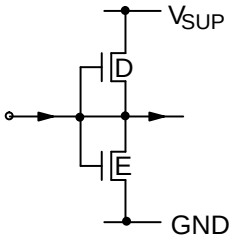


Fig. 3–8:
Chip Select Pin 18

3.5. Electrical Characteristics (pin numbers for 40-pin DIL package)

All voltages are referred to ground.

3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUPD}	Supply Voltage Digital	1	–0.3	6	V
V_I	Input Voltage, all Inputs	–	–0.3 V	V_{SUPD} + 0.3V	–
V_O	Output Voltage, all Outputs	–	–0.3 V	V_{SUPD} + 0.3V	–
I_{LCO}	Luma/Chroma/Active Video Output Current	19 – 35	–	10	mA
C_{LCO}	Load Capacitance on Luma/ Chroma/Active Video Outputs	19 – 35	–	30	pF

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.5.2. Recommended Operating Conditions at T_A = 0 to 65 °C, f_{MCLK} = 14.3 to 20.3 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUPD}	Supply Voltage Digital	1	4.75	5.0	5.25	V
V_{MCLKDC}	MCLK Main Clock Input D.C. Voltage	2	1.5	–	3.5	V
V_{MCLKPP}	MCLK Main Clock Input Peak-to-Peak Voltage		1.0	–	2.5	V
$\frac{t_{MCLKIH}}{t_{MCLKL}}$	MCLK Main Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{MCLKIHL}$	MCLK Main Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{MCLK}}$	–
f_{MCLK}	Main Clock Input Frequency		14.3	–	20.25	MHz
V_{REIL}	$\overline{\text{Reset}}$ Input Low Voltage	37	–	–	0.8	V
V_{REIH}	$\overline{\text{Reset}}$ Input High Voltage		2.4	–	–	V
V_{LCIL}	Luma/Chroma Input Low Voltage	6 to 17	–	–	0.4	V
V_{LCIH}	Luma/Chroma Input High Voltage		1,2	–	–	V
t_{IH}	Luma/Chroma Input Hold Time after MCLK Main Clock Input	6 to 17	18	–	–	ns
t_{IS}	Luma/Chroma Input Setup Time before MCLK Main Clock Input		4	–	–	ns
V_{CSIL}	Chip Select Input Low Voltage	18	–	–	0.6	V
V_{CSIH}	Chip Select Input High Voltage		2.8	–	–	V
V_{COIL}	Output Disable Input, Horizontal/ Vertical Blanking Input Low Voltage	36, 38, 39	–	–	0.6	V
V_{COIH}	Output Disable Input, Horizontal/ Vertical Blanking Input High Voltage		2.0	–	–	V
V_{IMIL}	IM Bus Input Low Voltage	3 to 5	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
f_{IMCLK}	IM Bus Clock Frequency	5	0.05	–	1000	kHz
t_{IM1}	IM Bus Clock Input Delay Time after IM Bus Ident Input		0	–	–	ns
t_{IM2}	IM Bus Clock Input Low Time		500	–	–	ns
t_{IM3}	IM Bus Clock Input High Time		500	–	–	ns
t_{IM4}	IM Bus Clock Input Setup Time before Ident Input High		0	–	–	ns
t_{IM5}	IM Bus Clock Input Hold Time after Ident Input High		0	–	–	ns
t_{IM6}	IM Bus Clock Input Setup Time before Ident End-Pulse Input		1.0	–	–	ns

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM7}	IM Bus Data Input Delay Time after IM Bus Clock Input	3	0	–	–	ns
t_{IM8}	IM Bus Data Input Setup Time before IM Bus Clock Input		0	–	–	ns
t_{IM9}	IM Bus Data Input Hold Time after IM Bus Clock Input		0	–	–	ns
t_{IM10}	IM Bus Ident End-Pulse Low Time	4	1.0	–	–	µs

3.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUPD} = 4.75 to 5.25 V, f_{MCLK} = 14.3 to 20.25 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUPD}	Supply Current	1	–	220	240	mA	T_A = 25 °C
V_{LCOL}	Luma/Chroma/Active Video Output Low Voltage	19 to 35	–	–	0.4	V	I_{LCO} = 3 mA
I_{LCOH}	Luma/Chroma/Active Video Output High Current (open drain mode)		–	–	10	µA	V_{LCO} = 5 V
V_{LCOHpp}	Luma/Chroma/Active Video Output High Voltage (push–pull mode)		2.8	–	–	V	I_{LCO} = 3 mA
t_{LCOLH}	Luma/Chroma/Active Video Output Low to High Transition Time (push-pull mode)		–	–	20	ns	C_L = 30 pF, transition from 0.6 V to 2.6 V
t_{LCOHL}	Luma/Chroma/Active Video Output High to Low Transition Time (push-pull mode)		–	–	20	ns	C_L = 30 pF, transition from 2.6 V to 0.6 V
t_{OH}	Luma/Chroma/Active Video Output Hold Time after MCLK Clock Input		8	–	–	ns	C_L = 30 pF
t_{OD}	Luma/Chroma/Active Video Output Delay Time after MCLK Clock Input		–	–	30	ns	C_L = 30 pF
$-I_{LCIL}$	Luma/Chroma Input Low Current	6 to 17	1.0	–	2.0	mA	V_{LCI} = 0.3 V
V_{LCIL}	Luma/Chroma Input High Voltage		1.2	–	–	V	I_{LCI} = –5 µA
C_{LCI}	Luma/Chroma Input Capacitance		–	7.0	–	pF	
$-I_{CSLC}$	Chip Select Input Low Current	18	–	–	100	µA	V_{CS}= 0.0 V
$-I_{CSHC}$	Chip Select Input High Current	18	–	–	2	mA	V_{CS} = 5.0 V

3.5.4. Waveforms

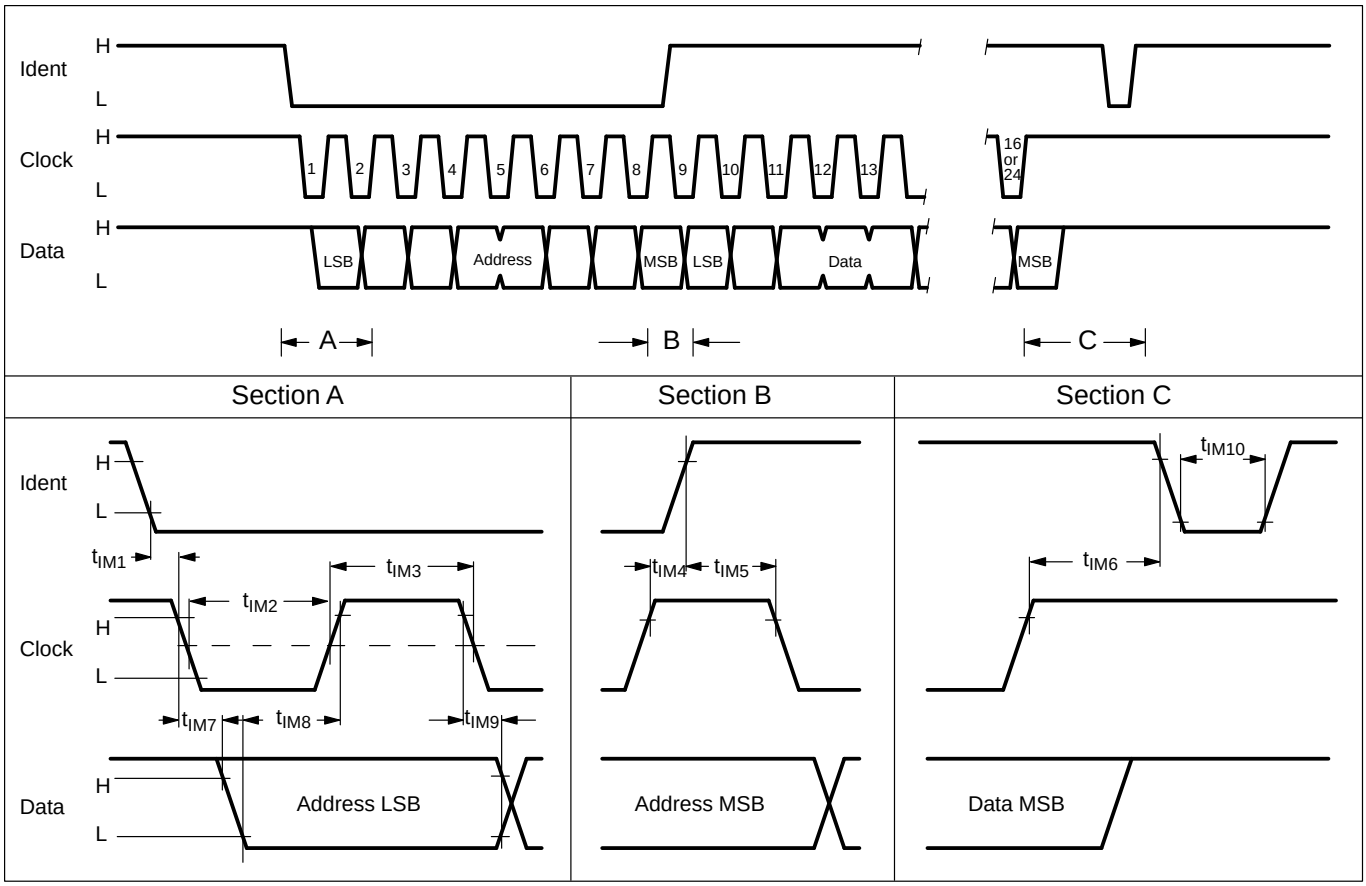


Fig. 3–9: IM bus waveforms

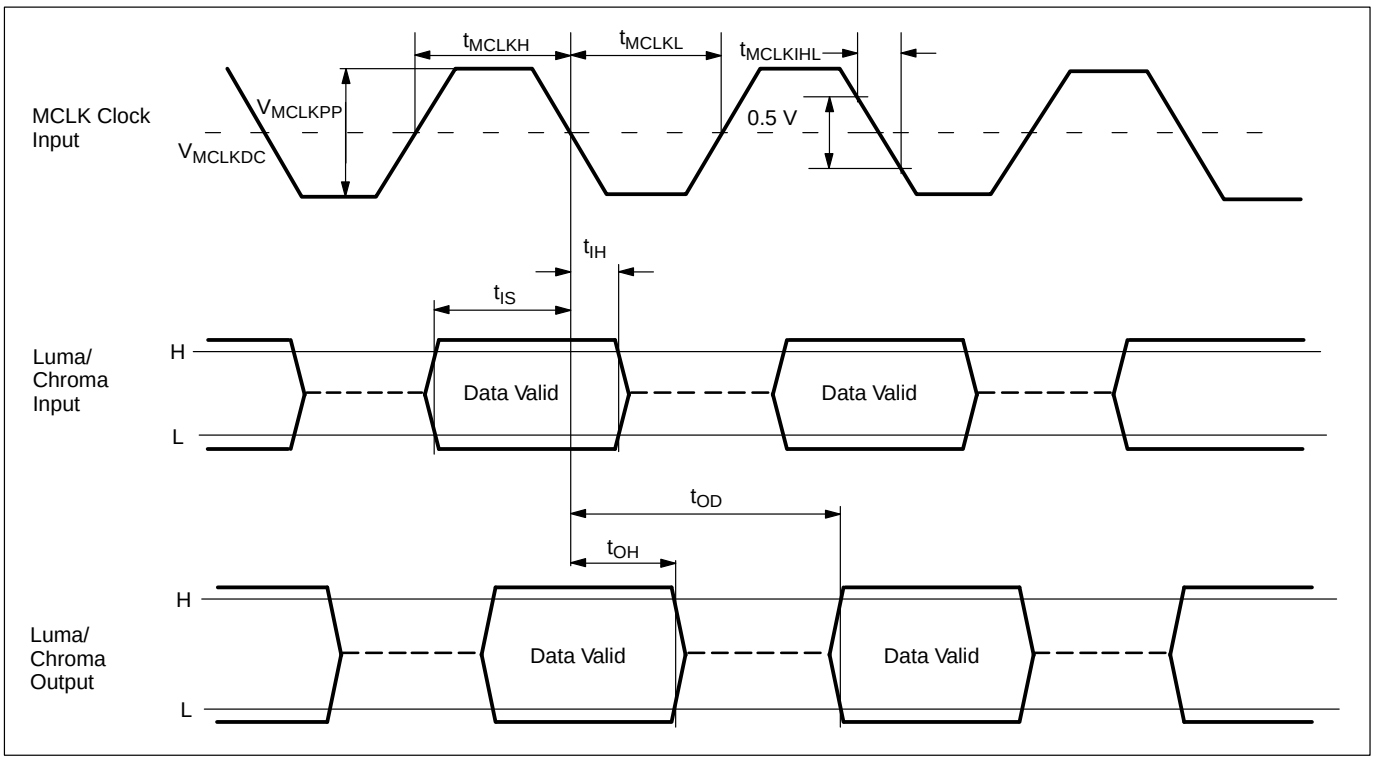


Fig. 3–10: Digital clock, luma and chroma waveforms

3.5.5. The Chroma Demultiplexers

Via pins 17 to 20, the DTI 2260 receives the V and U signals from the C0 to C3 outputs of the color decoder time-multiplexed in 4-bit nibbles (Fig. 3–11). For the digital signal processing, the 4-bit V and U chroma nibbles are demultiplexed to 8-bit signals by the V and U demultiplexers. Both demultiplexers are clocked by the MCLK main clock (pin 2). They are synchronized to the V and U transmission during the vertical blanking period.

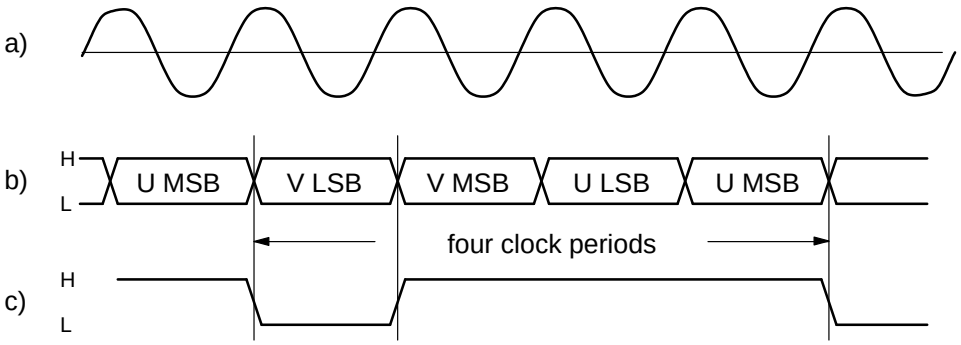


Fig. 3–11: Timing diagram of the multiplexed color difference signal transfer between decoder and DTI 2260

Notes to Fig. 3–11:

a) MCLK main clock signal

b) Muxed color difference signals from PVPU/ACVP/SPU/VSP/DMA to DTI 2260

c) Sync pulse on C0 output during sync time in vertical blanking interval.

4. DTI 2260 Documentation History

1. Final data sheet: “DTI 2260 Digital Transient Improvement Processor, Oct. 13, 1994, 6251-348-1DS. First release of the final data sheet.

ITT Semiconductors Group
World Headquarters
INTERMETALL
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174

Printed in Germany
by Simon Druck GmbH & Co., Freiburg (12/94)
Order No. 6251-348-1DS

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End of Data Sheet

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