National Semiconductor

June 25, 2009

DS64BR401

Quad Bi-Directional Transceiver with Equalization and De-Emphasis

General Description

The DS64BR401 is a quad lane bi-directional signal conditioning transceiver suitable for 6.0/3.0/1.5 Gbps SATA/SAS and other high-speed bus applications with data rates up to 6.4 Gbps. The device performs both receive equalization and transmit de-emphasis on each of its 8 channels to compensate for channel loss, allowing maximum flexibility of physical placement within a system. The receiver's continuous time linear equalizer (CTLE) provides a boost of up to +33 dB at 3 GHz and is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium. The transmitter features a programmable output de-emphasis driver and allows amplitude voltage levels to be selected from 600 mVp-p to 1200 mVp-p to suit multiple application scenarios. This Low Power Differential Signaling (LPDS) output driver is a power efficient implementation that maintains compatibility with AC coupled CML receiver. The programmable settings can be applied via pin settings or SMBus interface.

To enable seamless upgrade from SAS/SATA 3.0 Gbps to 6.0 Gbps data rates without compromising physical reach, DS64BR401 automatically detects the incoming data rate and selects the optimal de-emphasis pulse width. The device detects the out-of-band (OOB) idle and active signals of the SAS/SATA specification and passes through with minimum signal distortion.

With a typical power consumption of 200 mW/lane (100 mW/channel) at 6.4 Gbps, and control to turn-off unused channels, the DS64BR401 is part of National's PowerWise family of energy efficient devices.

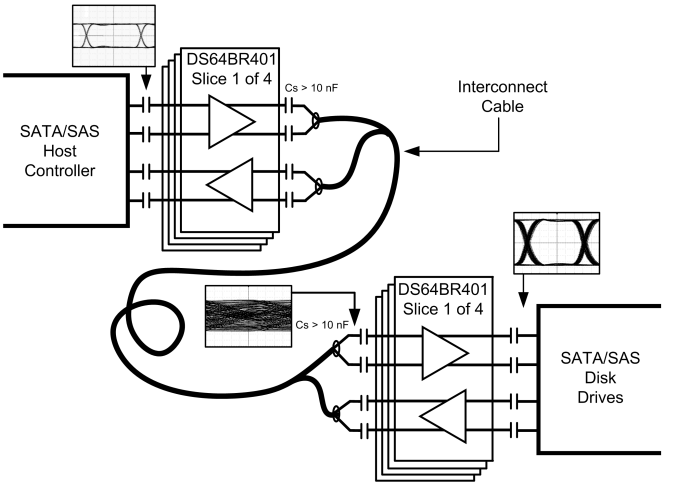
Features

- Quad lane bi-directional transceiver up to 6.4 Gbps rate
- Signal conditioning on input and output for extended reach
- Adjustable receive equalization up to +33 dB gain
- Adjustable transmit de-emphasis up to −12 dB
- Adjustable transmit VOD (600 mVp-p to 1200 mVp-p)
- <0.25 UI of residual DJ at 6.4 Gbps with 40” FR4 trace
- Automatic de-emphasis scaling based on rate detect
- SATA/SAS: OOB signal pass-through, <3 ns (typ) envelope distortion
- Adjustable electrical IDLE detect threshold
- Low power (100 mW/channel), per-channel power down
- Programmable via pin selection or SMBus interface
- Single supply operation at 2.5V ±5%
- >6 kV HBM ESD Rating
- 3.3V LVCMOS input tolerant for SMBus interface
- High speed signal flow–thru pinout package: 54-pin LLP (10 mm x 5.5 mm)

Applications

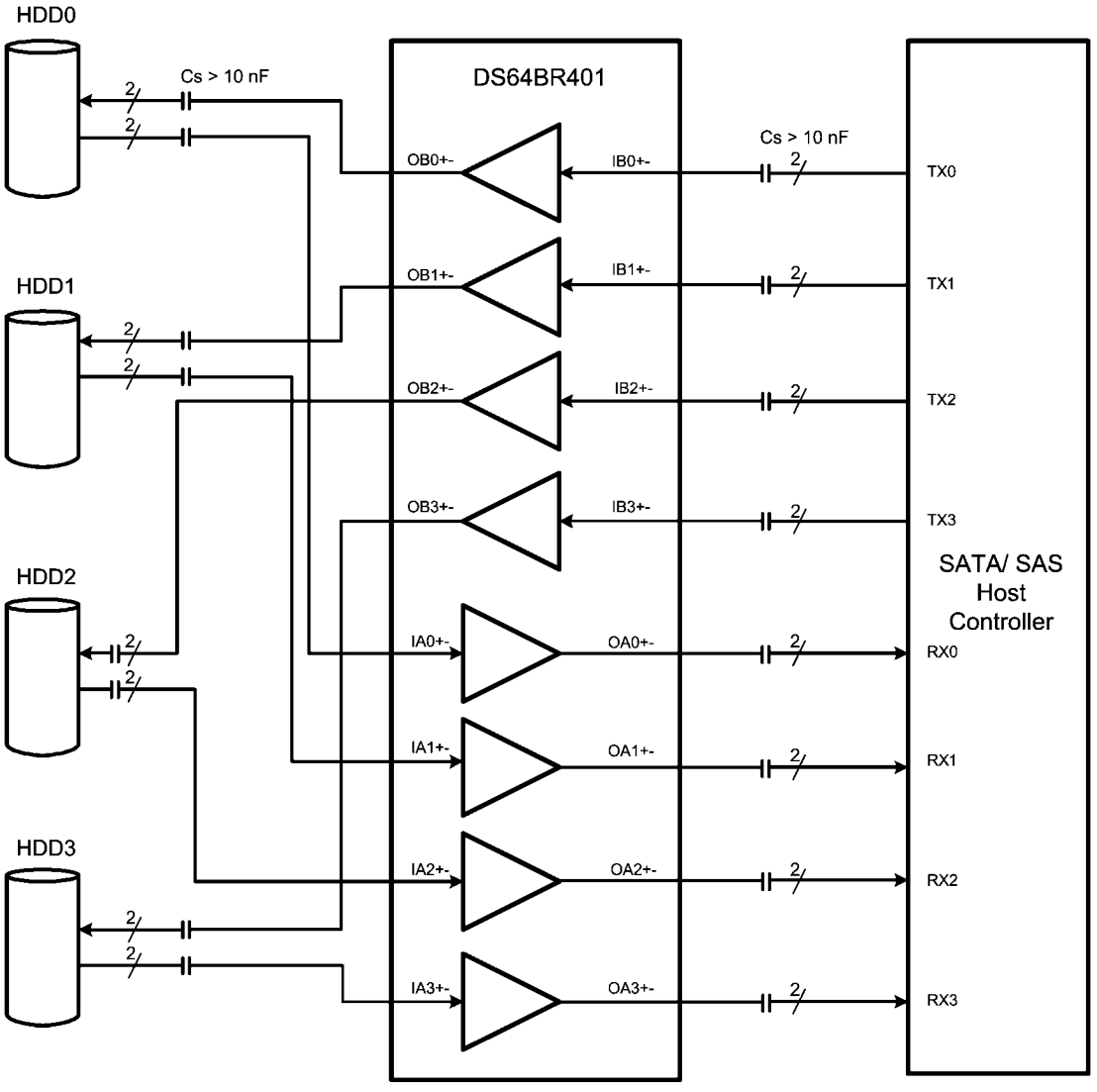
- SATA (1.5, 3.0 and 6 Gbps)
- SAS (1.5, 3.0 and 6 Gbps)
- XAUI (3.125 Gbps), RXAUI (6.25 Gbps)
- sRIO – Serial Rapid I/O
- Fibre Channel (4.25 Gbps)
- 10GBase-CX4, InfiniBand 4x (SDR & DDR)
- QSFP active copper cable modules
- High-speed active cable and FR-4 backplane traces

Typical Cable Application



DS64BR401 Quad Bi-directional Transceiver with Equalization and De-Emphasis

Typical Application Connection Diagram



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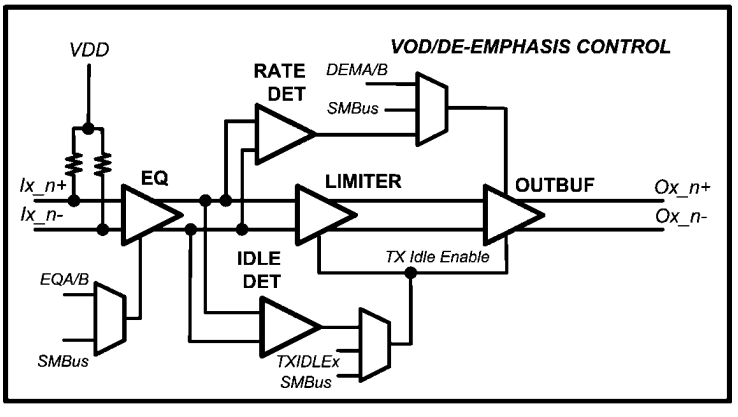
Block Diagram - Detail View of the each channel (1 of 8)



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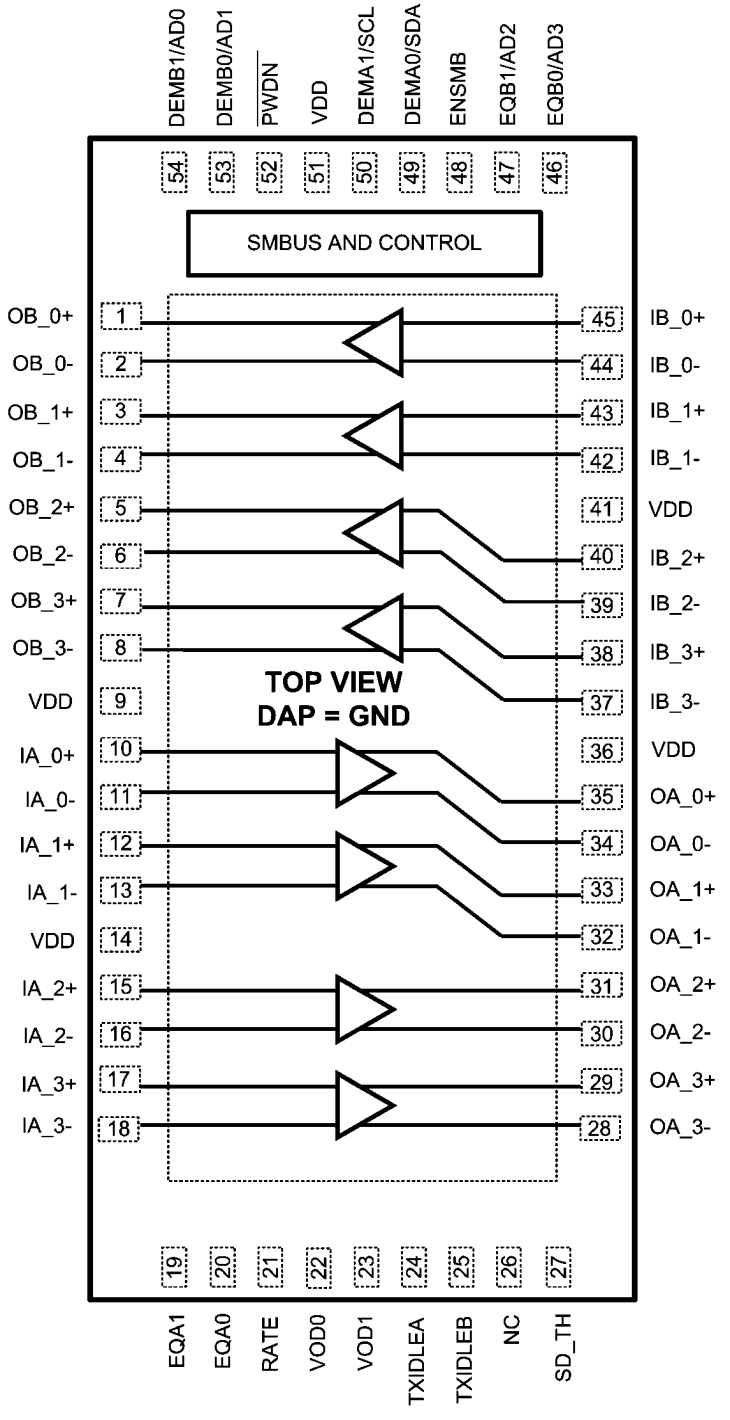
Pin Diagram



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DS64BR401 Pin Diagram 54L LLP

Ordering Information

NSID	Qty	Spec	Package
DS64BR401SQ	Tape & Reel Supplied As 2,000 Units	NOPB	SQA54A
DS64BR401SQE	Tape & Reel Supplied As 250 Units	NOPB	SQA54A

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Pin Descriptions
Differential High Speed I/O's			
IA_0+, IA_0- , IA_1+, IA_1-, IA_2+, IA_2-, IA_3+, IA_3-	10, 11 12, 13 15, 16 17, 18	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled.
OA_0+, OA_0-, OA_1+, OA_1-, OA_2+, OA_2-, OA_3+, OA_3-	35, 34 33, 32 31, 30 29, 28	O, LPDS	Inverting and non-inverting low power differential signaling (LPDS) 50Ω outputs with de-emphasis. Compatible with AC coupled CML inputs.
IB_0+, IB_0- , IB_1+, IB_1-, IB_2+, IB_2-, IB_3+, IB_3-	45, 44 43, 42 40, 39 38, 37	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled.
OB_0+, OB_0-, OB_1+, OB_1-, OB_2+, OB_2-, OB_3+, OB_3-	1, 2 3, 4 5, 6 7, 8	O, LPDS	Inverting and non-inverting low power differential signaling (LPDS) 50Ω outputs with de-emphasis. Compatible with AC coupled CML inputs.
Control Pins — Shared (LVCMOS)			
ENSMB	48	I, LVCMOS w/ internal pull-down	System Management Bus (SMBus) enable pin. When pulled high provide access internal digital registers that are a means of auxiliary control for such functions as equalization, de-emphasis, VOD, rate, and idle detection threshold. When pulled low, access to the SMBus registers are disabled and SMBus function pins are used to control the Equalizer and De-Emphasis. Please refer to “SMBus configuration Registers” section and Electrical Characteristics - Serial Management Bus Interface for detail information.
ENSMB = 1 (SMBUS MODE)			
SDA, SCL	49, 50	I, LVCMOS	ENSMB = 1 The SMBus SDA (data input/output bi-directional) and SCL (clock input) pins are enabled.
AD[3:0]	46, 47, 53, 54	I, LVCMOS w/ internal pull-down	ENSMB = 1 SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs. See section — System Management Bus (SMBus) and Configuration Registers for additional information.
ENSMB = 0 (NORMAL PIN MODE)			
EQA0, EQA1 EQB0, EQB1	20, 19 46, 47	I, Float, LVCMOS	EQA/B, 3–level controls the level of equalization of the A/B sides. The EQA/B pins are active only when ENSMB is de-asserted (Low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes high the SMBus registers provide independent control of each lane. See *Table 1*
DEMA0, DEMA1 DEMB0, DEMB1	49, 50 53, 54	I, Float, LVCMOS	DEMA/B, 3–level controls the level of de-emphasis of the A/B sides. The DEMA/B pins are only active when ENSMB is de-asserted (Low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes High the SMBus registers provide independent control of each lane. See *Table 2*

Pin Name	Pin Number	I/O, Type	Pin Descriptions
Control Pins — Both Modes (LVCMOS)			
RATE	21	I, Float, LVCMOS	RATE, 3–level controls the pulse width of de-emphasis of the output. RATE = 0 forces 3 Gbps, RATE = 1 forces 6 Gbps, RATE = Float enables auto rate detection and the pulse width (pull-back) is set appropriately after each exit from IDLE. This requires the transition from IDLE to ACTIVE state — OOB signal. See *Table 2*
TXIDLEA,TXIDLEB	24, 25	I, Float, LVCMOS	TXIDLEA/B, 3–level controls the driver output. TXIDLEA/B = 0 disables the signal detect/squelch function for all A/B outputs. TXIDLEA/B = 1 forces the outputs to be muted (electrical idle). TXIDLEA/B = Float enables the signal auto detect/squelch function and the signal detect voltage threshold level can be adjusted using the SD_TH pin. See *Table 3*
VOD0, VOD1	22, 23	I, LVCMOS w/ internal pull-down	VOD[1:0] adjusts the output differential amplitude voltage level. VOD[1:0] = 00 sets output VOD = 600 mV (Default) VOD[1:0] = 01 sets output VOD = 800 mV VOD[1:0] = 10 sets output VOD = 1000 mV VOD[1:0] = 11 sets output VOD = 1200 mV
$\overline{\text{PWDN}}$	52	I, LVCMOS	$\overline{\text{PWDN}}$ = 0 enables the device (normal operation). $\overline{\text{PWDN}}$ = 1 disables the device (low power mode). Pin must be driven to a logic low at all time or normal operation is not guaranteed.
Analog			
SD_TH	27	I, ANALOG	Threshold select pin for electrical idle detect threshold. Float pin for typical default 130 mVp-p (differential), otherwise connect resistor from SD_TH to GND to set threshold voltage. See *Table 4*, *Figure 5*
Power			
VDD	9, 14, 36, 41, 51	Power	Power supply pins. 2.5 V +/-5%
GND	DAP	Power	DAP is the large metal contact at the bottom side, located at the center of the 54 pin LLP package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.
NC	26		No Connect — Leave pin open

1 = HIGH, 0 = LOW, FLOAT = 3rd input state.

Don't drive FLOAT pin; pin is internally biased to mid level with 50 kΩ pull-up/pull-down.

Internal pulled-down = Internal 30 kΩ pull-down resistor to GND is present on the input.

Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (VDD)	-0.5V to +3.0V
LVCMOS Input/Output Voltage	-0.5V to +4.0V
CML Input Voltage	-0.5V to (VDD+0.5V)
LPDS Output Voltage	-0.5V to (VDD+0.5V)
Analog (SD_TH)	-0.5V to (VDD+0.5V)
Junction Temperature	+125°C
Storage Temperature	-40°C to +125°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
SQA54A Package	4.21 W
Derate SQA54A Package	52.6mW/°C above +25°C
ESD Rating	
HBM, STD - JESD22-A114C	≥6 kV
MM, STD - JESD22-A115-A	≥250 V
CDM, STD - JESD22-C101-C	≥1250 V
Thermal Resistance	
θ_{JC}	11.5°C/W
θ_{JA}, No Airflow, 4 layer JEDEC	19.1°C/W

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
VDD to GND	2.375	2.5	2.625	V
Ambient Temperature	-10	25	+85	°C
SMBus (SDA, SCL)	0		3.6	V
CML Differential Input Voltage	0		2.0	Vp-p
Supply Noise Tolerance up to 50 MHz, (Note 4)		100		mVp-p

Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless other specified. (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER						
PD	Power Dissipation	$\overline{PWDN}$ = 0, EQx = 0, DEMx = 0 dB, K28.5 pattern VOD = 1.0 Vp-p		758	950	mW
		$\overline{PWDN}$ = 1, ENSMB = 0		0.92	1.125	mW
LVCMOS / LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		3.6	V
V_{IL}	Low Level Input Voltage		0		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3V, Inputs OPEN: SDA, SCL, $\overline{PWDN}$	-15		+15	µA
		V_{IN} = 3.3V, Inputs with PULL-DOWN and FLOAT — mid level	-15		+120	uA
I_{IL}	Input Low Current	V_{IN} = 0V, Inputs OPEN: SDA, SCL, $\overline{PWDN}$ and with PULL-DOWN	-15		+15	µA
		V_{IN} = 0V, Inputs with FLOAT — mid level	-80		+15	uA
CML RECEIVER INPUTS (IN_n+, IN_n-)						
$RL_{RX-DIFF}$	Rx Differential Return Loss (SDD11), (Note 2)	150 MHz – 1.5 GHz		-20		dB
		150 MHz – 3.0 GHz		-13.5		
		150 MHz – 6.0 GHz		-8		
RL_{RX-CM}	Rx Common Mode Input Return Loss (SCC11)	150 MHz – 3.0 GHz, (Note 2)		-10		dB
R_{RX-IB}	Rx Impedance Balance (SDC11)	150 MHz – 3.0 GHz, (Note 2)		-27		dB
I_{IN}	Maximum current allowed at IN+ or IN- input pin.		–30		+30	mA
R_{IN}	Input Resistance	Single ended to V_{DD}, (Note 2)		50		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{ITD}	Input Differential Impedance between IN+ and IN-	DC tested, (Note 2)	85	100	115	Ω
R_{ITIB}	Input Differential Impedance Imbalance	DC tested, (Note 2)			5	Ω
R_{ICM}	Input Common Mode Impedance	DC tested, (Note 2)	20	25	35	Ω
$V_{RX-DIFF}$	Differential Rx peak to peak voltage	DC voltage, SD_TH = 20 kΩ to GND	0.1		1.2	V
V_{RX-SD_TH}	Electrical Idle detect threshold (differential)	SD_TH = Float, (Note 6), *Figure 5*	40		175	mVp-p
LPDS OUTPUTS (OUT_n+, OUT_n-)						
V_{OD}	Output Voltage Swing	R_L = 50 Ω ±1% to GND (AC coupled with 10 nF), 6.4 Gbps, (Note 5) DEMx = 0 dB, VOD[1:0] = 00	500	600	700	mV_{P-P}
		VOD[1:0] = 11	1100	1265	1450	mV_{P-P}
V_{OCM}	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω termination, (Note 2)		V_{DD} – 1.4		V
T_{TX-RF}	Transmitter Rise/ Fall Time	20% to 80% of differential output voltage, measured within 1” from output pins, (Notes 2, 5), *Figure 1*		67	85	ps
$T_{RF-DELTA}$	Tx rise/fall mismatch	20% to 80% of differential output voltage, (Notes 2, 5)			0.1	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss (SDD22), (Note 2)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, 150 MHz – 1.5 GHz		-11		dB
		150 MHz – 3.0 GHz		-10		
		150 MHz – 6.0 GHz		-5		
RL_{TX-CM}	Tx Common Mode Return Loss (SCC22)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, (Note 2) 50 MHz – 3.0 GHz		-10		dB
R_{TX-IB}	Tx Impedance Balance (SDC22)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, (Note 2) 50 MHz – 3.0 GHz		-30		dB
$I_{TX-SHORT}$	Tx Output Short Circuit Current Limit	OA/B_n = GND			90	mA
R_{OTD}	Output Differential Impedance between OUT+ and OUT-	DC tested, (Note 2)	85	100	125	Ω
R_{OTIB}	Output Differential Impedance Imbalance	DC tested, (Note 2)			5	Ω
R_{OCM}	Output Common Mode Impedance	DC tested, (Note 2)	20	25	35	Ω
$V_{TX-CM-DELTA}$	Common Mode Voltage Delta between active burst and electrical Idle of an OOB signal	(Note 7)			±40	mV
T_{DI}	Max time to transition to valid electrical idle after leaving active burst in OOB signaling	VIN = 800 mVp-p, repeating 1100b (D24.3) pattern at 3 Gbps, SD_TH = Float, *Figure 3*		6.5	9.5	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{ID}	Max time to transition to valid active burst after leaving idle in OOB signaling	VIN = 800 mVp-p, repeating 1100b (D24.3) pattern at 3 Gbps, SD_TH = Float, *Figure 3*		5.5	8	ns
T_{PD}	Differential Propagation Delay (Low to High and High to Low Edge)	Propagation delay measured at midpoint crossing between input to output, *Figure 2*, EQx[1:0] = 11, DEMx[1:0] = –6 dB	150	200	250	ps
		EQx[1:0] = OFF, DEMx[1:0] = 0 dB	120	170	220	ps
T_{LSK}	Lane to Lane Skew in a Single Part	V_{DD} = 2.5 V, T_A = 25°C			27	ps
T_{PPSK}	Part to Part Propagation Delay Skew	V_{DD} = 2.5 V, T_A = 25°C			35	ps
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 40” 4–mil FR4 trace, EQx[1:0] = 0F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (Note 2)		0.12	0.25	UI_{P-P}
DJ2	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 12 meters (30 AWG), EQx[1:0] = 1F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (Note 2)		0.05	0.15	UI_{P-P}
DJ3	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 40” 4–mil FR4 trace, EQx[1:0] = 0F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (Note 2)		0.05	0.12	UI_{P-P}
DJ4	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 12 meters (30 AWG), EQx[1:0] = 1F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (Note 2)		0.06	0.16	UI_{P-P}
RJ	Random Jitter	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, Repeating 1100b (D24.3) pattern		0.5		psrms

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DE-EMPHASIS						
DJ5	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch amplitude = 0.8 to 1.2 Vp–p, 10” 4–mil FR4 trace, EQx[1:0] = OFF, DEMx[1:0] = –6 dB, VOD = 1.0 Vp-p, K28.5, RATE = 1(Note 2)		0.09	0.20	UI_{P-P}
DJ6	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch amplitude = 0.8 to 1.2 Vp–p, 20” 4–mil FR4 trace, EQx[1:0] = OFF, DEMx[1:0] = –6 dB, VOD = 1.0 Vp-p, K28.5, RATE = 0(Note 2)		0.07	0.18	UI_{P-P}

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

Note 2: Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Note 5: Measured with clock-like {11111 00000} pattern.

Note 6: Measured at package pins of receiver. The 130 mVp-p is a typical threshold level and does not include hysteresis, thus less than 40 mVp-p is IDLE, greater than 175 mVp-p is ACTIVE. SD_TH pin connected with resistor to GND overrides this default setting.

Note 7: Common-mode voltage (VCM) is expressed mathematically as the average of the two signal voltages with respect to local ground.

VCM = (A + B) / 2, A = OUT+, B = OUT-.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{OL}	Data (SDA) Low Level Output Voltage	I_{OL} = 3mA			0.4	V
V_{IL}	Data (SDA), Clock (SCL) Input Low Voltage				0.8	V
V_{IH}	Data (SDA), Clock (SCL) Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(Note 8)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SDC	(Notes 8, 9)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	$V_{DD3.3}$, (Notes 8, 9, 10)		2000		Ω
		$V_{DD2.5}$, (Notes 8, 9, 10)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS. See *Figure 4*						
FSMB	Bus Operating Frequency	(Note 11)	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout	(Note 11)	25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period	(Note 11)	4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)	(Note 11)			2	ms
t_F	Clock/Data Fall Time	(Note 11)			300	ns
t_R	Clock/Data Rise Time	(Note 11)			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	(Note 11)			500	ms

Note 8: Recommended value. Parameter not tested in production.

Note 9: Recommended maximum capacitance load per bus segment is 400pF.

Note 10: Maximum termination voltage should be identical to the device supply voltage.

Note 11: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Timing Diagrams

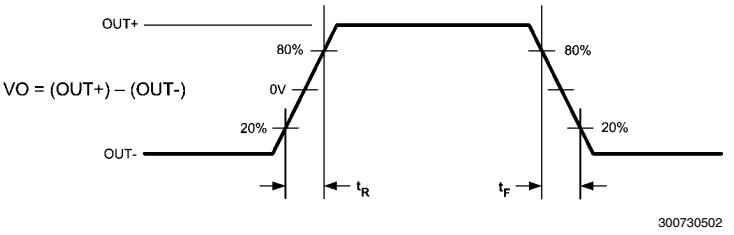


FIGURE 1. LPDS Output Transition Times

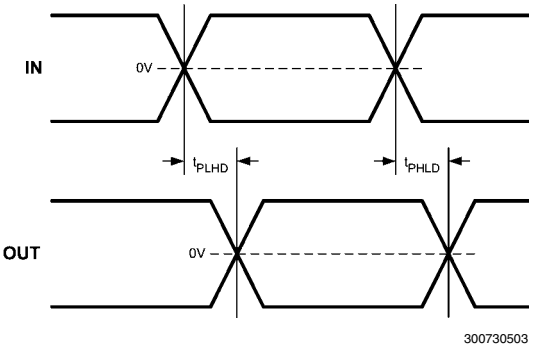


FIGURE 2. Propagation Delay Timing Diagram

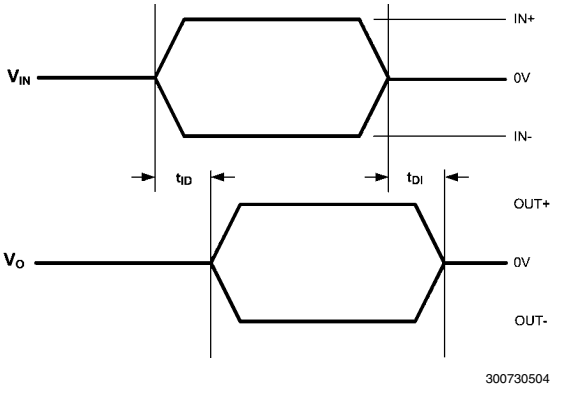


FIGURE 3. Idle Timing Diagram

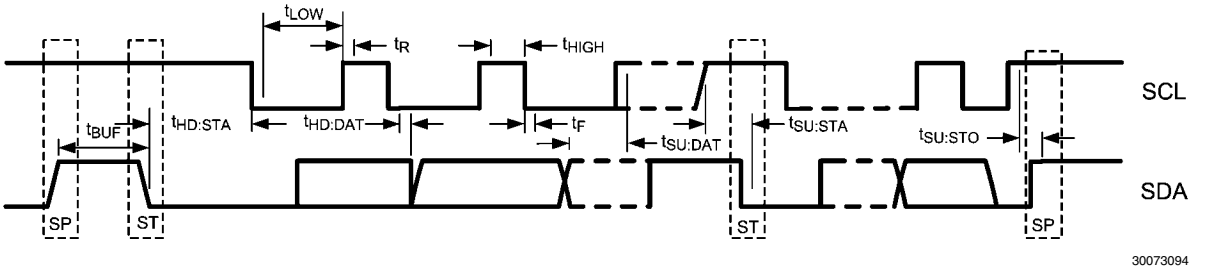


FIGURE 4. SMBus Timing Parameters

Functional Description

The DS64BR401 is a quad transceiver optimized for backplane trace or cable interconnect up to 6.4 Gbps. The DS64BR401 operates in two modes: Pin Control Mode (ENSMB = 0) and SMBus Mode (ENSMB = 1).

Pin Control Mode:

When in pin mode (ENSMB = 0) , the transceiver is configurable with external pins. Equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically increased per the De-Emphasis table below for improved performance over lossy media. Rate optimization is also pin controllable, with pin selections for 3 Gbps, 6 Gbps, and auto detect. The receiver electrical idle detect threshold is also programmable via an optional external resistor on the SD_TH pin.

SMBUS Mode

When in SMBus mode the VOD amplitude level, equalization and de-emphasis are all programmable on a individual lane basis, instead of grouped by sides as in the pin mode case. Upon assertion of ENSMB pins EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins remain active unless their respective registers are written to, in which case they are ignored until ENSMB is driven low. On power-up and when ENSMB is driven low all registers are reset to their default state. If $\overline{\text{PWDN}}$ = 1 is asserted while ENSMB = 1, the registers retain their current state.

TABLE 1. Equalization Input Select Pins for A and B ports (3–Level Input)

EQ0	EQ1	Equalization Level	Recommended Media Length
F	F	Off	Bypass
1	1	5.8 dB at 3 GHz	8 inch FR4 (4-mil trace) or 0.7 meters (30 AWG)
0	0	9 dB at 3 GHz	12 inch FR4 (4-mil trace) or 1 meters (30 AWG)
0	F	11.7 dB at 3 GHz	20 inch FR4 (4-mil trace) or 5 meters (30 AWG)
0	1	14.6 dB at 3 GHz	25 inch FR4 (4-mil trace) or 6 meters (30 AWG)
1	F	18.4 dB at 3 GHz	35 inch FR4 (4-mil trace) or 9 meters (30 AWG)
1	0	20 dB at 3 GHz	40 inch FR4 (4-mil trace) or 10 meters (30 AWG)
F	0	21.2 dB at 3 GHz	10 meters (30 AWG)
F	1	28.4 dB at 3 GHz	12 meters (30 AWG)
Note: F = Float (don't drive pin), 1 = High and 0 = Low.			

TABLE 2. De-Emphasis Input Select Pins for A and B ports (3–Level Input)

RATE	DEM1	DEM0	De-Emphasis Level (typ)	DE Pulse Width (typ)	VOD (typ)	Recommended Media Length
0/F	0	0	0 dB	0 ps	VOD: 600 to 1200 mVp-p	10 inch FR4 trace or 1 meter (28 AWG)
0/F	0	1	-3.5 dB	330 ps	VOD = 1000 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
			-2 dB	330 ps	VOD = 1200 mVp-p	15 inch FR4 trace or 2 meters (28 AWG)
0/F	1	0	-6 dB	330 ps	VOD = 1000 mVp-p	25 inch FR4 trace or 3 meters (28 AWG)
			-3 dB	330 ps	VOD = 1200 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
0/F	1	1	-9 dB	300 ps enhanced	VOD = 1000 mVp-p	5 meters (28 AWG)
			-11 dB	300 ps enhanced	VOD = 1200 mVp-p	7 meters (28 AWG)
0/F	0	F	-6 dB	300 ps enhanced	VOD = 1000 mVp-p	5 meters (26 AWG)
			-8 dB	300 ps enhanced	VOD = 1200 mVp-p	7 meters (26 AWG)
0/F	1	F	-12 dB	300 ps enhanced	VOD = 1000 mVp-p	8 meters (24 AWG)
			-13 dB	300 ps enhanced	VOD = 1200 mVp-p	9 meters (24 AWG)
0/F	F	0	-9 dB	250 ps enhanced	VOD = 1000 + 200 mVp-p	8 meters (26 AWG)
			-10 dB	250 ps enhanced	VOD = 1200 + 200 mVp-p	9 meters (26 AWG)

RATE	DEM1	DEM0	De-Emphasis Level (typ)	DE Pulse Width (typ)	VOD (typ)	Recommended Media Length
0/F	F	1	-12 dB	250 ps enhanced	VOD: (1000 to 1200) + 200 mVp-p	10 meters (24 AWG)
0/F	F	F	Reserved, don't use			
1/F	0	0	0 dB	0 ps	VOD: 600 to 1200 mVp-p	5 inch FR4 trace or 0.5 meter (28 AWG)
1/F	0	1	-3.5 dB	200 ps	VOD = 1000 mVp-p	10 inch FR4 trace or 1 meter (28 AWG)
			-2 dB	200 ps	VOD = 1200 mVp-p	10 inch FR4 trace or 1 meters (28 AWG)
1/F	1	0	-6 dB	200 ps	VOD = 1000 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
			-3 dB	200 ps	VOD = 1200 mVp-p	15 inch FR4 trace or 1 meters (28 AWG)
1/F	1	1	-9 dB	180 ps enhanced	VOD = 1000 mVp-p	3 meters (28 AWG)
			-11 dB	180 ps enhanced	VOD = 1200 mVp-p	4 meters (28 AWG)
1/F	0	F	-6 dB	180 ps enhanced	VOD = 1000 mVp-p	3 meters (26 AWG)
			-8 dB	180 ps enhanced	VOD = 1200 mVp-p	4 meters (26 AWG)
1/F	1	F	-12 dB	180 ps enhanced	VOD = 1000 mVp-p	5 meters (24 AWG)
			-13 dB	180 ps enhanced	VOD = 1200 mVp-p	6 meters (24 AWG)
1/F	F	0	-9 dB	160 ps enhanced	VOD = 1000 + 200 mVp-p	5 meters (26 AWG)
			-10 dB	160 ps enhanced	VOD = 1200 + 200 mVp-p	6 meters (26 AWG)
1/F	F	1	-12 dB	160 ps enhanced	VOD: (1000 to 1200) + 200 mVp-p	7 meters (24 AWG)
1/F	F	F	Reserved, don't use			

Note: F = Float (don't drive pin), 1 = High and 0 = Low. Enhanced DE pulse width provides de-empahsis on second bit. When RATE = F (auto rate detection active), the DE level and pulse width settings follow detected rate after exiting IDLE. RATE = 0 is 3 Gbps and RATE = 1 is 6 Gbps. De-emphasis should only be used with VOD = 1000 mVp-p or 1200 mVp-p. VOD less then 1000 mVp-p is not recommended with de-emphasis. Please refer to VOD1 and VOD0 pin description to set the output differential voltage level.

TABLE 3. Idle Control (3–Level Input)

TXIDLEA/B	Function
0	This state is for lossy media, dedicated Idle threshold detect circuit disabled, output follows input based on EQ settings. Idle state not guaranteed.
Float	Float enables automatic idle detection. Idle on the input is passed to the output. Internal 50KΩ resistors hold TXIDLEA/B pin at a mid level - don't connect this pin if the automatic idle detect function is desired. This is the default state. Output in Idle if differential input signal less than value set by SD_TH pin.
1	Manual override, output in electrical Idle. Differential inputs are ignored.

TABLE 4. Receiver Electrical Idle Detect Threshold Adjust

SD_TH resistor value (Ω)	Receiver Electrical Idle Detect Threshold (DIFF p-p)
Float (no resistor required)	130 mV (default condition)
0	225 mV
80k	20 mV
SD_TH resistor value can be set from 0 through 80k ohms to achieve desired idle detect threshold, see *Figure 5*	

Typical Performance Curves

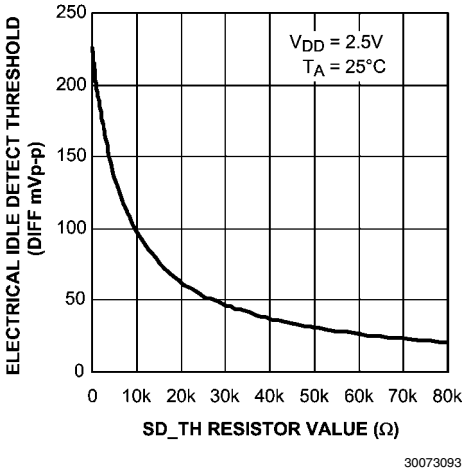


FIGURE 5. Typical Idle Threshold vs. SD_TH resistor value

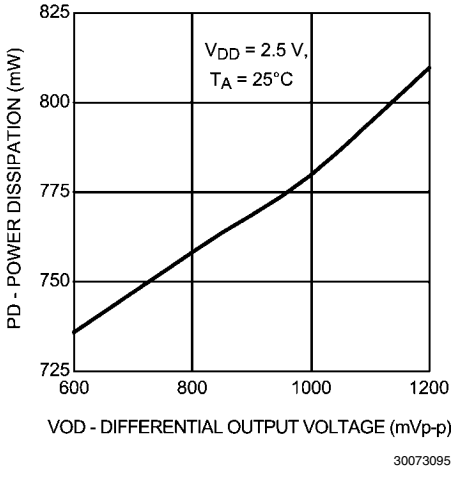


FIGURE 6. Typical Power Dissipation (PD) vs. Output Differential Voltage (VOD)

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB must be pulled high to enable SMBus mode and allow access to the configuration registers.

The DS64BR401 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBus slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is A0'h. Based on the SMBus 2.0 specification, the DS64BR401 has a 7-bit slave address of 1010000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 0000'b or A0'h. The device address byte can be set with the use of the AD[3:0] inputs. Below are some examples.

AD[3:0] = 0001'b, the device address byte is A2'h

AD[3:0] = 0010'b, the device address byte is A4'h

AD[3:0] = 0100'b, the device address byte is A8'h

AD[3:0] = 1000'b, the device address byte is B0'h

The SDC and SDA pins are 3.3V LVCMOS signaling and include high-Z internal pull up resistors. External low impedance pull up resistors maybe required depending upon SMBus loading and speed. Note, these pins are not 5V tolerant.

TRANSFER OF DATA VIA THE SMBUS

During normal operation the data on SDA must be stable during the time when SDC is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SDC is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SDC is High indicates a message STOP condition.

IDLE: If SDC and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBUS TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

RECOMMENDED SMBUS REGISTER SETTINGS

When SMBus mode is enabled (ENSMB = 1), the default register settings are not configured to an appropriate level. Below is the recommended settings to configure the EQ, VOD and DE to a medium level that supports interconnect length of 20 inches FR4 trace or 3 to 5 meters of cable length. Please refer to *Table 1*, *Table 2*, *Table 5* for additional information and recommended settings.

1. Reset the SMBus registers to default values:
   Write 01'h to address 0x00.
2. Set equalization to external pin level EQ[1:0] = 00 (~9 dB at 3 GHz) for all channels (CH0–CH7):
   Write 30'h to address 0x0F, 0x16, 0x1D, 0x24, 0x2C, 0x33, 0x3A, 0x41.
3. Set VOD = 1.0V for all channels (CH0–CH7):
   Write 0F'h to address 0x10, 0x17, 0x1E, 0x25, 0x2D, 0x34, 0x3B, 0x42.
4. Set de-emphasis to -6 dB enhance for all channels (CH0–CH7):
   Write 88'h to address 0x11, 0x18, 0x1F, 0x26, 0x2E, 0x35, 0x3C, 0x43.
5. Block the device from resetting to default values:
   Write 02'h to address 0x00.

IDLE AND RATE DETECTION TO EXTERNAL PINS

The functions of IDLE and RATE detection to external pins for monitoring can be supported in SMBus mode. The external GPIO pins of 19, 20, 46 and 47 will be changed and they will serve as outputs for IDLE and RATE detect signals.

The following external pins should be set to auto detection:

RATE = F (FLOAT) – auto RATE detect enabled

TXIDLEA/B = F (FLOAT) – auto IDLE detect enabled

There are 4 GPIO pins that can be configured as outputs with reg_4E[0].

To disable the external SMBus address pins, so pin 46 and 47 can be used as outputs:

Write 01'h to address 0x4E.

Care must be taken to ensure that only the desired status block is enabled and attached to the external pin as the status blocks can be OR’ed together internally. Register bits reg_47[5:4] and bits reg_4C[7:6] are used to enable each of the status block outputs to the external pins. The channel status blocks can be internally OR’ed together to monitor more than one channel at a time. This allows more information to be presented on the status outputs and later if desired, a diagnosis of the channel identity can be made with additional SMBus writes to register bits reg_47[5:4] and bits reg_4C[7:6].

Below are examples to configure the device and bring the internal IDLE and RATE status to pins 19, 20, 46, 47.

To monitor the IDLE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

Write 32'h to address 0x47.

The following IDLE status should be observable on the external pins:

pin 19 – CH0 with CH2,

pin 20 – CH1 with CH3,

pin 46 – CH4 with CH6,

pin 47 – CH5 with CH7.

Pin = HIGH (VDD) means IDLE is detected (no signal present).

Pin = LOW (GND) means ACTIVE (data signal present).

To monitor the RATE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

Write C0'h to address 0x4C.

The following RATE status should be observable on the external pins:

pin 19 – CH0 with CH2,

pin 20 – CH1 with CH3,

pin 46 – CH4 with CH6,

pin 47 – CH5 with CH7.

Pin = HIGH (VDD) means high data rate is detected (6 Gbps).

Pin = LOW (GND) means low rate is detected (3 Gbps).

TABLE 5. SMBus Register Map

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x00	Reset	7:2	Reserve	R/W	0x00	Set bits to 0.
		1	Block SMBus Reset			SMBus Reset Block 0: Allow SMBus reset from bit 0 1: Block SMBus reset from bit 0
		0	Reset			SMBus Reset 1: Reset registers to default value
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel [7]: CHA_3 [6]: CHA_2 [5]: CHA_1 [4]: CHA_0 [3]: CHB_3 [2]: CHB_2 [1]: CHB_1 [0]: CHB_0 00'h = all channels enabled FF'h = all channels disabled
0x02	PWDN Control	7:1	Reserve	R/W	0x00	Set bits to 0.
		0	Override $\overline{\text{PWDN}}$			0: Allow $\overline{\text{PWDN}}$ pin control 1: Block $\overline{\text{PWDN}}$ pin control
0x08	Pin Control Override	7:5	Reserve	R/W	0x00	Set bits to 0.
		4	Override IDLE			0: Allow IDLE pin control 1: Block IDLE pin control
		3	Reserve			Set bit to 0.
		2	Override RATE			0: Allow RATE pin control 1: Block RATE pin control
		1:0	Reserve			Set bits to 0.

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x0E	CH0 - CHB0 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x0F	CH0 - CHB0 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH0 IB0 EQ			IB0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x10	CH0 - CHB0 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH0 OB0 VOD			OB0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x11	CH0 - CHB0 DE Control	7:0	CH0 OB0 DEM	R/W	0x03	OB0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x12	CH0 - CHB0 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x15	CH1 - CHB1 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x16	CH1 - CHB1 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH1 IB1 EQ			IB1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x17	CH1 - CHB1 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH1 OB1 VOD			OB1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x18	CH1 - CHB1 DE Control	7:0	CH1 OB1 DEM	R/W	0x03	OB1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x19	CH1 - CHB1 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x1C	CH2 - CHB2 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x1D	CH2 - CHB2 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH2 IB2 EQ			IB2 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x1E	CH2 - CHB2 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH2 OB2 VOD			OB2 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x1F	CH2 - CHB2 DE Control	7:0	CH2 OB2 DEM	R/W	0x03	OB2 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x20	CH2 - CHB2 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x23	CH3 - CHB3 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x24	CH3 - CHB3 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH3 IB3 EQ			IB3 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x25	CH3 - CHB3 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH3 OB3 VOD			OB3 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x26	CH3 - CHB3 DE Control	7:0	CH3 OB3 DEM	R/W	0x03	OB3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x27	CH3 - CHB3 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x2B	CH4 - CHA0 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x2C	CH4 - CHA0 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH4 IA0 EQ			IA0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x2D	CH4 - CHA0 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH4 OA0 VOD			OA0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x2E	CH4 - CHA0 DE Control	7:0	CH4 OA0 DEM	R/W	0x03	OA0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x2F	CH4 - CHA0 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x32	CH5 - CHA1 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x33	CH5 - CHA1 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH5 IA1 EQ			IA1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x34	CH5 - CHA1 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH5 OA1 VOD			OA1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x35	CH5 - CHA1 DE Control	7:0	CH5 OA1 DEM	R/W	0x03	OA1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x36	CH5 - CHA1 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x39	CH6 - CHA2 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x3A	CH6 - CHA2 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH6 IA2 EQ			IA2 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x3B	CH6 - CHA2 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH6 OA2 VOD			OA2 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x3C	CH6 - CHA2 DE Control	7:0	CH6 OA2 DEM	R/W	0x03	OA2 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x3D	CH6 - CHA2 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x40	CH7 - CHA3 IDLE RATE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is muted (electrical idle) 1: Output is ON (SD is disabled)
		3:2	Reserve			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x41	CH7 - CHA3 EQ Control	7:6	Reserve	R/W	0x20	Set bits to 0.
		5:0	CH7 IA3 EQ			IA3 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h = 5 dB at 3 GHz 00 = 110000 = 30'h = 9 dB at 3 GHz 0F = 110010 = 32'h = 11.7 dB at 3 GHz 01 = 111001 = 39'h = 14.6 dB at 3 GHz 1F = 110101 = 35'h = 18.4 dB at 3 GHz 10 = 110111 = 37'h = 20 dB at 3 GHz F0 = 111011 = 3B'h = 21.2 dB at 3 GHz F1 = 111101 = 3D'h = 28.4 dB at 3 GHz
0x42	CH7 - CHA3 VOD Control	7	Reserve	R/W	0x03	Set bit to 0.
		6:0	CH7 OA3 VOD			OA3 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV
0x43	CH7 - CHA3 DE Control	7:0	CH7 OA3 DEM	R/W	0x03	OA3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00000011 = 03'h = –3.5 dB (Default) 10 = 00000101 = 05'h = –6.0 dB 0F = 10001000 = 88'h = –6.0 dB 01 = 10010000 = 90'h = –9.0 dB 1F = 10100000 = A0'h = –12.0 dB F0 = 10010000 = 90'h = –9.0 dB F1 = 10100000 = A0'h = –12.0 dB FF = 11000000 = C0'h = Reserve
0x44	CH7 - CHA3 IDLE Threshold	7:4	Reserve	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x47	EN Digital Test Point IDLE Detect	7:6	Reserve	R/W	0x02	Set bits to 0.
		5	CH2, CH3 CH6, CH7			0: Disabled IDLE Test Point for CH2, 3, 6, 7. 1: Enable IDLE Test Point for CH2, 3, 6, 7.
		4	CH0, CH1 CH4, CH5			0: Disabled IDLE Test Point for CH0, 1, 4, 5. 1: Enable IDLE Test Point for CH0, 1, 4, 5.
		3:0	Reserve			Set bits to 0010'b or h'2.
0x4C	EN Digital Test Point RATE Detect	7	CH2, CH3 CH6, CH7	R/W	0x00	0: Disabled RATE Test Point for CH2, 3, 6, 7. 1: Enable RATE Test Point for CH2, 3, 6, 7.
		6	CH0, CH1 CH4, CH5			0: Disabled RATE Test Point for CH0, 1, 4, 5. 1: Enable RATE Test Point for CH0, 1, 4, 5.
		5:0	Reserve			Set bits to 0.
0x4E	Digital Test	7:1	Reserve	R/W	0x00	Set bits to 0.
		0	Block AD[3:0] pins			1: Configure GPIO pin 46, 47, 53, 54 to be outputs.

Applications Information

GENERAL RECOMMENDATIONS

The DS64BR401 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

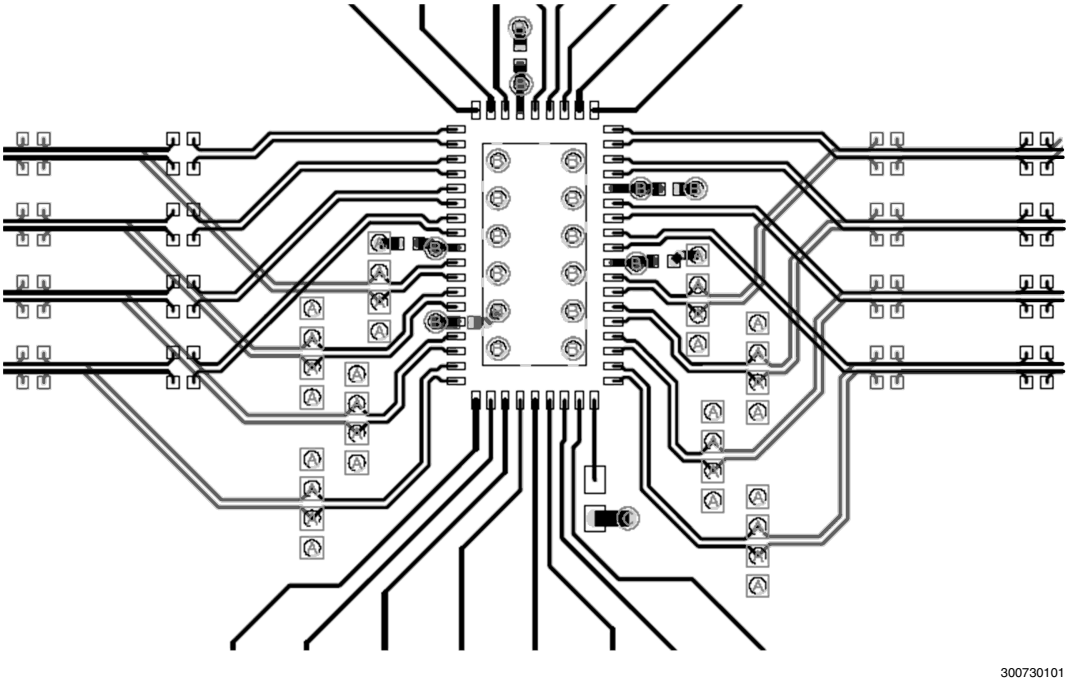
PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and LPDS outputs must have a controlled differential impedance of 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

The graphic shown below depicts a typical microstrip trace routing design of the top and bottom layers. This should be used as a reference to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each via hole. To further improve the signal quality, a ground via placed close to the signal via for a low inductance return current path is recommended. When the via structure is associated with stripline trace and a thick board, further optimization such as back drilling is often used to reduce the high frequency effects of via stubs on the signal path. To minimize cross-talk coupling, it is recommended to have >3X gap spacing between the differential pairs. For example, if the trace width is 5 mils with 5 mils spacing – 100Ω differential impedance (closely coupled). The gap spacing between the differential pairs should be >15 mils.

POWER SUPPLY BYPASSING

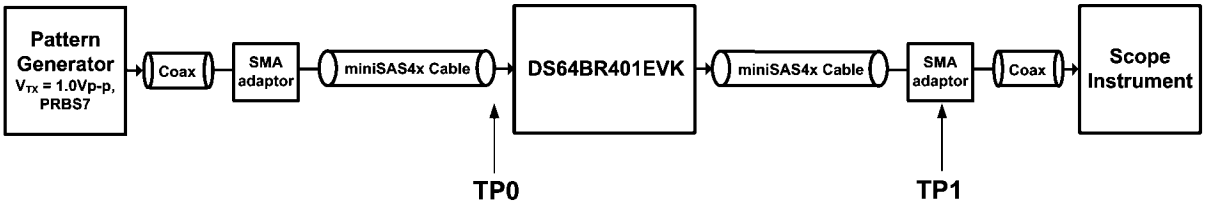
Two approaches are recommended to ensure that the DS64BR401 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS64BR401. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.



300730101

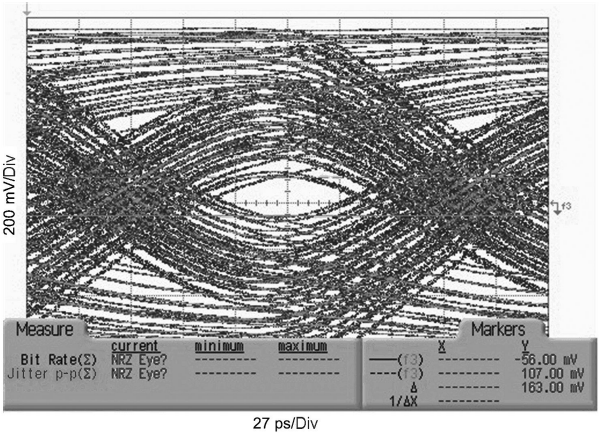
FIGURE 7. Typical PCB Trace Routing

Typical Performance Eye-Diagram Characteristics



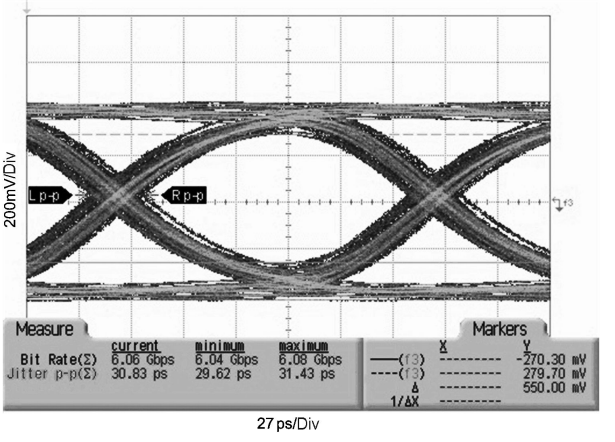
30073096

FIGURE 8. Test Setup Connection Diagram



30073097

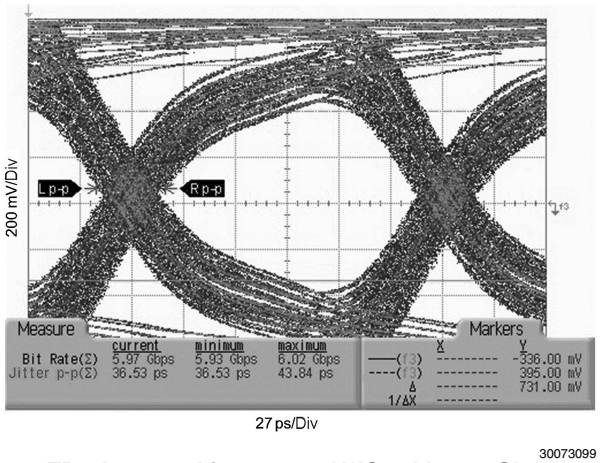
TP0: Input — After 5m 26–AWG Cable at 6 Gbps



30073098

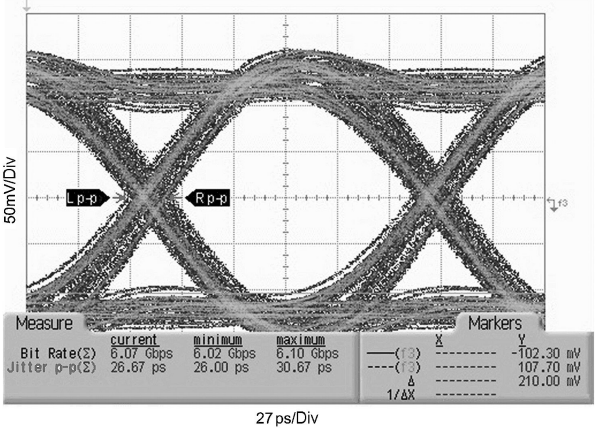
TP1: Output — After 1m 28–AWG Cable at 6 Gbps (EQ[1:0] = F0, DEM[1:0] = 01)

FIGURE 9.



30073099

TP0: Input — After 1m 28–AWG cable at 6 Gbps

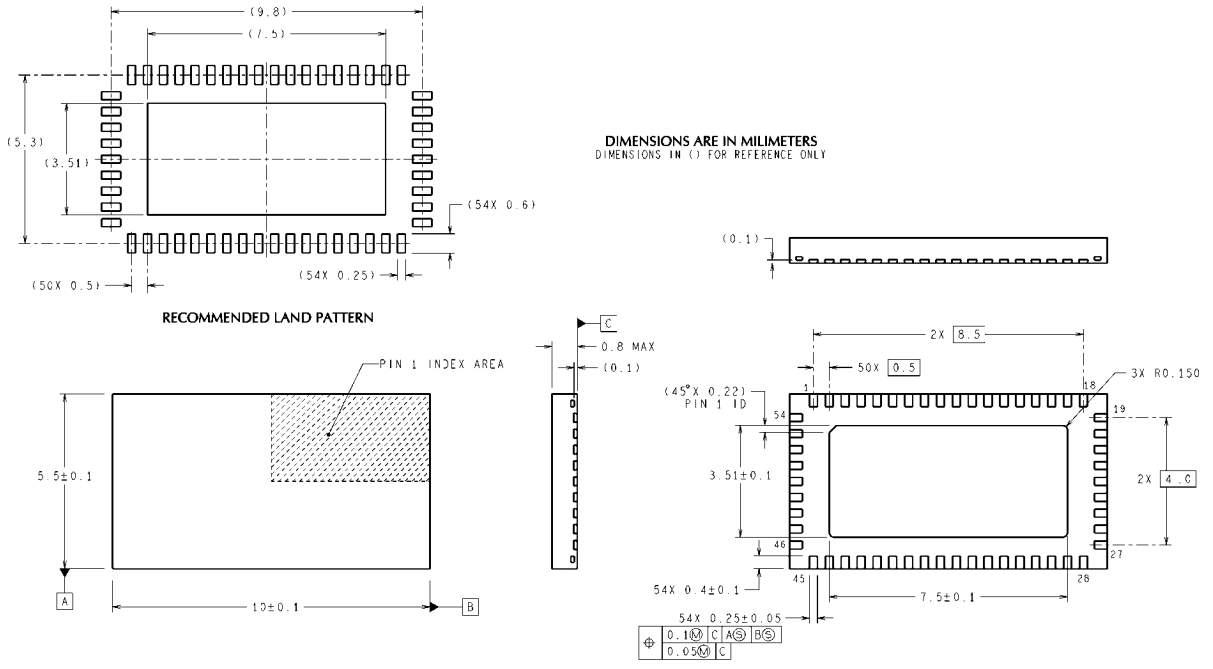


300730100

TP1: Output — After 5m 26–AWG Cable at 6 Gbps (EQ[1:0] = 11, DEM[1:0] = F0)

FIGURE 10.

Physical Dimensions inches (millimeters) unless otherwise noted



SQA54A (Rev B)

54-pin LLP Package (5.5 mm x 10 mm x 0.8 mm, 0.5 mm pitch)
Order Number: DS64BR401SQ — Tape & Reel Supplied As 2,000 Units,
DS64BR401SQE — Tape & Reel Supplied As 250 Units
Package Number: SQA54A

Notes

Notes

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Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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