DALLAS SEMICONDUCTOR

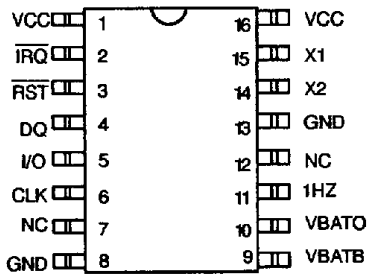
DS1608
EconoRAM Time Chip

FEATURES
- Unique 1-wire interface requires only one port pin for communication
- 3-wire I/O interface for high speed data communications
- Contains real-time clock/calendar in binary format
- 4096 bits of SRAM organized in 16 pages, 256 bits per page
- Interval timer can automatically accumulate time when power is applied
- Programmable cycle counter can accumulate the number of system power-on/off cycles
- Programmable alarms can be set to generate interrupts for interval timer, real-time clock, and/or cycle counter
- Data integrity assured with strict read/write protocols
- Space-saving 16-pin SOIC package
- Operating voltage range from 2.5 to 5.5 Volts

COMPARISON TO DS2404
The DS1608 and DS2404 share many features. The differences between the two parts are as follows:

- The clock oscillator is permanently enabled in the DS1608
- Permanent write protection and programmable expiration are not available with the DS1608
- The DS1608 does not incorporate the parasite powered circuitry
- Lasered serial number: family codes differ between the two and the 48 bit serial number is fixed with the DS1608

PIN ASSIGNMENT



16 PIN SOIC (300 Mil)

PIN DESCRIPTION

V_{CC}	-	2.5 to 5.5 Volts
$\overline{IRQ}$	-	Interrupt Output
$\overline{RST}$	-	3-Wire Reset Input
DQ	-	3-Wire Input/Output
I/O	-	1-Wire Input/Output
CLK	-	3-Wire Clock Input
NC	-	No Connection
GND	-	Ground
V_{BATB}	-	Battery Backup Input
V_{BATO}	-	Battery Operate Input
1 Hz	-	1 Hz Output
X_1, X_2	-	Crystal Connections

ORDERING INFORMATION

DS1608	16-pin DIP; -20°C to +70°C
DS1608S	16-pin SOIC; -20°C to +70°C

DESCRIPTION
TheDS1608EconoRAMTimeChipoffersasimplesolution for storing and retrieving vital data and time information with minimal hardware. The DS1608 contains a lasered ROM, real-time clock/calendar, interval timer, cycle counter, programmable interrupts and 4096 bits of SRAM. Two separate ports are provided for communication, 1-wire and 3-wire. Using the 1-wire port, only one pin is required for communication. The 3-wire port

provides high speed communication using the traditional Dallas Semiconductor 3-wire interface. With either interface, a strict protocol for accessing the DS1608 insures data integrity. Utilizing backup energy sources, the data is nonvolatile and allows for stand-alone operation.

The DS1608 features can be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, and event scheduler.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 16	V_{CC}	**Power input pins** for V_{CC} operate mode. 2.5 to 5.5 volts operation. Either pin can be used for V_{CC}. Only one is required for normal operation. (See V_{BATO} pin description and "Power Control" section).
2	$\overline{IRQ}$	**Interrupt output pin:** Open drain.
3	$\overline{RST}$	**Reset input pin** for 3-wire operation.
4	DQ	**Data input/output pin** for 3-wire operation.
5	I/O	**Data input/output** for 1-wire operation: Open drain.
6	CLK	**Clock input pin** for 3-wire operation.
7, 12	NC	**No connection pins.**
8, 13	GND	**Ground pin:** Either pin can be used for ground.
9	V_{BATB}	**Battery backup input pin:** Battery voltage can be 2.5 to 5.5 volts. (See V_{BATO} pin description and "Power Control" section.)
10	V_{BATO}	**Battery operate input pin** for 2.5 to 5.5 volt operation. The V_{CC} & V_{BATB} pins must be grounded when this pin is used to power the chip. (See "Power Control" section.)
11	1Hz	**1 Hz square wave output:** Open drain.
14, 15	X_1, X_2	**Crystal pins.** Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S (be sure to request 6 pF load capacitance). **NOTE:** X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area.

OVERVIEW

The DS1608 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to an external 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

Two communication ports are provided, a 1-wire port and a 3-wire port. A port selector determines which of the two ports is being used. The ROM data is accessible only through the 1-wire port. The scratchpad and memory are accessible via either port.

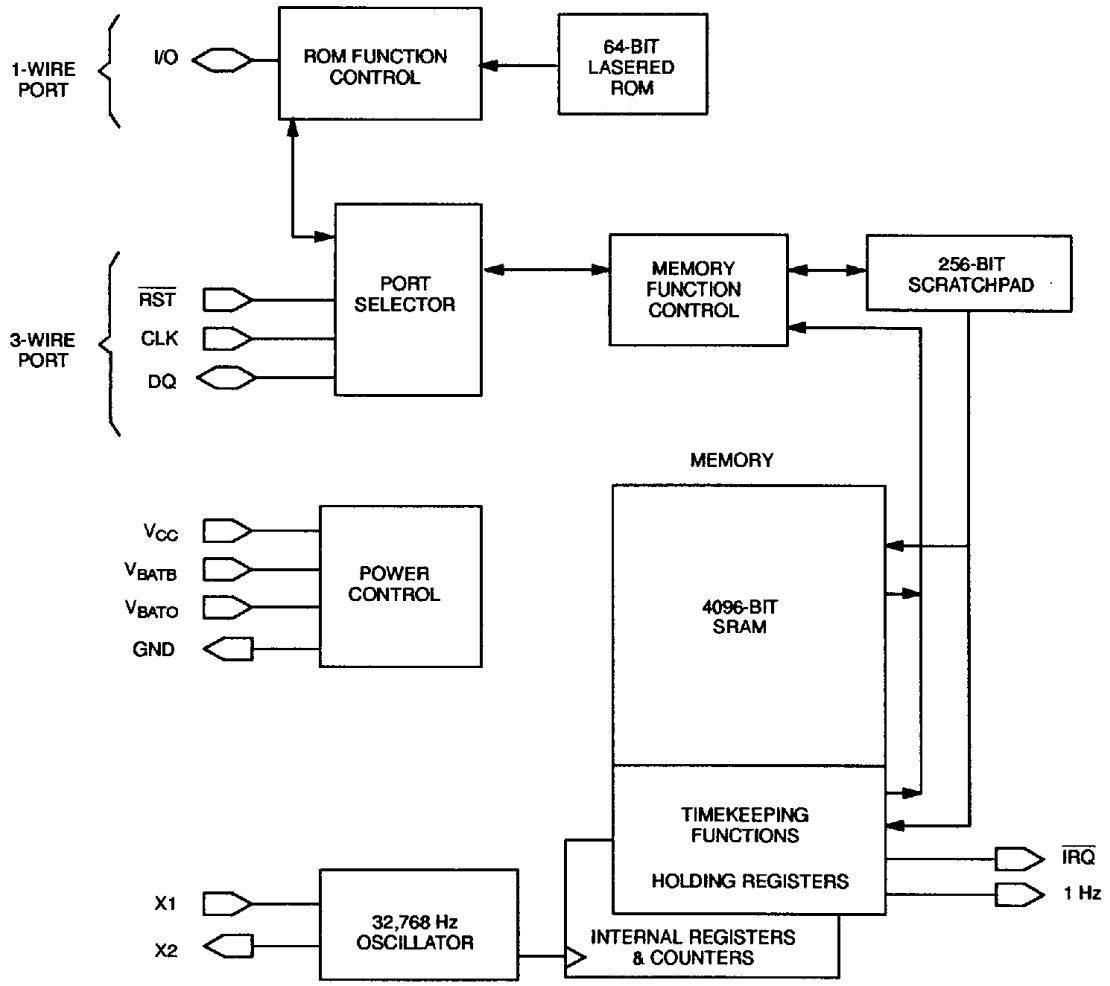
If the 3-wire port is used, the master provides one of four memory function commands: 1) read memory, 2) read scratchpad, 3) write scratchpad, or 4) copy scratchpad. The only way to write memory is to first write the scratchpad and then copy the scratchpad data to memory. (See Figure 6.)

If the 1-wire port is used, the memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the

master may then provide any one of the four memory function commands.

The "Power Control" section provides for two basic power configurations, battery operate mode and V_{CC} operate mode. The battery operate mode utilizes one supply connected to V_{BATO}. The V_{CC} operate mode may utilize two supplies; the primary supply connects to V_{CC} and a backup supply connects to V_{BATB}.

DS1608 BLOCK DIAGRAM Figure 1



COMMUNICATION PORTS

Two communication ports are provided, a 1-wire and a 3-wire port. The advantages of using the 1-wire port are as follows: 1) provides access to the 64-bit lasered ROM, 2) consists of a single communication signal (I/O), and 3) multiple devices may be connected to the 1-wire bus. The 1-wire bus has a maximum data rate of 16.6K bits/second and requires one 5KΩ external pullup.

The 3-wire port consists of three signals, $\overline{RST}$, CLK, and DQ. $\overline{RST}$ is an enable input, DQ is bidirectional serial data, and the CLK input is used to clock in or out the serial data. The advantages of using the 3-wire port are 1) high data transfer rate (2 MHz), 2) simple timing, and 3) no external pull-up required.

Port selection is accomplished on a first-come, first-serve basis. Whichever port comes out of reset first will

obtain control. For the 3-wire port, this is done by bringing $\overline{RST}$ high. For the 1-wire port, this is done on the first falling edge of I/O after the reset and presence pulses. (See "1-Wire Signalling" section.)

64-BIT LASERED ROM

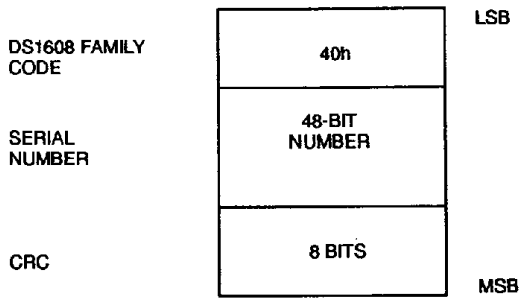
Each DS1608 contains a ROM code that is 64 bits long. The first eight bits are a 1-wire family code (DS1608 code is 40h). The next 48 bits are a serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$.

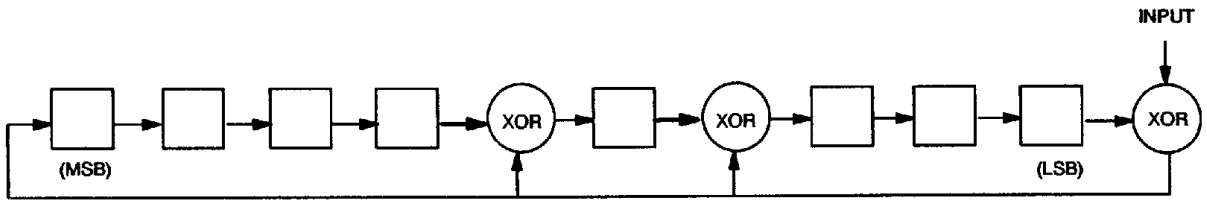
Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

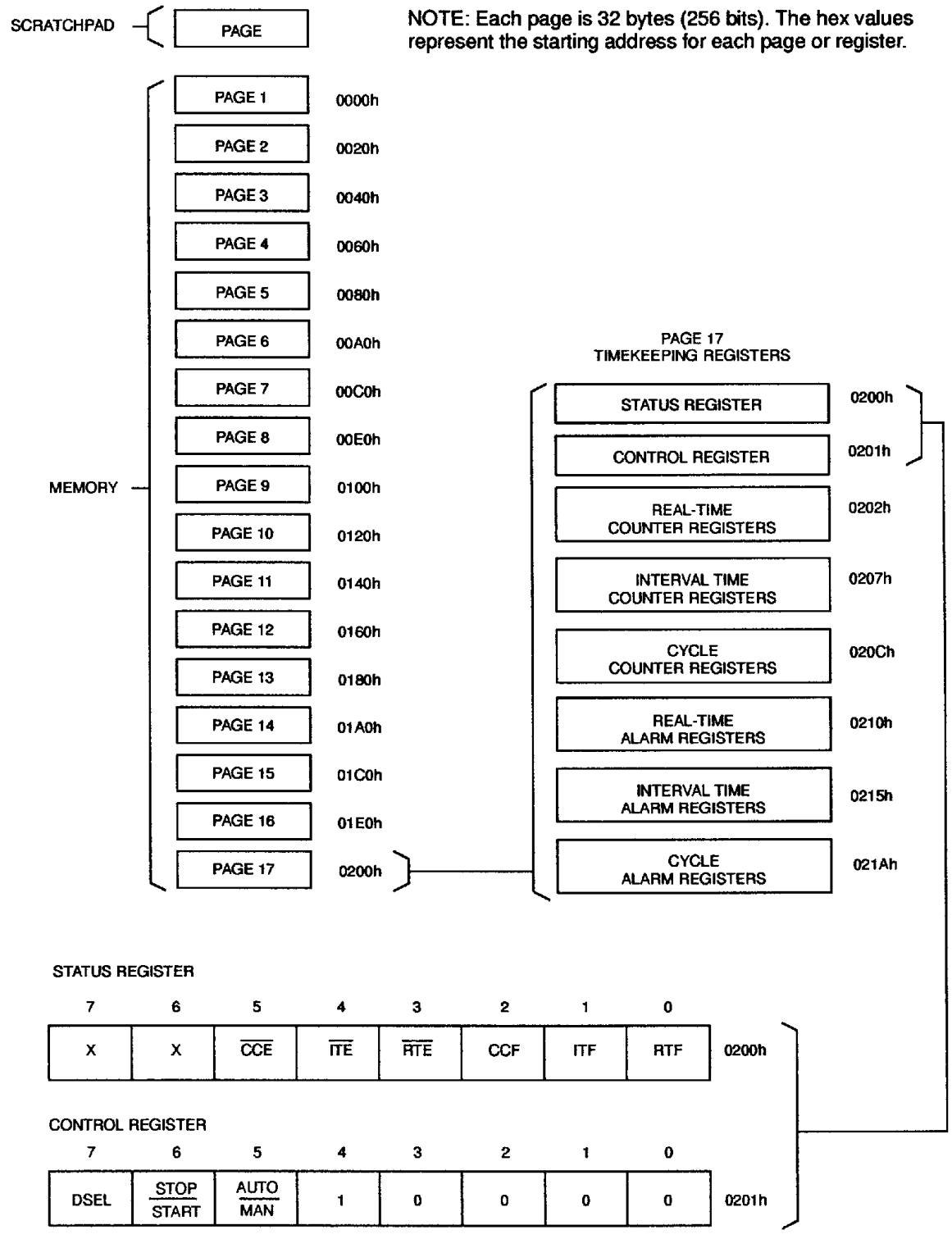
64-BIT LASERED ROM Figure 2



1-WIRE CRC CODE Figure 3



MEMORY MAP Figure 4



MEMORY

The memory map in Figure 4 shows a page (32 bytes) called the scratchpad and 17 pages called memory. Pages 1 through 16 each contain 32 bytes which make up the 4096-bit SRAM. Page 17 has only 30 bytes which contain the timekeeping registers.

The scratchpad is an additional page of memory that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

TIMEKEEPING

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator must be on for the real time clock, interval timer, cycle counter and 1 Hz output to function.

Oscillator

The DS1608 oscillator is always enabled. When the circuit is first powered on, it may take several seconds for the oscillator to start, especially at temperature extremes.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

Interval Timer

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

Cycle Counter

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

STATUS/CONTROL REGISTERS

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

Status Register

7	6	5	4	3	2	1	0	
X	X	$\overline{CCE}$	$\overline{ITE}$	$\overline{RTE}$	CCF	ITF	RTF	0200h
Don't care bits					Read Only			

0	RTF	Real-time clock alarm flag
1	ITF	Interval timer alarm flag
2	CCF	Cycle counter alarm flag

When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3	$\overline{RTE}$	Real-time interrupt enable
4	$\overline{ITE}$	Interval timer interrupt enable
5	$\overline{CCE}$	Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

Control Register

7	6	5	4	3	2	1	0	
DSEL	STOP/$\overline{START}$	AUTO/$\overline{MAN.}$	1	0	0	0	0	0201h

Bits 0, 1, 2, and 3 will always read zero and bit 4 will always read 1 regardless of whether it is written to an opposite state or not.

5 AUTO/$\overline{MAN}$ Automatic/$\overline{Manual}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/$\overline{START}$ bit.

6 STOP/$\overline{START}$ Stop/$\overline{Start}$ (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7 DSEL Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is 123 ± 2 ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 ± 0.5 ms.

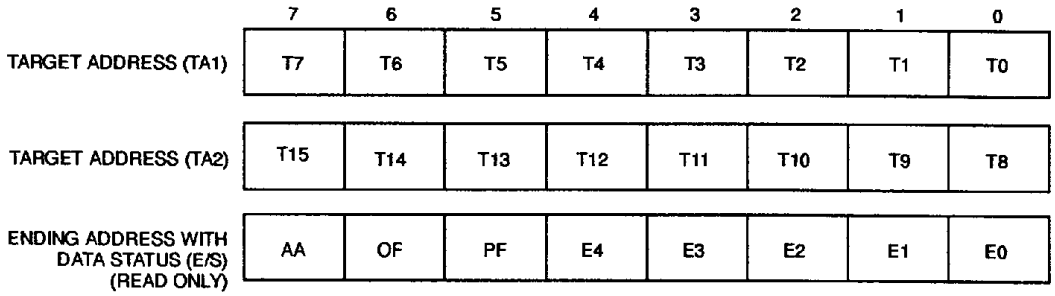
MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. Two examples follow the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

ADDRESS REGISTERS Figure 5



Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [55h]

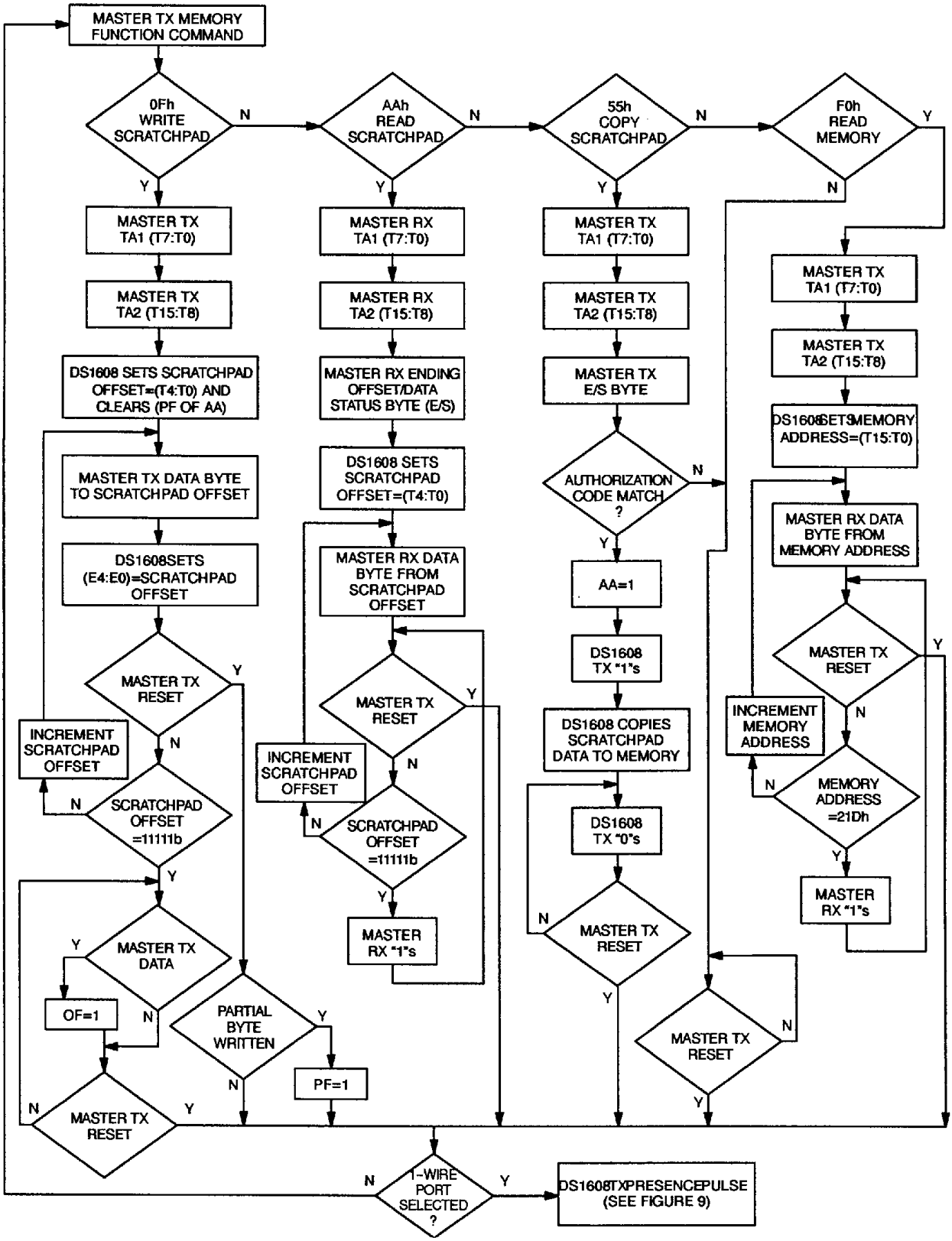
This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. At this point, the part will go into a T_X mode, transmitting a logic 1 to indicate the copy is in progress. A logic 0 will be transmitted after the data has been copied. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 2 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of page 17. After the end of page 17, logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION EXAMPLES

Example 1: Write one page of data to page 16
Read page 16 (3-wire port)

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master pulses $\overline{RST}$ low
TX	0Fh	Issue "write scratchpad" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
TX	<32 data bytes>	Write 1 page of data to scratchpad
TX	Reset	Master pulses $\overline{RST}$ low
TX	AAh	Issue "read scratchpad" command
RX	E0h	Read TA1, beginning offset=0
RX	01h	Read TA2, address=01E0h
RX	1Fh	Read E/S, ending offset=31d, flags=0
RX	<32 data bytes>	Read scratchpad data and verify
TX	Reset	Master pulse $\overline{RST}$ low
TX	55h	Issue "copy scratchpad" command
TX	E0h	TA1 } AUTHORIZATION CODE
TX	01h	TA2 } AUTHORIZATION CODE
TX	1Fh	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until DQ=0 (~30 µs typical)
TX	Reset	Master pulse $\overline{RST}$ low
TX	F0h	Issue "read memory" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
RX	<32 data bytes>	Read memory page 16 and verify
TX	Reset	Master pulse $\overline{RST}$ low, done

Example 2: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory (1-wire port).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until 0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<542 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1-WIRE BUS SYSTEM

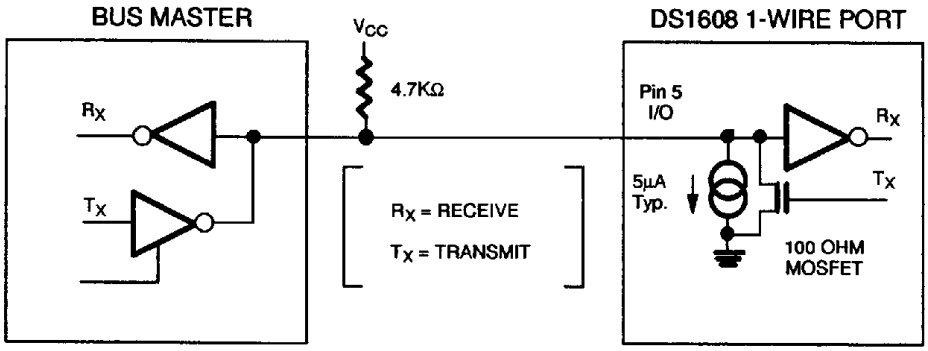
The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS1608 behaves as a slave. The exception is when the DS1608 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3-state outputs. The 1-wire port of the DS1608 (I/O pin 5) is open drain with an internal circuit equivalent to that shown in Figure 7. A multidrop bus consists of a 1-wire bus with multiple slaves attached. The 1-wire bus requires a pull-up resistor of approximately 5KΩ.

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

HARDWARE CONFIGURATION Figure 7



TRANSACTION SEQUENCE

The protocol for accessing the DS1608 via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1608 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 8):

Read ROM [33h]

This command allows the bus master to read the DS1608's 8-bit family code, 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single 1-wire device is on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific 1-wire device on a multidrop bus. If the DS1608 ROM

sequence is issued it will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the search ROM command on the 1-wire bus.

3. The bus master reads a bit from the 1-wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 0 onto the 1-wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3-step routine have the following interpretations:

   00 - There are still devices attached which have conflicting bits in this position.

   01 - All devices still coupled have a 0 bit in this bit position.

   10 - All devices still coupled have a 1 bit in this bit position.

   11 - There are no devices attached to the 1-wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.

5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.

8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two read time slots and receives two zeros.

16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

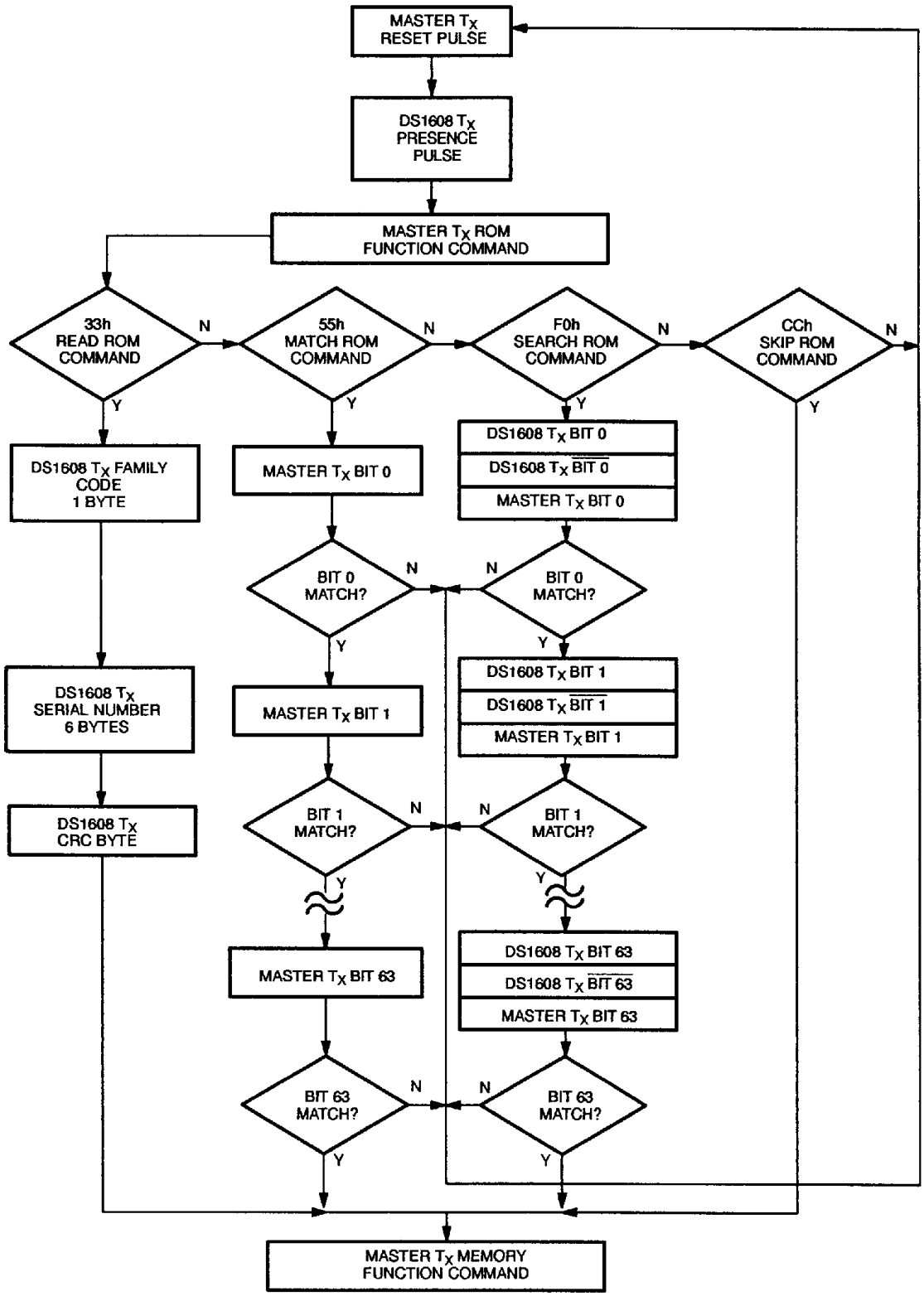
Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

ROM FUNCTIONS FLOW CHART (1-WIRE PORT ONLY) Figure 8



(SEE FIGURE 5)

I/O SIGNALLING

TheDS1608requiresstrictprotocolstoinsuredataintegrity. The protocol consists of seven types of signalling on one line: reset pulse, presence pulse, write 0, write 1, read 0, read 1, and interrupt pulse. All these signals, with the exception of the interrupt pulse, are initiated by the bus master.

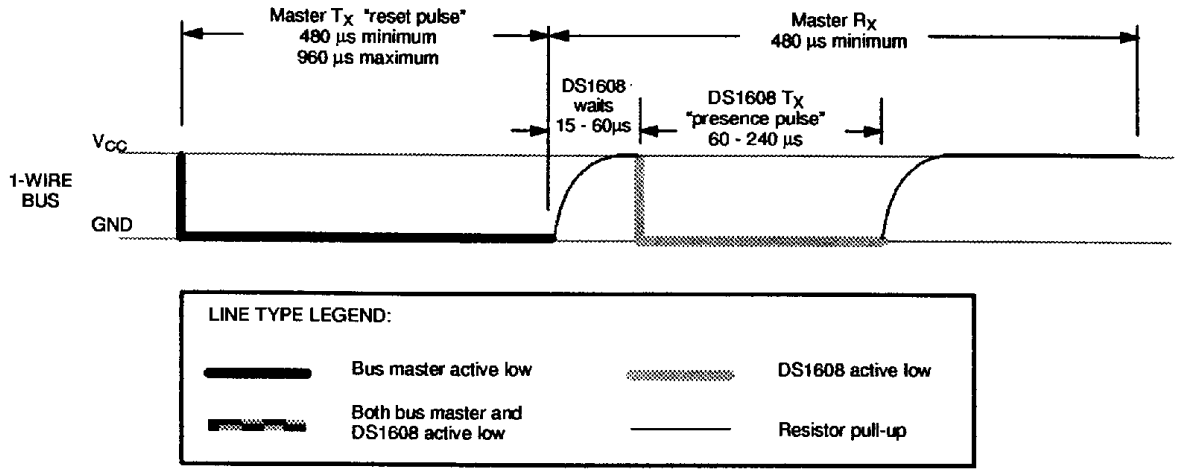
The initialization sequence required to begin any communication with the DS1608 is shown in Figure 9. A reset pulse followed by a presence pulse indicates the DS1608 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS1608 waits 15-60 µs and then transmits the presence pulse (a low signal for 60 - 240 µs). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the R_X mode for 480 µs. These conditions will be discussed in the "Interrupt" section.

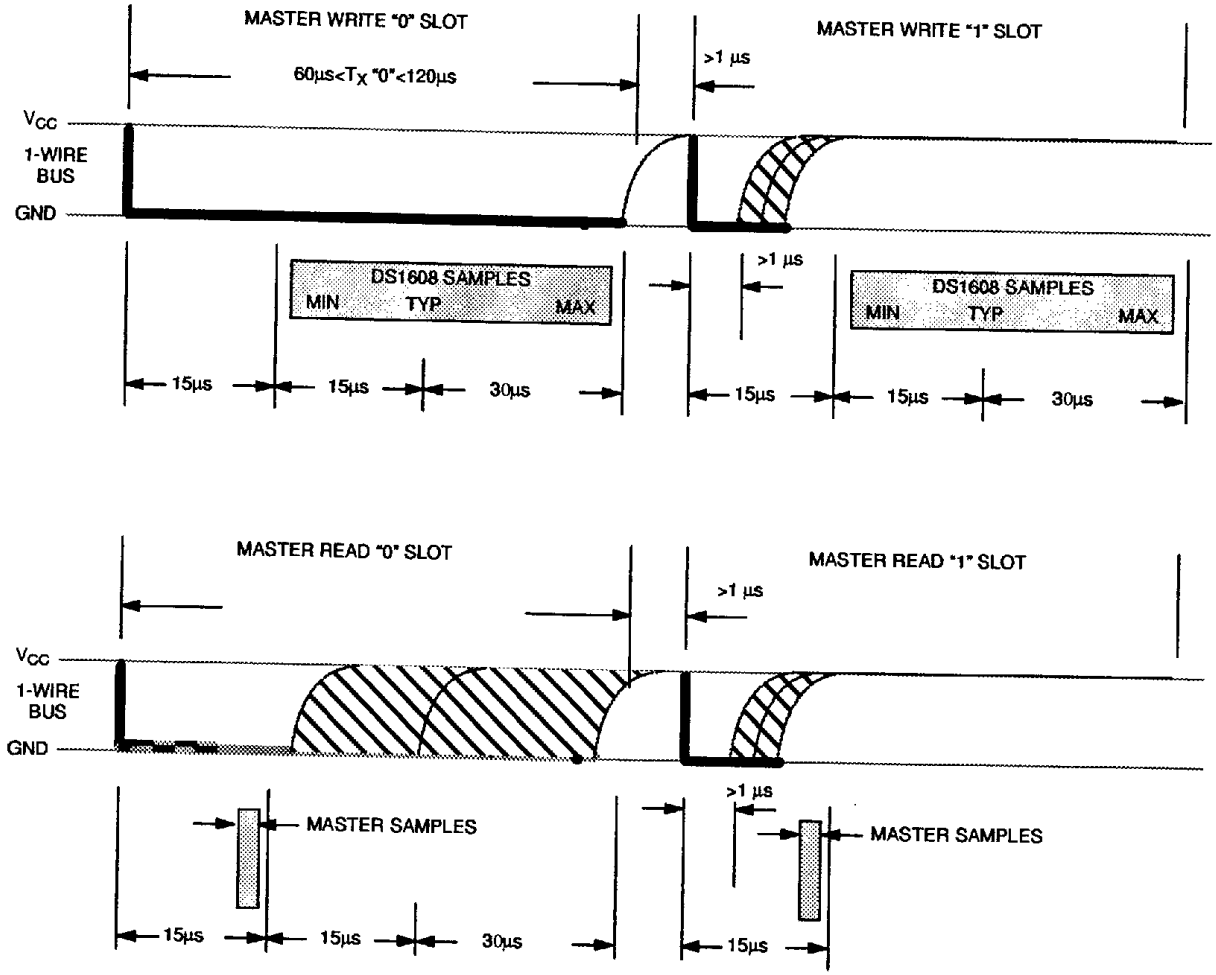
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 10. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS1608 to the master by triggering a delay circuit in the DS1608. During write time slots, the delay circuit determines when the DS1608 will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS1608 will hold the I/O line low.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9



READ/WRITE TIMING DIAGRAM Figure 10



DETAILED MASTER READ "1" TIMING Figure 11

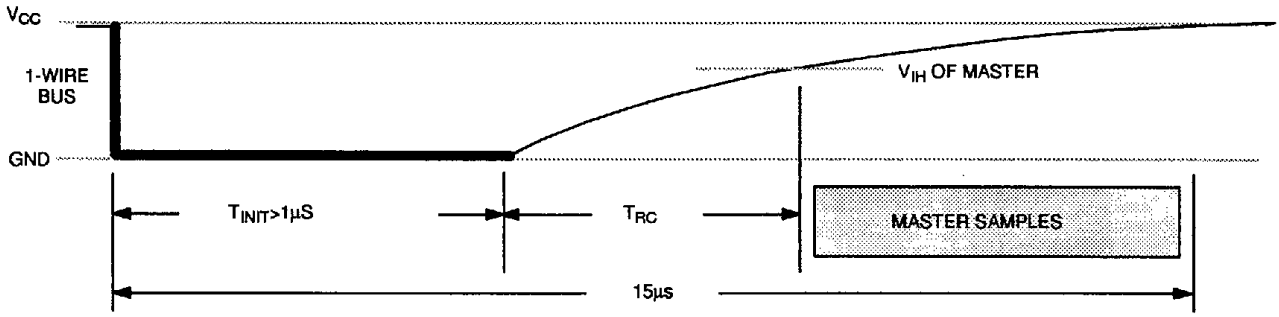
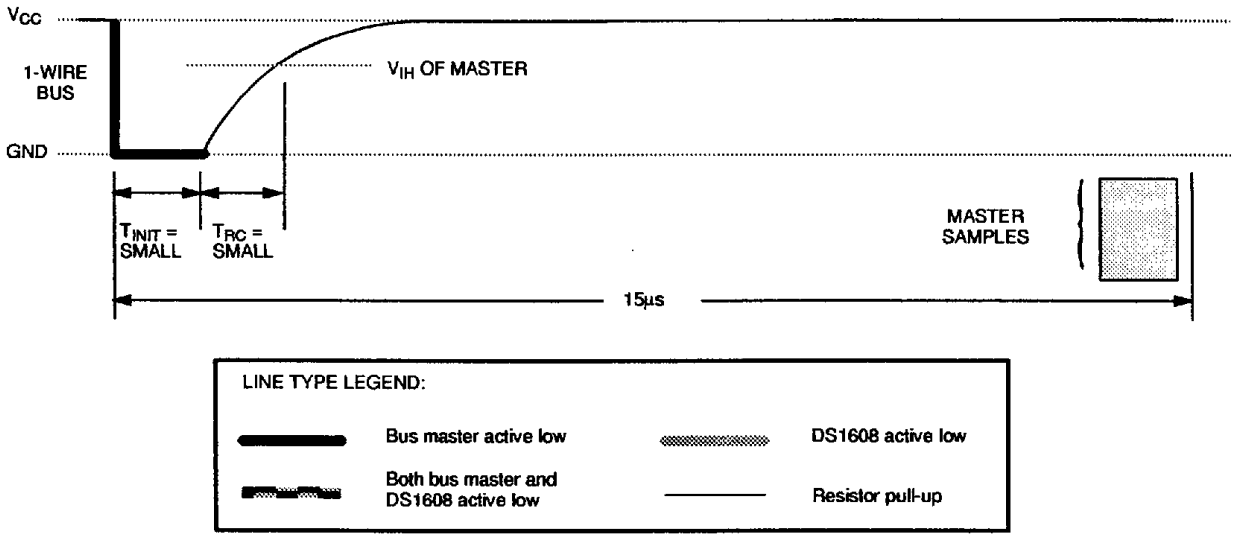


Figure 12 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs. Figure 13 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15µs period.

RECOMMENDED MASTER READ "1" TIMING Figure 12



Interrupts

An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the flags are read) or if the corresponding interrupt enable bit(s) is disabled. An interrupt condition may be detected on either the $\overline{IRQ}$ pin or the I/O pin. During the interrupt condition, the open-drain $\overline{IRQ}$ pin is driven low and held low until the interrupt condition ceases.

On the 1-wire port, the part responds, in general, by driving the I/O pin low for an extended period of time and then releasing. The interrupt condition may produce two types of interrupts on the 1-wire port. A type 1 interrupt (Figure 13) occurs only when I/O is high and there has been no communication (i.e., there has not been a falling edge on I/O since the last presence pulse). If this is the case, I/O is driven low for a period of 960 µs to 3840 µs as soon as an interrupt condition begins. A presence pulse will follow the interrupt pulse.

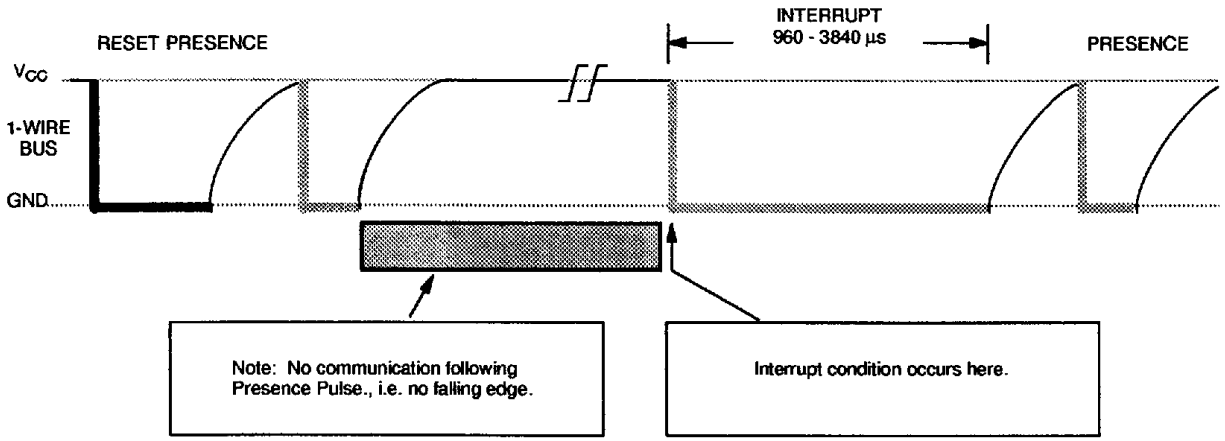
A type 2 interrupt (Figure 15) occurs if the host issues a reset pulse and an interrupt condition exists when the host releases the reset. If this is the case, I/O is driven low for an additional period of time, extending the reset pulse to a total period of 960 µs to 4800 µs. A presence pulse will follow the interrupt pulse. As long as the interrupt condition exists, the type 2 interrupt will occur with every reset pulse.

NOTE: If the interrupt condition begins during communication, a type 1 interrupt will not be issued. However, type 2 interrupts will occur during resets as expected.

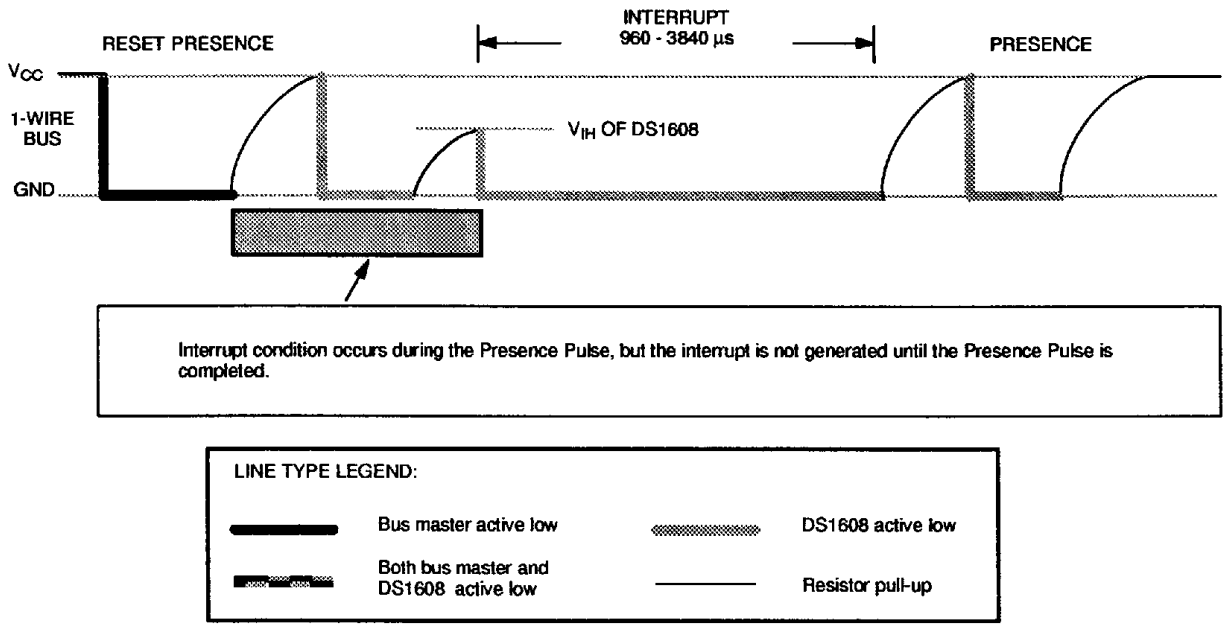
Special cases exist as follows:

Special Case A (Figure 14): If the interrupt condition begins during a presence pulse, the type 1 interrupt will be postponed until the presence pulse is over and I/O is a logic 1.

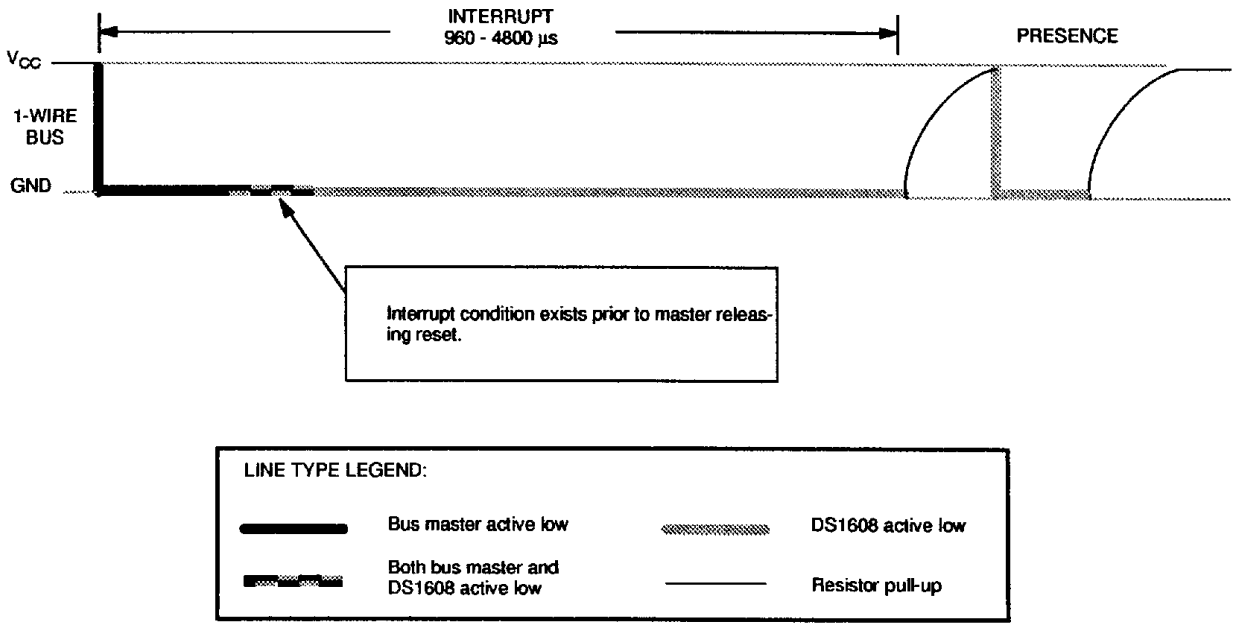
TYPE 1 INTERRUPT Figure 13



TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 14



TYPE 2 INTERRUPT Figure 15



3-WIRE I/O COMMUNICATIONS

The 3-wire bus is comprised of three signals. These are the $\overline{RST}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. Driving the $\overline{RST}$ input low terminates communication. (See Figures 22 and 23.)

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. When reading data from the DS1608, the DQ pin goes to a high impedance state while the clock is high. Taking $\overline{RST}$ low will terminate any communication and cause the DQ pin to go to a high impedance state.

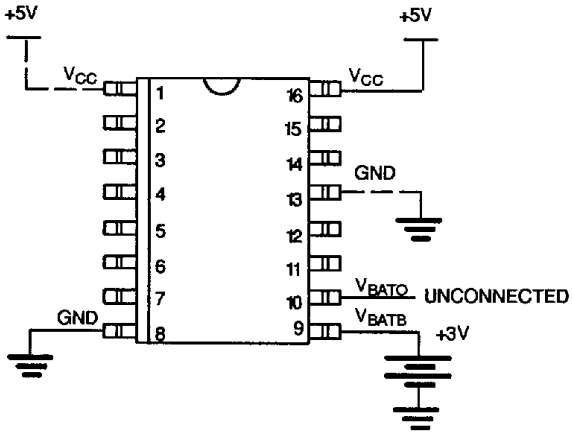
POWER CONTROL

There are two typical methods of supplying power to the DS1608, V_{CC} Operate mode and Battery Operate mode.

V_{CC} Operate Mode (Battery Backed)

Figure 16 shows the necessary connections for operating the DS1608 in V_{CC} Operate mode.

VCC OPERATE MODE Figure 16



V_{CC}	Pin 1 & 16	2.5 to 5.5 volts
V_{BATB}	Pin 9	2.5 to 5.5 volts*
V_{BATO}	Pin 10	must be unconnected

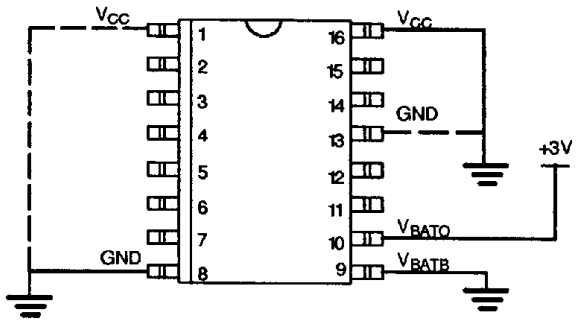
*While V_{BATB} may range from 2.5 to 5.5V, if the voltage on V_{BATB} ever exceeds the voltage on V_{CC}, the DS1608 will retain data, but will not allow access through the 1- or 3-wire port to the RAM.

The V_{BATB} pin is normally connected to any standard 3-volt lithium cell or other energy source. As V_{CC} falls below V_{BATB}, the power switching circuit allows V_{BATB} to provide energy for maintaining clock functionality and data retention. Communication can take place only with the ROM and not the RAM while V_{BATB} is greater than V_{CC}. During power-up, when V_{CC} rises above V_{BATB} (~200 mV), the power switching circuit connects V_{CC} and disconnects V_{BATB}. No communication can take place until V_{CC} has stayed (~200 mV) above V_{BATB} for 123 ± 2 ms.

Battery Operate Mode

Figure 17 shows the necessary connections for operating the DS1608 in Battery Operate mode.

BATTERY OPERATE MODE Figure 17



V_{CC}	Pin 1 & 16	Ground
V_{BATB}	Pin 9	Ground
V_{BATO}	Pin 10	2.5 to 5.5 volts

The V_{BATO} pin is normally connected to any standard 3-volt lithium cell or other energy source. Battery Operate mode provides low power consumption when used in conjunction with 1-wire interface.

Note: If the the 3-wire interface is used in Battery Operate mode, the voltage on DQ must never exceed the voltage on V_{BATO}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-20°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 9
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{RST}$ Logic 1		2.8		5.5	V	1
Supply	V_{CC}	2.8		5.5	V	1
Battery	V_{BATB}, V_{BATO}	2.8	3.0	5.5	V	1, 6

DC ELECTRICAL CHARACTERISTICS

(-20°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			1	mA	
$\overline{RST}$ Resistance to Ground	Z_{RST}		65		KΩ	
D/Q Resistance to Ground	Z_{DQ}		65		KΩ	
CLK Resistance to Ground	Z_{CLK}		65		KΩ	
Active Current	I_{CC1}			2	mA	5
Standby Current	I_{CC2}			500	µA	
I/O Operate Current	I_{BATO}			500	nC	10
Batt Current (OSC On)	I_{BAT1}			350	nA	7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	
I/O (1-Wire)	$C_{IN/OUT}$			80	pF	8

AC ELECTRICAL CHARACTERISTICS: 3-WIRE INTERFACE (-20°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	2,3,4
CLK Low Time	t_{CL}	250			ns	2
CLK High Time	t_{CH}	250			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise & Fall	t_R,t_F			500	ns	2
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	2
RST to I/O High Z	t_{CDZ}			50	ns	2

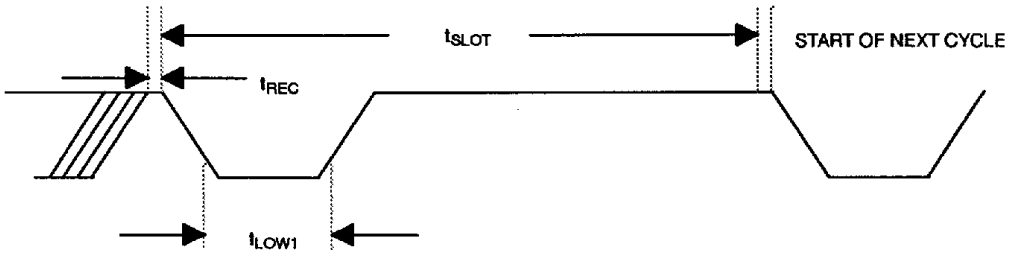
AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE (-20°C to 70°C; V_{CC}=2.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Interrupt	t_{INT}	960		4800	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

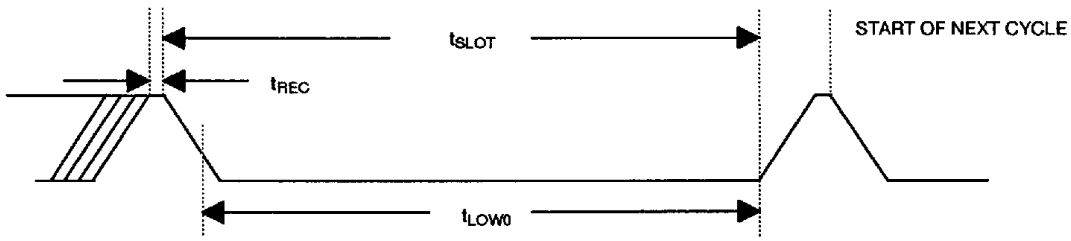
NOTES:

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. When battery is applied to V_{BATO} input, V_{CC} and V_{BATB} must be 0V.
7. V_{BATB}, or V_{BATO} = 3.0V; all inputs inactive state.
8. Capacitance on the I/O pin could be 80 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
9. For auto-mode operation of the interval timer, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.
10. Read or write scratchpad (all 32 bytes) at 3.0V.

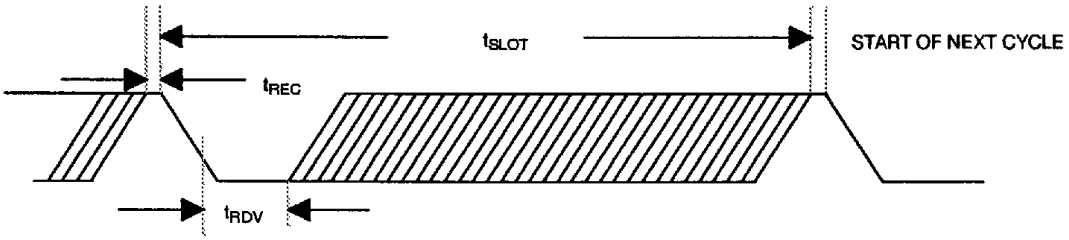
1-WIRE WRITE ONE TIME SLOT Figure 18



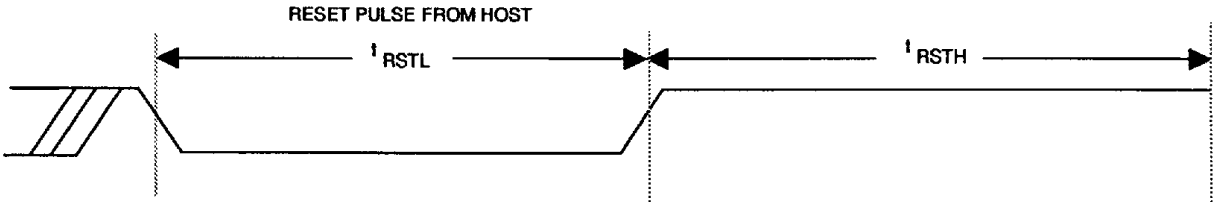
1-WIRE WRITE ZERO TIME SLOT Figure 19



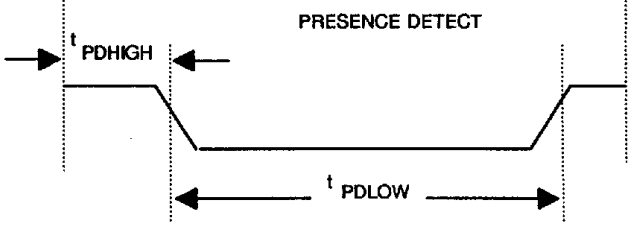
1-WIRE READ ZERO TIME SLOTS Figure 20



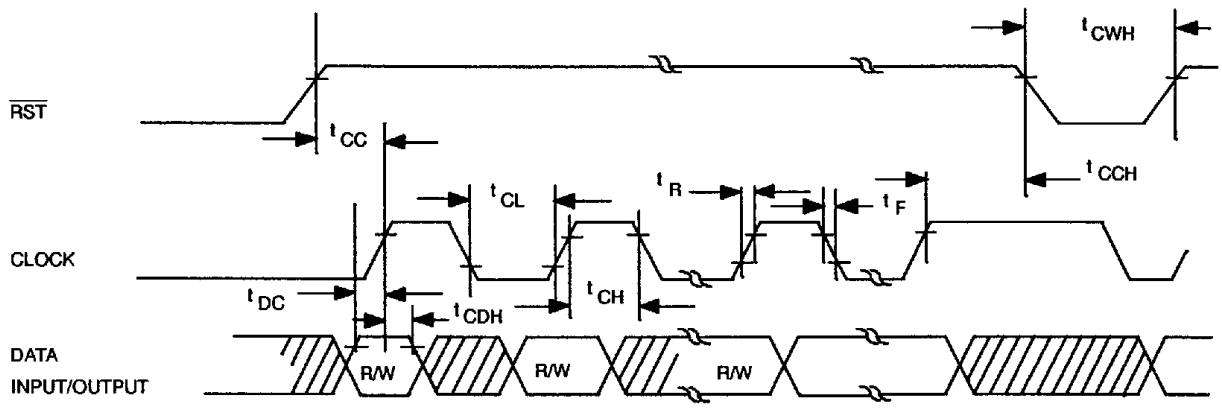
1-WIRE PRESENCE DETECT Figure 21



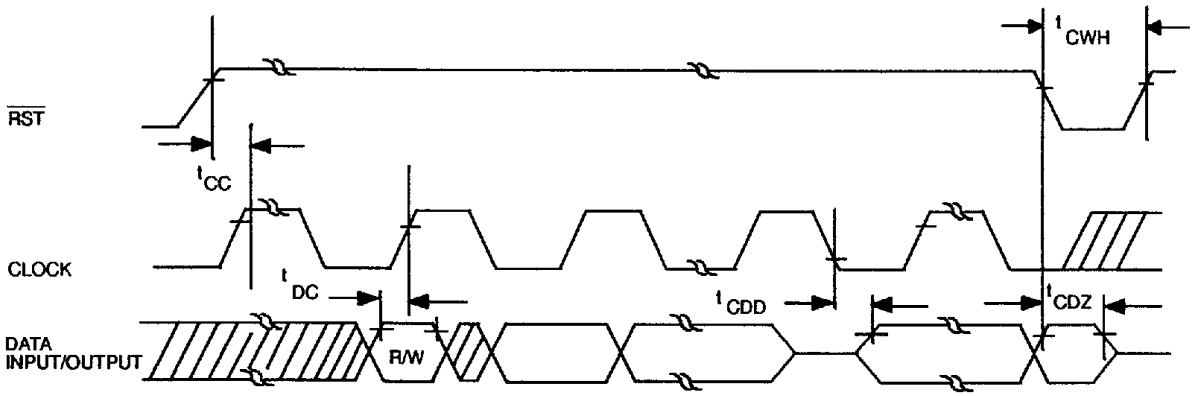
1-WIRE RESET PULSE



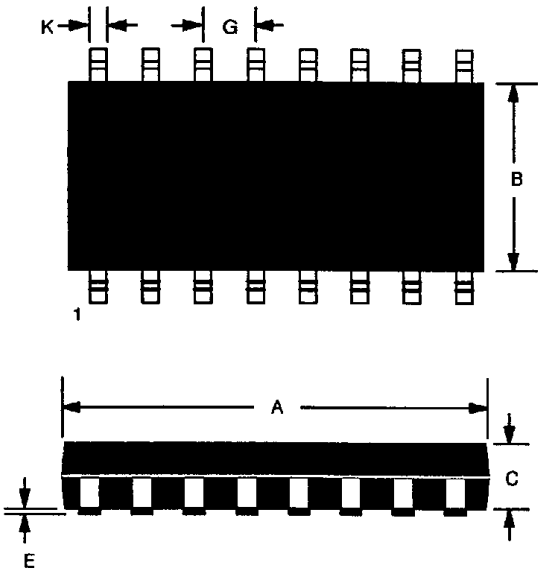
3-WIRE WRITE DATA TIMING DIAGRAM Figure 22

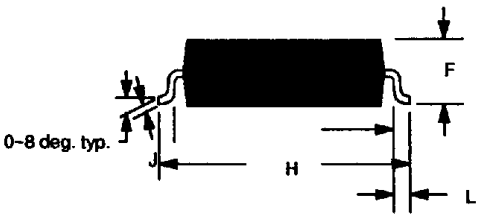


3-WIRE READ DATA TIMING DIAGRAM Figure 23



DS1608 ECONORAM TIME CHIP 16-PIN SOIC





PKG	16-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.402	0.412
B IN. MM	0.290	0.300
C IN. MM	0.089	0.095
E IN. MM	0.004	0.012
F IN. MM	0.094	0.105
G IN. MM	0.050 BSC	
H IN. MM	0.398	0.416
J IN. MM	0.009	0.013
K IN. MM	0.013	0.019
L IN. MM	0.016	0.040