



November 15, 2007

DS10CP152

1.5 Gbps 2X2 LVDS Crosspoint Switch

General Description

The DS10CP152 is a 1.5 Gbps 2x2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.

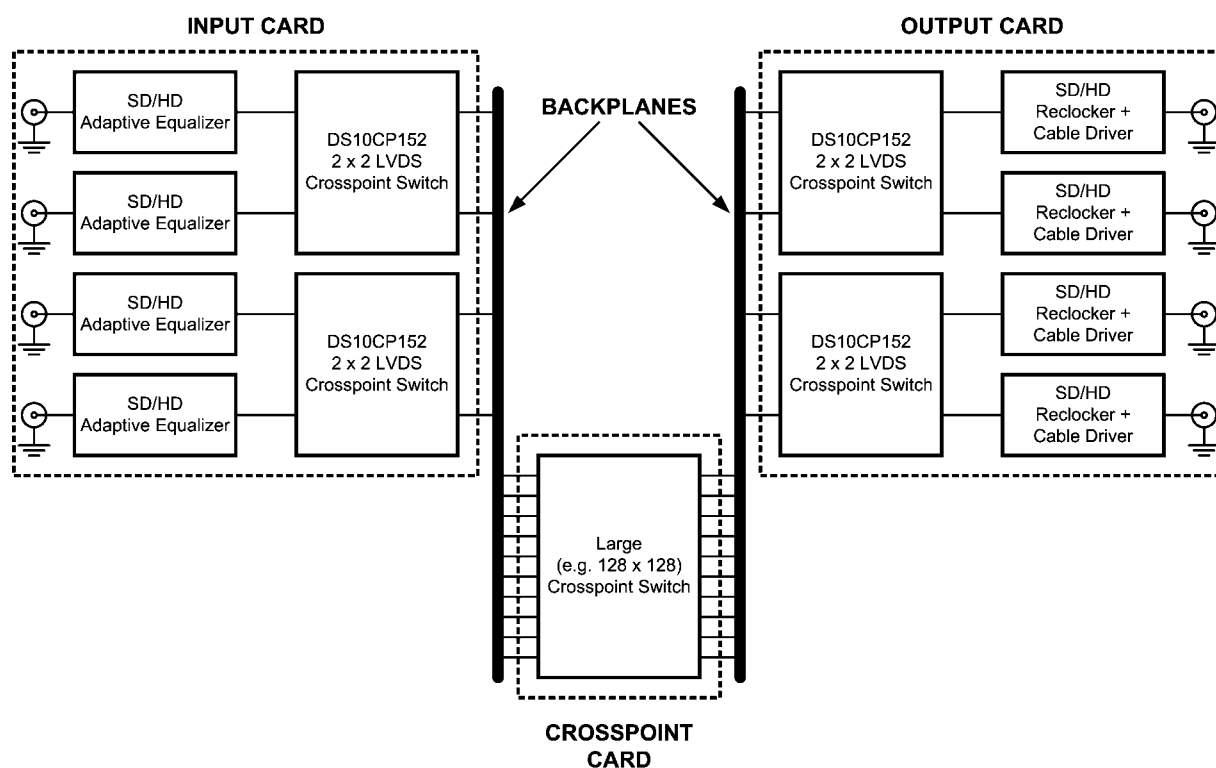
Features

- DC - 1.5 Gbps low jitter, low skew, low power operation
- Pin configurable, fully differential, non-blocking architecture
- Wide Input Common Mode Voltage Range allows DC-coupled interface to LVDS, CML and LVPECL drivers
- On-chip 100Ω input and output termination minimizes insertion and return losses, reduces component count and minimizes board space
- 7 kV ESD on LVDS I/O pins protects adjoining components
- Small SOIC-16 space saving package

Applications

- High-speed channel select applications
- Clock and data buffering and muxing
- SD/HD SDI Routers

Typical Application

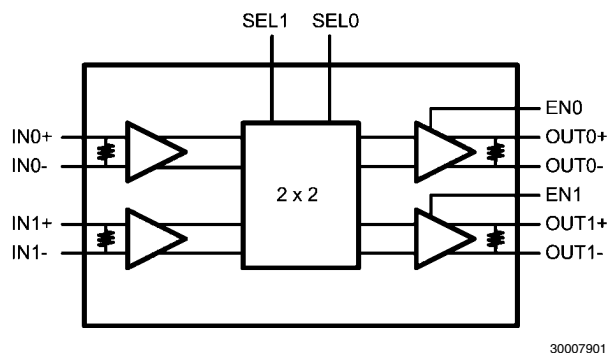


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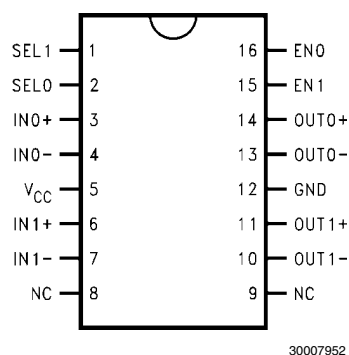
Ordering Code

| NSID | Function |
|--------------|-----------------------|
| DS10CP152TMA | 2x2 Crosspoint Switch |

Block Diagram



Connection Diagram



DS10CP152 Pin Diagram

Pin Descriptions

| Pin Name | Pin Number | I/O, Type | Pin Description |
|--------------------------------|-------------------|-----------|--|
| IN0+, IN0- , IN1+, IN1- | 3, 4, 6, 7 | I, LVDS | Inverting and non-inverting high speed LVDS input pins. |
| OUT0+, OUT0- , OUT1+, OUT1- | 14, 13, 11, 10 | O, LVDS | Inverting and non-inverting high speed LVDS output pins. |
| SEL0, SEL1 | 1, 2 | I, LVCMOS | Switch configuration pins. |
| EN0, EN1 | 16, 15 | I, LVCMOS | Output enable pins. |
| NC | 8, 9 | NC | "NO CONNECT" pins. |
| VDD | 5 | Power | Power supply pin. |
| GND | 12 | Power | Ground pin. |

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Package Thermal Resistance

 θ_{JA} +72.7°C/W θ_{JC} +41.2°C/W

ESD Susceptibility

HBM (Note 1) ≥ 7 kVMM (Note 2) ≥ 250 VCDM (Note 3) ≥ 1250 V**Note 1:** Human Body Model, applicable std. JESD22-A114C**Note 2:** Machine Model, applicable std. JESD22-A115-A**Note 3:** Field Induced Charge Device Model, applicable std. JESD22-C101-C

| | |
|--|------------------------------|
| Supply Voltage | -0.3V to +4V |
| LVC MOS Input Voltage | -0.3V to ($V_{CC} + 0.3$ V) |
| LVDS Input Voltage | -0.3V to +4V |
| LVDS Differential Input Voltage | 0V to 1V |
| LVDS Output Voltage | -0.3V to ($V_{CC} + 0.3$ V) |
| LVDS Differential Output Voltage | 0V to 1V |
| LVDS Output Short Circuit Current Duration | 5 ms |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature Range | |
| Soldering (4 sec.) | +260°C |
| Maximum Package Power Dissipation at 25°C | |
| M16A Package | 1.72W |
| Derate M16A Package | 13.75 mW/°C above +25°C |

Recommended Operating Conditions

| | Min | Typ | Max | Units |
|--|-----|-----|-----|-------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Receiver Differential Input Voltage (V_{ID}) | 0 | | 1 | V |
| Operating Free Air Temperature (T_A) | -40 | +25 | +85 | °C |

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------------|-----------------------------------|--|------|------|-----------------|-------|
| LVC MOS DC SPECIFICATIONS | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{DD} | V |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V |
| I_{IH} | High Level Input Current | $V_{IN} = 3.6$ V $V_{CC} = 3.6$ V | 40 | 175 | 250 | μA |
| I_{IL} | Low Level Input Current | $V_{IN} = \text{GND}$ $V_{CC} = 3.6$ V | | ±1 | ±10 | μA |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18$ mA, $V_{CC} = 0$ V | | -0.9 | -1.5 | V |
| LVDS INPUT DC SPECIFICATIONS | | | | | | |
| V_{ID} | Input Differential Voltage | $V_{CM} = +0.05$ V or $V_{CC} - 0.05$ V | 0 | | 1 | V |
| V_{TH} | Differential Input High Threshold | | | 0 | +100 | mV |
| V_{TL} | Differential Input Low Threshold | | -100 | 0 | | mV |
| V_{CMR} | Common Mode Voltage Range | $V_{ID} = 100$ mV | 0.05 | | $V_{CC} - 0.05$ | V |
| I_{IN} | Input Current | $V_{IN} = 3.6$ V or 0V $V_{CC} = 3.6$ V or 0V | | ±1 | ±10 | μA |
| C_{IN} | Input Capacitance | Any LVDS Input Pin to GND | | 1.7 | | pF |
| R_{IN} | Input Termination Resistor | Between IN+ and IN- | | 100 | | Ω |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|----------------------------|------|-----|-------|----------|
| LVDS OUTPUT DC SPECIFICATIONS | | | | | | |
| V_{OD} | Differential Output Voltage | $R_L = 100\Omega$ | 250 | 350 | 450 | mV |
| ΔV_{OD} | Change in Magnitude of V_{OD} for Complimentary Output States | | -35 | | 35 | mV |
| V_{OS} | Offset Voltage | $R_L = 100\Omega$ | 1.05 | 1.2 | 1.375 | V |
| ΔV_{OS} | Change in Magnitude of V_{OS} for Complimentary Output States | | -35 | | 35 | mV |
| I_{OS} | Output Short Circuit Current (Note 8) | OUT to GND | | -23 | -55 | mA |
| | | OUT to V_{CC} | | 8 | 55 | mA |
| C_{OUT} | Output Capacitance | Any LVDS Output Pin to GND | | 1.2 | | pF |
| R_{OUT} | Output Termination Resistor | Between OUT+ and OUT- | | 100 | | Ω |
| SUPPLY CURRENT | | | | | | |
| I_{CC} | Supply Current | EN0 = EN1 = H | | 58 | 70 | mA |
| I_{CCZ} | Outputs Powered Down Supply Current | EN0 = EN1 = L | | 25 | 30 | mA |

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .

Note 7: Typical values represent most likely parametric norms for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 9, 10)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|-------------------------------|--|---|-----------|-----|------|------|-------------------|
| LVDS OUTPUT AC SPECIFICATIONS | | | | | | | |
| t _{PLHD} | Differential Propagation Delay Low to High (Note 11) | R _L = 100Ω | | | 440 | 650 | ps |
| t _{PHLD} | Differential Propagation Delay High to Low (Note 11) | | | | 400 | 650 | ps |
| t _{SKD1} | Pulse Skew t _{PLHD} – t _{PHLD} (Notes 11, 12) | | | | 40 | 120 | ps |
| t _{SKD2} | Channel to Channel Skew (Notes 11, 13) | | | | 25 | 60 | ps |
| t _{SKD3} | Part to Part Skew (Notes 11, 14) | | | | 45 | 190 | ps |
| t _{LHT} | Rise Time (Note 11) | R _L = 100Ω | | | 170 | 350 | ps |
| t _{HLT} | Fall Time (Note 11) | | | | 170 | 350 | ps |
| t _{ON} | Output Enable Time | | | | 5 | 20 | μs |
| t _{OFF} | Output Disable Time | | | | 3 | 12 | ns |
| t _{SEL} | Select Time | | | | 3 | 12 | ns |
| JITTER PERFORMANCE (Note 11) | | | | | | | |
| t _{RJ1} | Random Jitter (RMS Value) | V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) | 135 MHz | | 0.5 | 1.2 | ps |
| t _{RJ2} | | | 311 MHz | | 0.5 | 1.2 | ps |
| t _{RJ3} | | | 503 MHz | | 0.5 | 1.2 | ps |
| t _{RJ4} | | | 750 MHz | | 0.5 | 1.2 | ps |
| t _{DJ1} | Deterministic Jitter (Peak-to-Peak Value) | V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) | 270 Mbps | | 9 | 38 | ps |
| t _{DJ2} | | | 622 Mbps | | 7 | 36 | ps |
| t _{DJ3} | | | 1.06 Gbps | | 7 | 34 | ps |
| t _{DJ4} | | | 1.5 Gbps | | 9 | 35 | ps |
| t _{TJ1} | Total Jitter (Peak to Peak Value) | V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) | 270 Mbps | | 0.01 | 0.03 | UI _{P-P} |
| t _{TJ2} | | | 622 Mbps | | 0.01 | 0.04 | UI _{P-P} |
| t _{TJ3} | | | 1.06 Gbps | | 0.01 | 0.05 | UI _{P-P} |
| t _{TJ4} | | | 1.5 Gbps | | 0.01 | 0.07 | UI _{P-P} |

Note 9: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 10: Typical values represent most likely parametric norms for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 13: t_{SKD2} , Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).

Note 14: t_{SKD3} , Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 15: Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

Note 16: Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

Note 17: Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

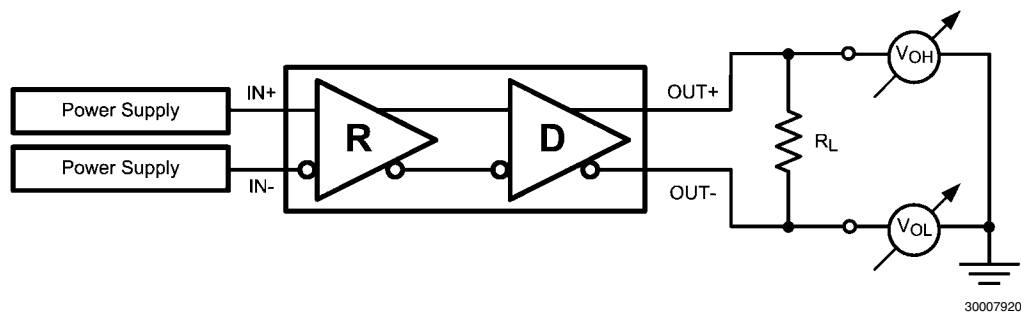


FIGURE 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

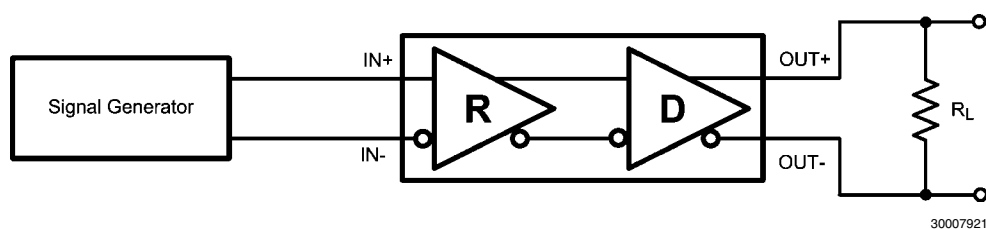


FIGURE 2. Differential Driver AC Test Circuit

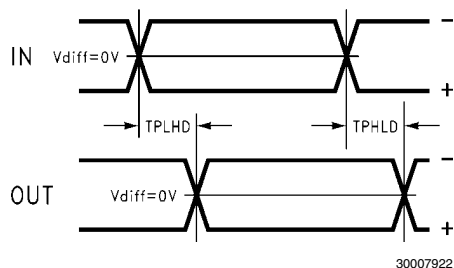


FIGURE 3. Propagation Delay Timing Diagram

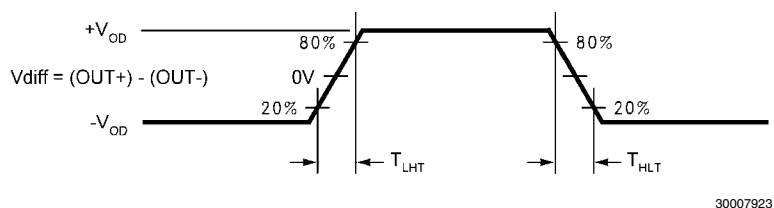


FIGURE 4. LVDS Output Transition Times

Functional Description

The DS10CP152 is a 1.5 Gbps 2x2 LVDS digital crosspoint switch optimized for high-speed signal routing and switching

over lossy FR-4 printed circuit board backplanes and balanced cables.

TABLE 1. Switch Configuration Truth Table

| SEL1 | SEL0 | OUT1 | OUT0 |
|------|------|------|------|
| 0 | 0 | IN0 | IN0 |
| 0 | 1 | IN0 | IN1 |
| 1 | 0 | IN1 | IN0 |
| 1 | 1 | IN1 | IN1 |

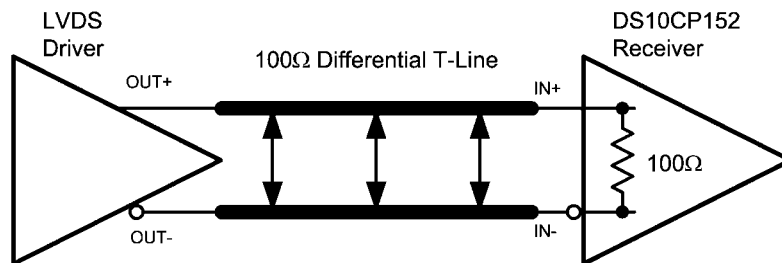
TABLE 2. Output Enable Truth Table

| EN1 | EN0 | OUT1 | OUT0 |
|-----|-----|----------|----------|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Disabled | Enabled |
| 1 | 0 | Enabled | Disabled |
| 1 | 1 | Enabled | Enabled |

INPUT INTERFACING

The DS10CP152 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS10CP152 can be DC-coupled with all common differential

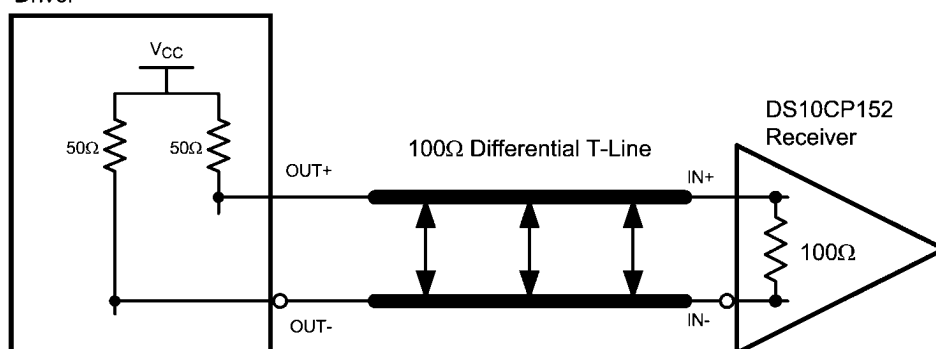
drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS10CP152 inputs are internally terminated with a 100Ω resistor.



Typical LVDS Driver DC-Coupled Interface to an DS10CP152 Input

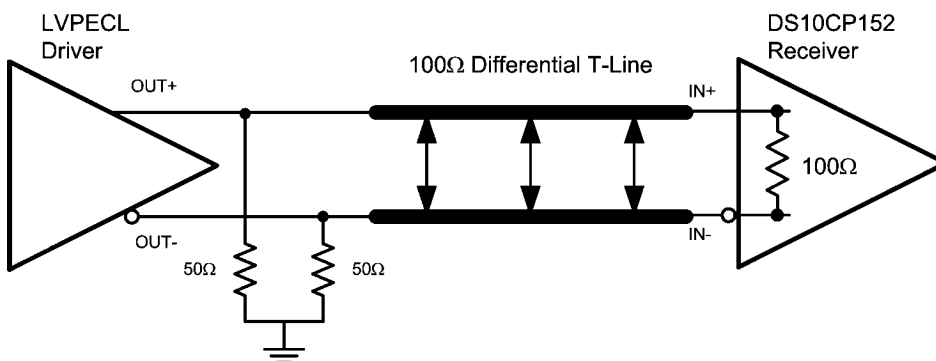
30007931

CML3.3V or CML2.5V
Driver



Typical CML Driver DC-Coupled Interface to an DS10CP152 Input

30007932



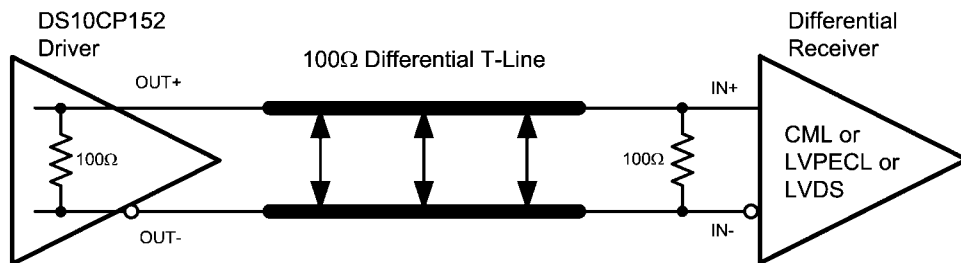
Typical LVPECL Driver DC-Coupled Interface to an DS10CP152 Input

30007933

OUTPUT INTERFACING

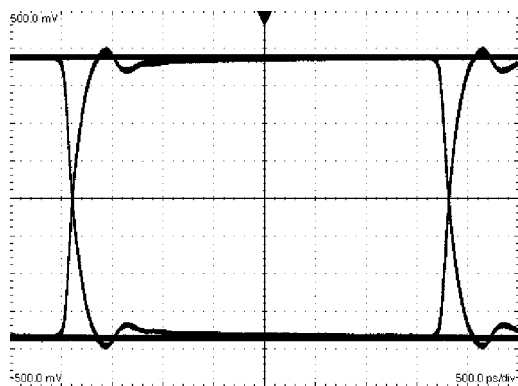
The DS10CP152 outputs signals compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and

assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

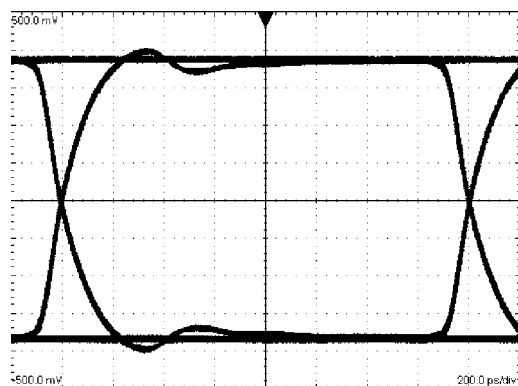


Typical DS10CP152 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver 30007934

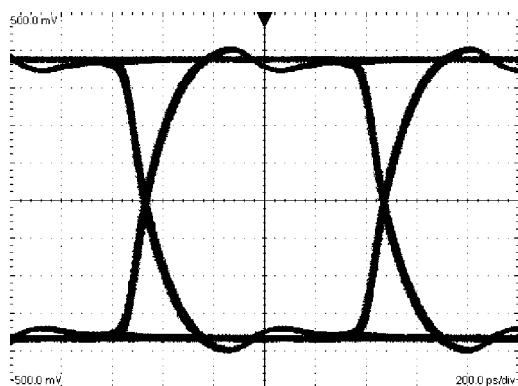
Typical Performance Characteristics



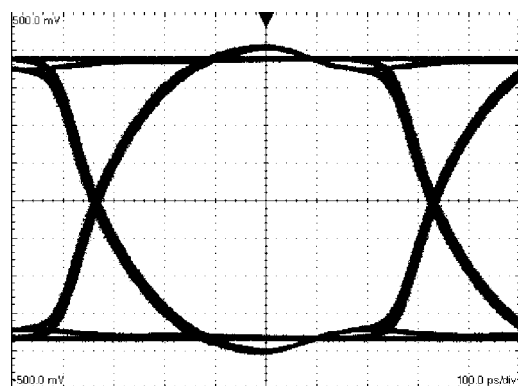
A 270 Mbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:500 ps / DIV



A 622 Mbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:200 ps / DIV



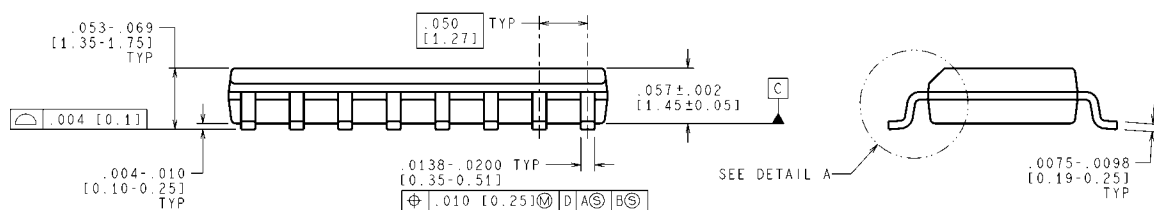
A 1.06 Gbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:200 ps / DIV



A 1.5 Gbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
V:100 mV / DIV, H:100 ps / DIV

The drawing shows a rectangular package with pins on all four sides. Key dimensions and features include:

- Top Dimension:** A distance of 16 from the left edge to the center of the first pin, and a total width of $3.90 \pm .004$ [9.91 \pm 0.1] between the centers of the first and last pins.
- Right Dimension:** A distance of 9 from the right edge to the center of the last pin.
- Left Dimension:** A total height of $.228 - .244$ [5.8 - 6.2] between the top and bottom edges.
- Right Dimension:** A distance of $.154 \pm .004$ [3.91 \pm 0.1] from the right edge to the center of the last pin.
- Pin 1 Identification:** A circle on the left side of the package is labeled "PIN 1 ID".
- Pin Numbers:** The pins are numbered 1 through 8, starting from the bottom-left and proceeding clockwise.



M16A (Rev J)

Notes

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