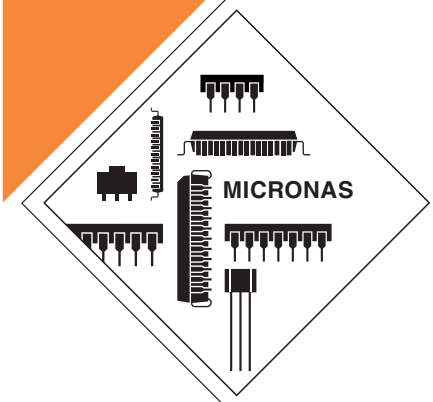


PRELIMINARY DATA SHEET

DRX 3975D
Fourth-Generation COFDM Demodulator

Edition Aug. 22, 2005
6251-659-1PD

MICRONAS

Contents

Fourth-Generation COFDM

1. Introduction

The DRX 3975D is a fourth-generation COFDM demodulator that offers today's highest level of front-end integration resulting in ultimate DVB-T digital reception, compliant to ETS 300 744, DTG D-Book, EICTA E-Book, and Nordig Unified v1.0.2 .

The IC applies cutting-edge digital filtering techniques in combination with a high-performance A/D-converter and PLL configuration, resulting in superior performance figures in the presence of digital- and analog adjacent channels.

Progressive channel estimator algorithms provide exceptional performance in multipath- and dynamic-echo conditions – an especially important feature for single-frequency networks and indoor reception.

The state-of-the-art impulsive noise cruncher suppresses interferences originating from sources such as cars, electrical motors, and household appliances.

1.1. Features

– Highest level of front-end integration and flexibility:
  • Single 8 MHz SAW filter operation
  • 2 AGC control signals available for RF and IF amplifier control
  • Flexible clock reference options
  • Re-use of 4 MHz tuner clock reference
  • Pre-SAW sense input for optimal RF AGC setting and RF-level measurement
– Excellent digital reception performance:
  • Superior digital and analog adjacent channel performance (> −40dB for QEF)
  • Impulsive noise cruncher
  • Multipath and dynamic echoes
– The input IF frequency ranging up to 44 MHz ensures upward compatibility for new tuner topologies
– Integrated microprocessor to perform autonomous detection and operation of all possible DVB-T modes, without interaction with the host processor
– Fully automatic and fast signal acquisition: UHF and VHF band-scan in <20 seconds
– Meets all international DVB-T receiver specifications: Nordig Unified, DTG, EICTA
– Comfortable software drivers for integration of tuner and COFDM demodulator
– Secondary serial interface for tuner control
– 5 V tolerant AGC and secondary serial protocol outputs
– 2 general purpose I/O pins (GPIO)
– Configurable parallel or serial MPEG-TS output
– PMQFP64 package: small footprint 10×10mm
– IEEE 1149.1 boundary scan

1.2. Applications

– IDTV / hybrid TV
– Set-top boxes
– PVR / DVDR
– Network interface modules (NIM)
– PC-TV applications

2. Functional Description

Fig. 2–1 shows a block diagram of the DVB-T demodulator. The next sections describe the behavior of the demodulator in more detail.

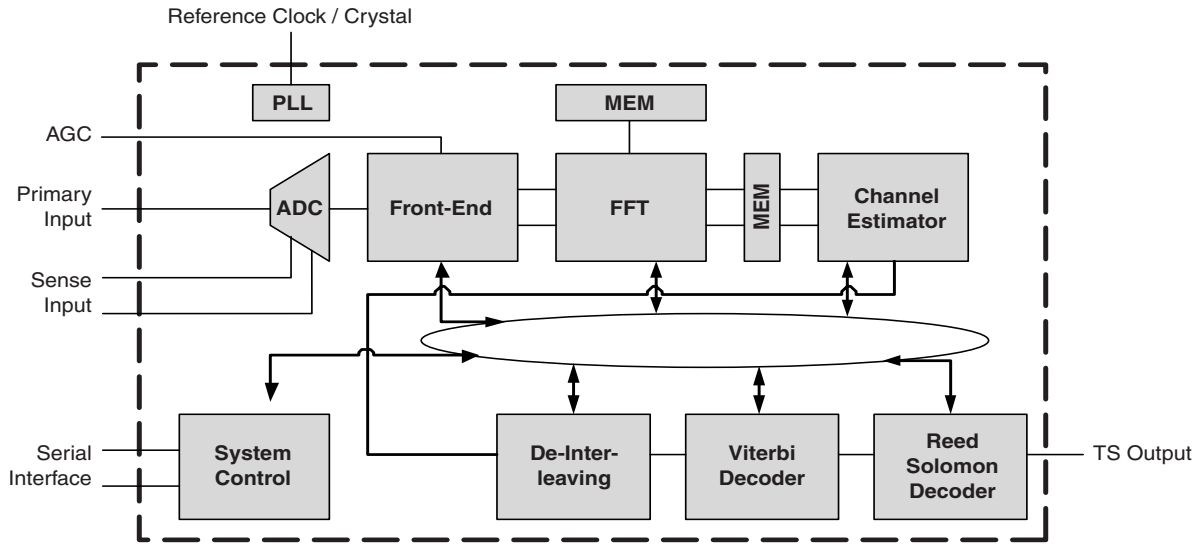


Fig. 2–1: Block diagram of the DVB-T demodulator

2.1. Input

The IC offers a very flexible sampling concept allowing users to apply a COFDM signal at various IF frequencies. Depending on the chosen SAW filter, one can program the DRX 3975D to accept IF frequencies in the range between 4 and 44 MHz. Optimum performance is achieved when centering the IF frequency around 12 or 36 MHz.

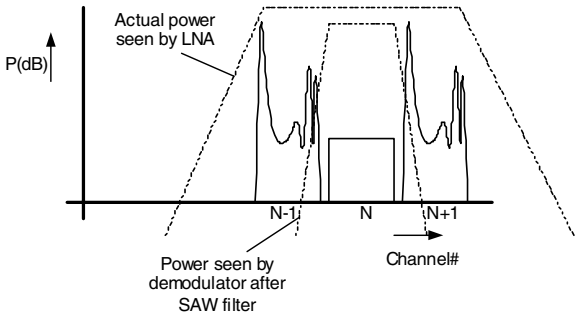


Fig. 2–2: Adjacent channel situation

2.2. Pre-SAW Sense Input

The pre-SAW sense input accurately measures all adjacent channel energy. It allows the DRX 3975D to control the RF amplifier stage of the tuner in its linear operating range. A stable and autonomous RF-AGC control loop is guaranteed. The pre-SAW sense input is needed in combination with tuners which do not have an own wide-band AGC.

2.3. AGC

The DRX 3975D provides two AGC control signals, resulting in two options for tuner and IF control.

2.3.1. Dual AGC

If the system in front of the demodulator consists of two variable amplifiers, the RF-AGC and IF-AGC signals are used to control both of them.

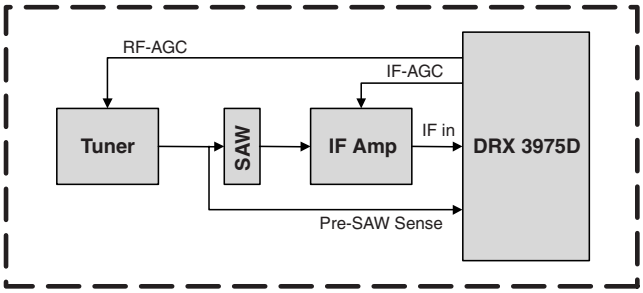


Fig. 2–3: Dual AGC application

2.3.2. IF AGC Only

When using a tuner with closed loop RF AGC, only the IF-AGC is required to control the IF amplifier.

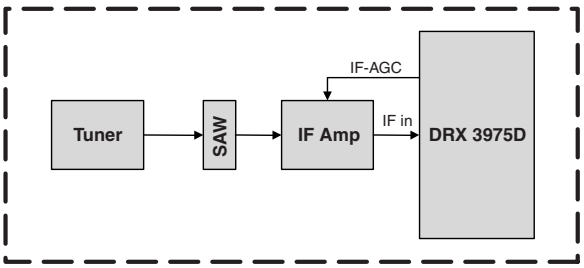


Fig. 2–4: Application with IF AGC only

2.3.3. AGC TOP setting

When RF AGC signal is used, the RF-AGC should be programmed so that an optimal setting of the available amplifiers in the system is chosen. Therefore, a take-over Point can be defined. The demodulator will increase the RF gain till the take-over-point (TOP) is reached. The demodulator uses the sense-input to measure the energy level. Further amplification is achieved by increasing the IF gain. A graphical representation of this behavior is shown in the following picture.

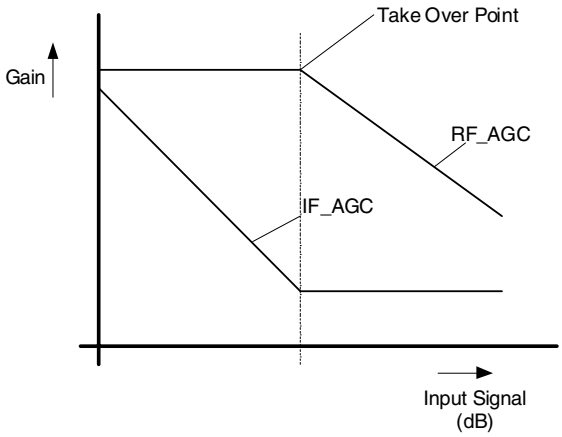


Fig. 2–5: AGC TOP setting

2.4. ADC

The IF input is sampled by a wideband 10 bits ADC. The clock of the ADC is generated by the integrated PLL. Additional filtering in front of the ADC is applied to further improve noise behavior and adjacent channel performance.

2.5. PLL

The clock source can either be a crystal connected to XI and XO or an external oscillator, such as a clock generated by a tuner. The frequency can range from 4 to 32 MHz. Please contact the Application Support group for the correct settings to support different clock frequencies

The integrated sample rate correction filters allow for intermediate frequencies to be applied. Once the DRX 3975D is informed about the used crystal frequency, the appropriate settings will automatically be applied. This for instance allows reuse of a 20.25 MHz crystal, that is used for the Micronas MPEG-2 decoder, the MDE 95xyD.

A high-quality, low phase-noise PLL is integrated to provide the clock for the ADC. This enables the use of a 4 MHz clock source as a reference. Many tuners provide a 4 MHz clock reference signal, which saves the need for an additional crystal.

2.6. Filter Section

High attenuation filters are implemented to filter remaining analog or digital adjacent signals. Besides IQ separation, sample rate correction is performed to match the actual sampling frequency to the incoming COFDM signal rate. Coarse synchronization takes place so that the output of the FFT can be used for further processing of the reference information available in the COFDM signal.

2.7. FFT

A 2k and 8k points FFT is implemented to convert the time-domain signal coming from the front-end to the frequency domain. The near-floating point algorithm allows a very high dynamic range to be covered without saturating the different stages of the FFT.

2.8. Channel Estimator

The channel estimator forms the heart of the DRX 3975D. The channel estimator reconstructs the shape of the received (and possibly distorted) channel, making use of the pilot signals. These channel characteristics are used to equalize the frequency response of the channel, for all carriers.

The channel estimator uses progressive digital algorithms to minimize noise and to maximize echo performance in both static and dynamic environments. In a single receiver setup, a common 64QAM DVB-T signal with 0 dB echoes, degraded with 21 dB of noise, can be received by the DRX 3975D with a quasi error-free (QEF) quality.This makes the DRX 3975D very suitable for single frequency networks (SFN) and indoor reception.

The dynamic pre-echo detection enables the DRX 3975D to detect changes in the reception environments. Appearance of pre-echoes as well as post-echoes is communicated to the channel estimation algorithm, assuring optimum time-domain synchronization for maximum performance.

The channel estimator reports the channel characteristics to the error correction unit for effective error correction. Several channel quality indicators are made available to interface to the host controller, for example C/N, BER. This information can be used to realize a signal quality indicator, using the appropriate DRX 3975D software driver functions.

2.9. Error Correction

Next to the de-interleaving functions described in the ETS300 744 standard, the error correction unit of the DRX 3975D comprises a Viterbi decoder and a Reed Solomon decoder, which will produce an error-free output signal, using the channel state information of the channel estimator. BER values are calculated and made available to the host application.

2.10. System Control

The DRX 3975D is controlled by a dedicated, integrated processor. The microcode, containing all necessary control algorithms (firmware), is loaded at power-up. In combination with the DRX 3975D software driver, the processor takes care of initialization and control of the complete front-end, including the tuner.

The processor can detect all COFDM and channel-related parameters automatically, independent from the TPS information, which speeds up locking time and “zap-behavior”. Parameters involved are: frequency offset; signal bandwidth; spectrum inversion; COFDM mode (2k/8k); guard interval; constellation; code rate; hierarchy.

Also, the TPS data and cell ID are extracted and made available via one of the DRX 3975D software driver functions.

Resulting from the autonomous operation of the DRX 3975D, including COFDM detection and configuration, the interaction with the application host-processor is kept to a minimum.

2.11. Transport Stream

The IC supports a serial as well as a parallel Transport Stream (=TS) interface. The parallel TS interface consists of a TS clock, valid, start, error and data[7:0]. The serial interface uses the same interface with the only difference that the serial data is output on the lowest TS data pin MD[0].

Table 2–1: Transport Stream signals

TS Interface	Description
MCLK	TS clock
MVAL	TS valid
MSTRT	TS start
MERR	TS error
$MD\_[7:0]_{parallel}/MD\_[0]_{serial}$	TS data

A digital time oscillator (= DTO) has been provided to minimize PCR jitter. The DTO is able to generate a “variable” or “fixed” TS clock. In “variable” mode, the TS clock is automatically and continuously adapted to match the channel bit-rate. In “fixed” mode, the closest TS clock derived from the 48 MHz system clock is chosen to match the channel bit-rate.

2.11.1.Transport Stream Data Format

The TS data consists of TS packets of 204 bytes. Each packet consists of 188 MPEG bytes and 16 parity bytes. The first byte of a TS packet contains the sync byte (=47hex). If a TS packet contains errors, the transport error indicator (=TEI) is set. The MSB bit of the second byte is the transport error indicator (see Fig. 2–6).

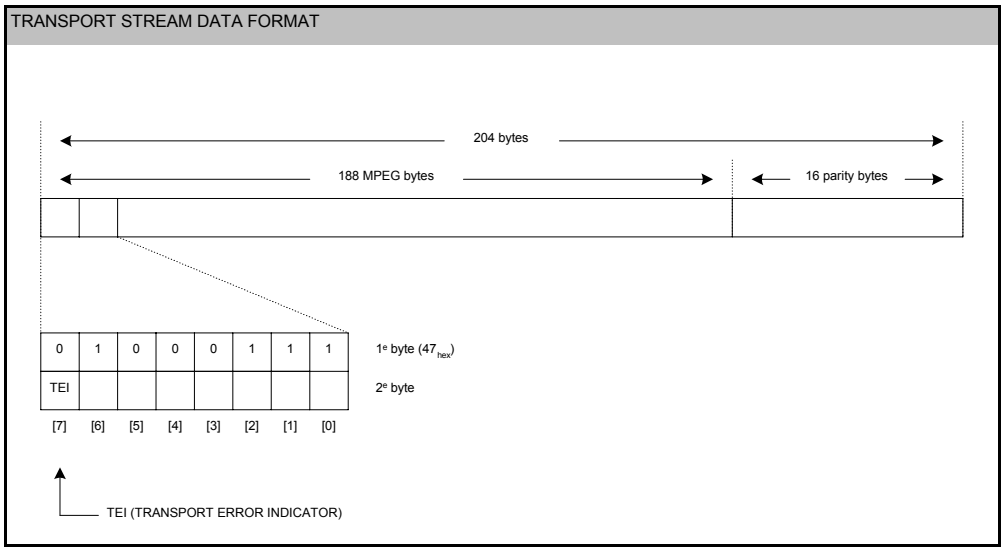


Fig. 2–6: Transport Stream data format

2.11.2.Transport Stream interface

The TS data is transmitted through the TS interface. The TS data consists of TS packets of 204 bytes. By default, only the 188 MPEG bytes are output. The 16 parity bytes are output optionally. By default, the TS clock is continuously adapted to match the channel bit-rate. In this mode, there are no interruptions or discontinuities in the TS data (valid is always active[1)]. When the TS clock is fixed, there are interruptions or discontinuities in the TS data (valid is not always active[1)].

The TS interface signals; valid, start, error and data, change on the negative edge of the TS clock so the interface signals should be latched on the **positive edge** of the TS clock.

The TS clock (= ***MCLK***) is a continuously running clock. The clock can optionally be disabled during the interpacket gaps (if available). The TS valid (= ***MVAL***) is active[1)] during the transmission of the 188 MPEG bytes. The valid can optionally be set active[1)] during the transmission of the parity bytes.

The TS start (= ***MSTRT***) is active[1)] during the first byte (= 47_{hex} sync byte) of a TS packet. The TS error (= ***MERR***) is set active[1)] when a packet contains errors. The error is active[1)] during the transmission of the 188 MPEG bytes. The error can optionally be set active[1)] during the transmission of the parity bytes. The TS data (= ***MD_[7:0]***) is default output in parallel mode.

In serial mode the TS data is output on the lowest TS data pin (= ***MD_[0]***). The TS data is output in MSB first format. Optionally the TS data can be output in LSB first format. The TS valid (= ***MVAL***) is active[1)] during the transmission of a byte. The TS start (= ***MSTRT***) is active[1)] during the first bit (= MSB) of the first byte (= 47_{hex} sync byte) of a TS packet. The TS start can optionally be set active[1)] during the transmission of all the bits of first byte (= 47_{hex} sync byte). The TS error (= ***MERR***) is set active[1)] during the transmission of a byte when a packet contains errors.

All the TS interface signals (clock, valid, start, error and data) can be inverted independently.

[1)] Default state active = high.

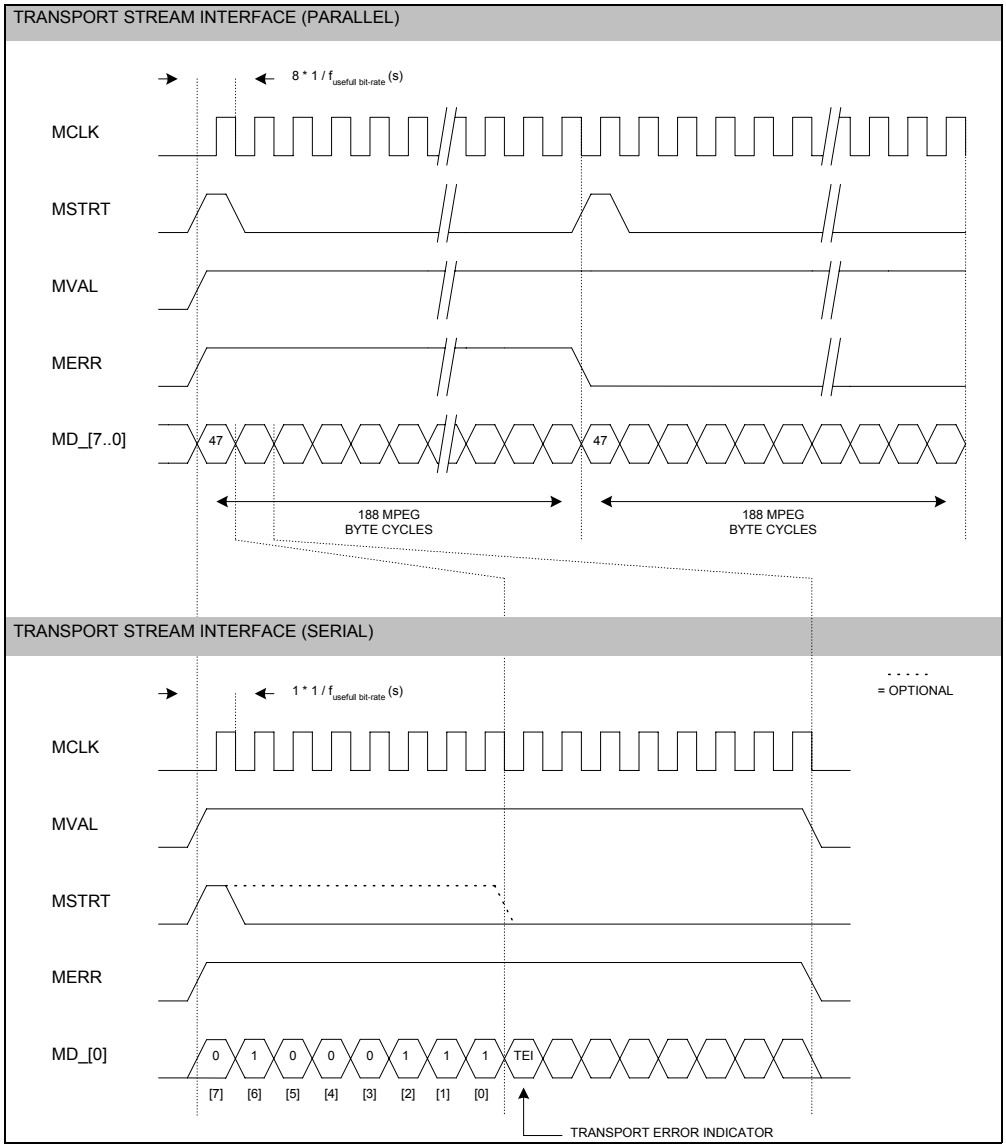


Fig. 2–7: Transport Stream interface (no parity bytes)

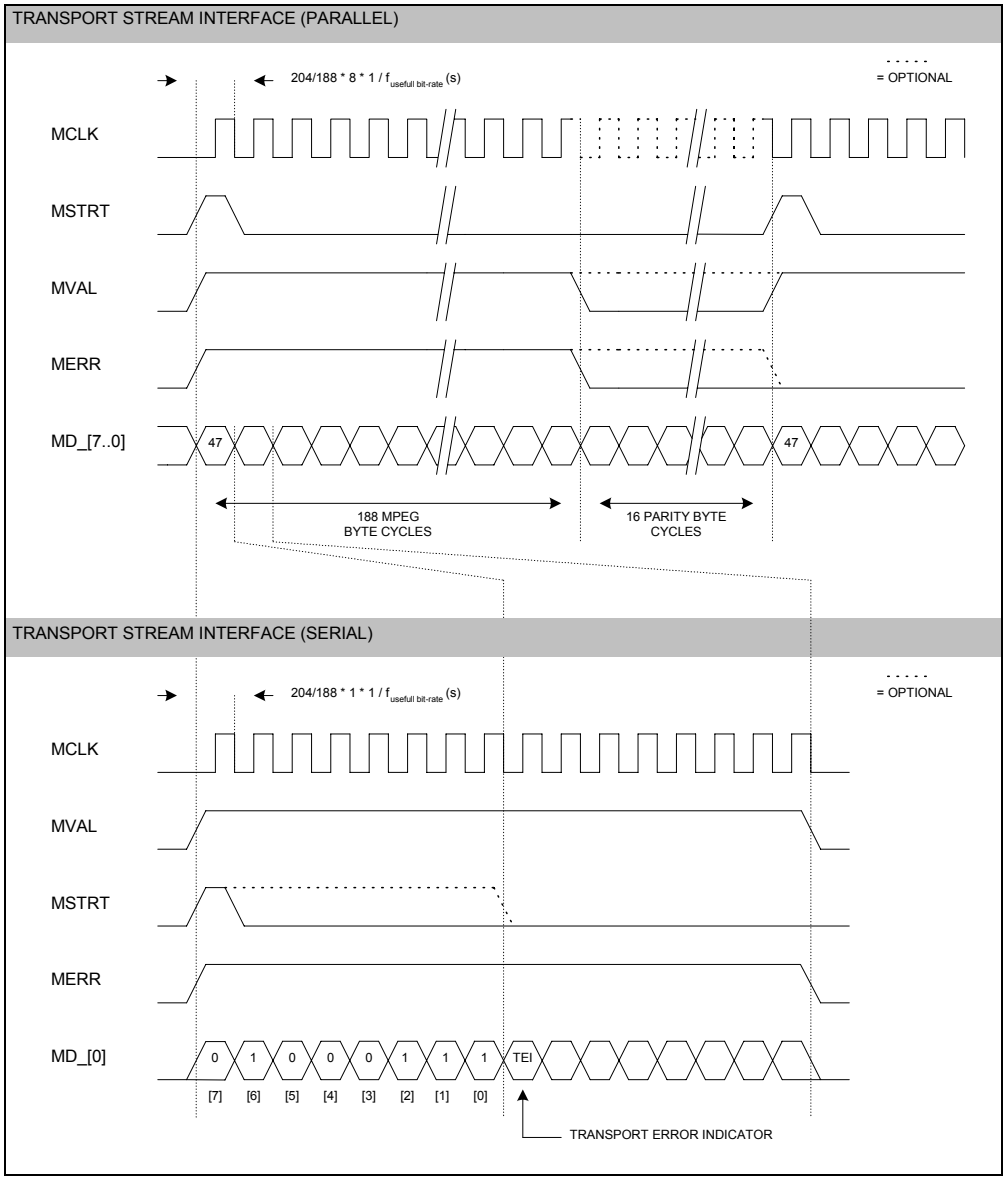


Fig. 2–8: Transport Stream interface (with parity bytes)

3. Control Interface

3.1. Serial Interface

The DRX 3975D is controlled via an I^2C compatible serial interface. The host application utilizes low-level read/write I^2C functions to control the device driver. A wide range of I^2C access protocols is supported, ranging from a simple 5 Bytes access with no ‘repeated start’ to more enhanced multiple access modes for faster control.

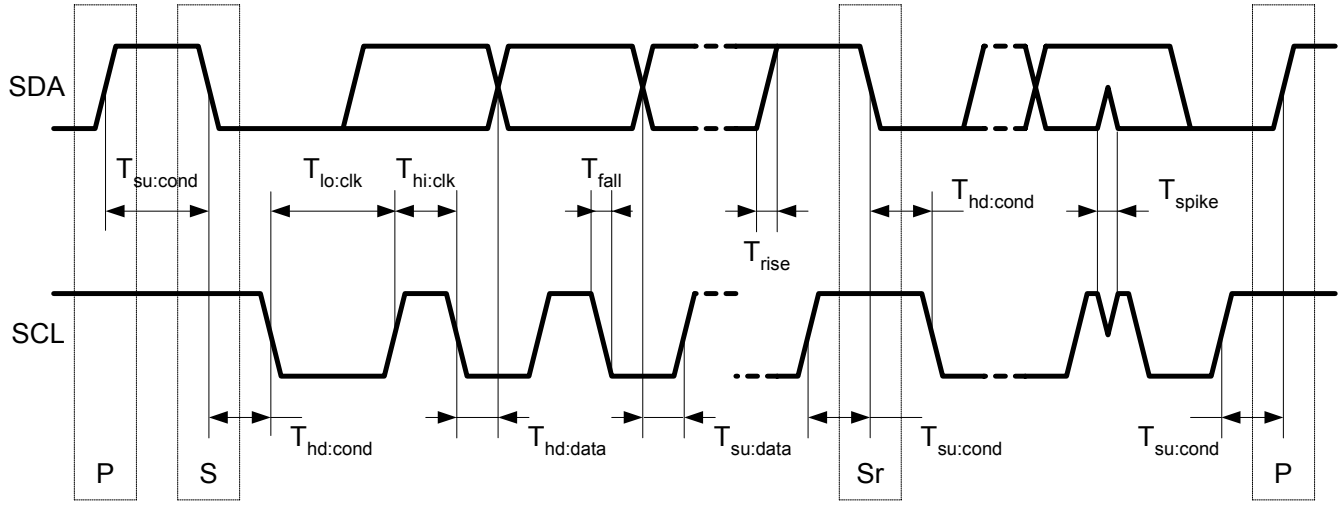


Fig. 3–1: Serial protocol timing diagram P=Stop, S=Start, Sr=Repeated Start.

3.2. Serial Protocol

The timing diagram shows the various timing parameters for connection to an I^2C bus. The actual timing depends on the setting of the I^2C timing divider denoted here as T_{div}. This value is used to divide the system clock before it is used to time the several periods when driving the bus signals. The relation is shown in the formula column in the table below.

Table 3–1: Serial interface timing parameters

Parameter	Formula	Type	Low Speed	High Speed
T_{div}		–	12	4
T_{spike}	$4 \times P_{sys\_clk}$	max	83 ns	83 ns
T_{rise}	$4 \times P_{sys\_clk} \times T_{div}$	max	1000 ns	333 ns
T_{fall}	$2 \times P_{sys\_clk} \times T_{div}$	max	500 ns	166 ns
$T_{hi:clk}$	$16 \times P_{sys\_clk} \times T_{div}$	min	4000 ns	1333 ns
$T_{lo:clk}$	$19 \times P_{sys\_clk} \times T_{div}$	min	4750 ns	1583 ns
$T_{su:data}$	$9 \times P_{sys\_clk} \times T_{div}$	min	2250 ns	750 ns
$T_{hd:data}$	$10 \times P_{sys\_clk} \times T_{div}$	min	2500 ns	833 ns
$T_{su:cond}$	$19 \times P_{sys\_clk} \times T_{div}$	min	4750 ns	1583 ns
$T_{hd:cond}$	$16 \times P_{sys\_clk} \times T_{div}$	min	4000 ns	1333 ns

3.3. Software Driver Functions

The driver functions that are available to initialize and control the DRX 3975D is described in a separate Software User Guide.

The driver will rely on a low level I^2C read/write function to be supplied by the host application. The function prototype is:

```
DRXStatus_t DRXBSP_I2C_WriteRead (

pI2CdeviceAddr        wdevAddr,

u16_t                 wcount,

pu8_t                 wdata,

pI2CdeviceAddr_t      rdevAddr,

u16_t                 rcount,

pu8_t                 rdata )
```

And must result in the following I^2C activity:

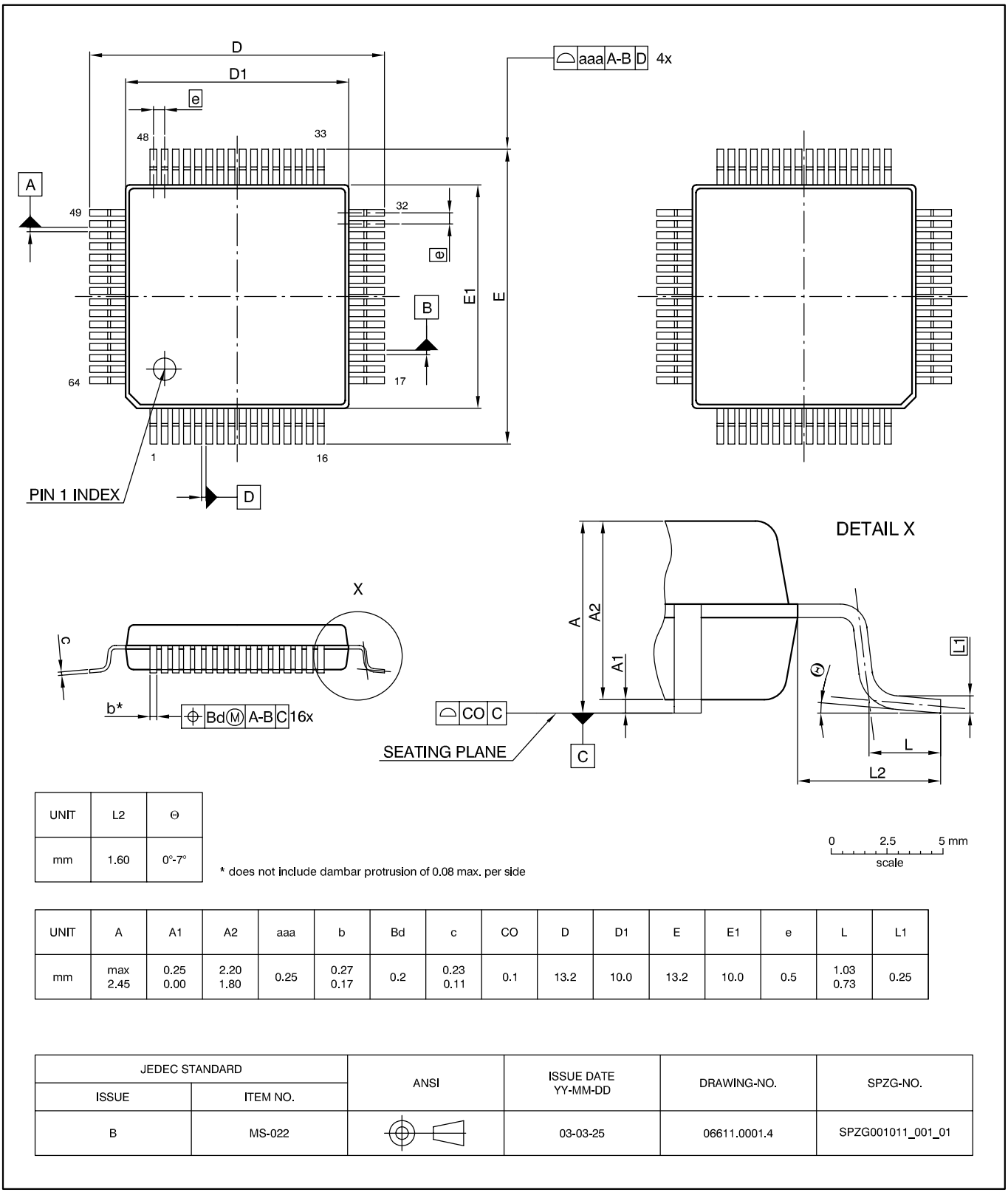
S(tart) *wdevAddr wdata* (sto)**P** **S**(tart) *rdevAddr rdata* (sto) **P**

wdevAddr points to the address of the DRX 3975D which depends on the value applied to pin 53 (ASEL). The chip address is 0xE0 when ASEL is connected to ground and 0xE2 when ASEL is connected to VDDH. The rdevAddr points to the same address as wdevAddr with the lowest bit inverted (0xE1 or 0xE3). *wdata* will have the length of *wcount* and *rdata* will have the length of *rcount*. In cases where the host can operate with repeated starts, the middle (sto)P is not necessary .

Once this function is made available by the customer, the high level drivers can be compiled into the host application to allow programming of the DRX 3975D with a minimum of effort. For more details, please refer to the Software User Guide.

4. Specifications

4.1. Outline Dimensions



UNIT	L2	Θ
mm	1.60	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	max 2.45	0.25 0.00	2.20 1.80	0.25	0.27 0.17	0.2	0.23 0.11	0.1	13.2	10.0	13.2	10.0	0.5	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-03-25	06611.0001.4	SPZG001011_001_01

Fig. 4–1:
Plastic Metric Quad Flat Package, 64 leads, 10 × 10 × 2 mm^3
(PMQFP64-2)
Weight approximately 0.5 g

4.2. Pin Connections and Short Descriptions

NC = not internally connected, leave unconnected on PCB
DNC = if not used, do not connect!

.
Table 4–1: DRX 3975D Pinning

Pin No.	Pin Name	Type	Connection (if not used)	Description
1	IRQN	IN/OUT	DNC	Interrupt Request (active low) or user-programmable IO-2
2	RSTN	IN		Reset (active low)
3	VDDL	SUPPLY		Digital 1.8 V
4	VSSL	SUPPLY		Digital GND
5	NC		DNC	Not Connected
6	NC		DNC	Not Connected
7	NC		DNC	Not Connected
8	NC		DNC	Not Connected
9	NC		DNC	Not Connected
10	NC		DNC	Not Connected
11	NC		DNC	Not Connected
12	NC		DNC	Not Connected
13	VSSH	SUPPLY		Digital GND
14	VDDH	SUPPLY		Digital 3.3 V
15	SCL1	IN/OUT		Primary Serial Interface Clock
16	SDA1	IN/OUT		Primary Serial Interface Data
17	MCLK	OUT	DNC	MPEG Clock
18	MVAL	OUT	DNC	MPEG Valid
19	VDDL	SUPPLY		Digital 1.8 V
20	VSSL	SUPPLY		Digital GND
21	MSTRT	IN/OUT		MPEG Start. See application note for pull-up/pull-down resistor requirements determining Primary Serial Interface frequency setting.
22	MERR	IN/OUT		MPEG Error. See application note for pull-up/pull-down resistor requirements determining Primary Serial Interface frequency setting.
23	VSSH	SUPPLY		Digital GND
24	VDDH	SUPPLY		Digital 3.3 V
25	MD_0	OUT		MPEG Data[0] or MPEG serial data
26	MD_1	OUT	DNC	MPEG Data[1]

Table 4–1: DRX 3975D Pinning

Pin No.	Pin Name	Type	Connection (if not used)	Description
27	MD_2	OUT	DNC	MPEG Data[2]
28	MD_3	OUT	DNC	MPEG Data[3]
29	MD_4	OUT	DNC	MPEG Data[4]
30	MD_5	OUT	DNC	MPEG Data[5]
31	MD_6	OUT	DNC	MPEG Data[6]
32	MD_7	OUT	DNC	MPEG Data[7]
33	SDA2	IN/OUT		Secondary (tuner) Serial Interface Data (open-collector 5 V tolerant)
34	SCL2	IN/OUT		Secondary (tuner) Serial Interface Clock (open-collector 5 V tolerant)
35	VDDL	SUPPLY		Digital 1.8 V
36	VSSL	SUPPLY		Digital GND
37	VDDAH	SUPPLY		Analog 3.3 V
38	INP	IN		differential IF in
39	INN	IN		differential IF in (inverted)
40	VSSAH	SUPPLY		Analog GND
41	PDP	IN		differential Pre-SAW sense in
42	PDN	IN		differential Pre-SAW sense in (inverted)
43	VDDAL	SUPPLY		Analog 1.8 V
44	VSSAL	SUPPLY		Analog GND
45	RES	IN	DNC	Bias
46	SUBA	SUPPLY		Analog GND
47	VDDAL	SUPPLY		Analog 1.8 V
48	VSSAL	SUPPLY		Analog GND
49	NC		DNC	Digital GND
50	NC		DNC	Digital 3.3 V
51	VDDL	SUPPLY		Digital 1.8 V

Table 4–1: DRX 3975D Pinning

Pin No.	Pin Name	Type	Connection (if not used)	Description
52	VSSL	SUPPLY		Digital GND
53	ASEL	IN		Adress Select Primary Serial Interface
54	UIO	IN/OUT	DNC	User Programmable IO-1
55	VSSH	SUPPLY		Digital GND
56	XO	OUT		Crystal Oscillator out
57	XI	IN		Crystal Oscillator in or Clock in
58	VDDH	SUPPLY		Digital 3.3 V
59	TDO	OUT		JTAG Test Data Out
60	TMS	IN		JTAG Test Mode Select
61	TCK	IN		JTAG Test Clock
62	TDI	IN		JTAG Test Data In
63	AGC1	OUT	DNC	Automatic (IF tuner) Gain Control 1 (open collector 5 V tolerant)
64	AGC2	OUT	DNC	Automatic (RF tuner) Gain Control 2 (open collector 5 V tolerant)

Note: 5.0 V should never be applied when the 3.3 V is down

4.3. Pin Configuration

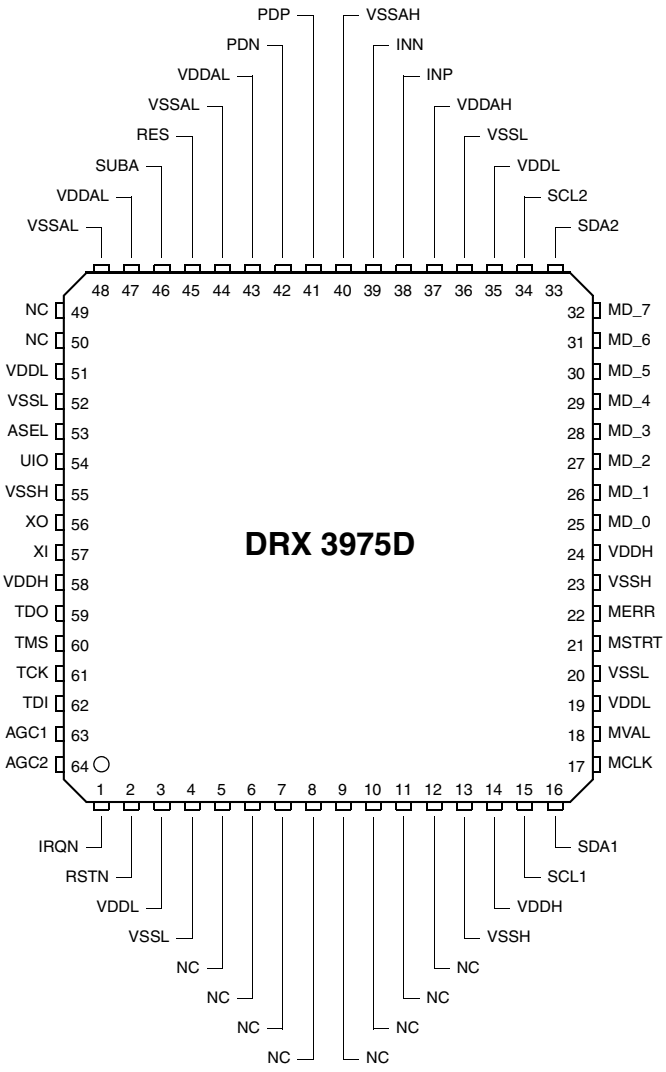


Fig. 4–2: PMQFP64-2 package

4.4. Electrical Characteristics

Abbreviations:

tbd = to be defined
vacant = not applicable
positive current values mean current flowing into the chip

4.4.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

All voltages listed are referenced to ground except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Table 4–2: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
T_A [1]	Ambient Temperature		–10	70 [2]	°C
T_C	Case Temperature		–10	105 [3]	°C
T_S	Storage Temperature		–40	125	°C
P_{MAX}	Maximum Power Dissipation		–	1200 [1, 3]	mW
V_{DDL}	Digital 1.8 V	VDDL	–0.3	2.0	V
V_{DDH}	Digital 3.3 V	VDDH	–0.3	3.6	V
V_{DDAL}	Analog 1.8 V	VDDAL	–0.3	2.0	V
V_{DDAH}	Analog 3.3 V	VDDAH	–0.3	3.6	V
V_{SUP_DIF}	Voltage difference within supply domains of the same supply voltage		0	0.2	V
$V_{I\ ANALOG}$	Analog input voltage	INP, INN	–0.2	2.1	V

[1] Measured on Micronas typical 2-layer (1s1p) board based on JESD - 51.2 Standard with maximum power consumption allowed for this package

[2] A power-optimized board layout is recommended. The Case Temperature mentioned in the “Absolute Maximum Ratings” must not be exceeded at worst case conditions of the application.

[3] Package limit

Table 4–2: Absolute Maximum Ratings, continued

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
I_I	Input Current	RSTN, INP, INN, PDP, PDN, RES, ASEL, XI, TMS, TCK, TDI, SCL1, SDA1, MSTRT, MERR, SDA2, SCL2, UIO, IRQN,	tbd	tbd	mA
I_O	Output Current	SCL1, SDA1, MSTRT, MERR, SDA2, SCL2, UIO, IRQN, MCLK, MVAL, MD_0, MD_1, XO, AGC1, AGC2, MD_2, MD_3, MD_4, MD_5, MD_6, MD_7, TDO,	tbd	tbd	mA
$V_{IDIG, 5.0V}$	Digital input voltage, 5.0 V compliant	AGC1, AGC2, SCL2, SDA2	–0.3	5.4	V
$V_{IDIG, 3.3V}$	Digital input voltage, 3.3 V	ASEL, UIO, IRQN, TDI, TMS, TCK, RSTN, SCL1, SDA1	–0.3	3.6	V
$V_{ODIG, 5.0V}$	Digital output voltage, 5.0 V compliant	AGC1, AGC2, SCL2, SDA2	–0.3	5.4	V
$V_{ODIG, 3.3V}$	Digital output voltage, 3.3 V	UIO, MCLK, MVAL, MD_0, MD_1, MD_2, MD_3, MD_4, MD_5, MD_6, MD_7, MSTRT, MERR, TDO, SCL1, SDA1	–0.3	3.6	V

Note: 5.0 V should never be applied when the 3.3 V is down

4.4.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions/Characteristics” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

All voltages listed are referenced to ground except where noted.

All GND pins must be connected to a low-resistive ground plane (0 V) close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Note: 5.0 V should never be applied when the 3.3 V is down

4.4.2.1. General Recommended Operating Conditions

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
T_A	Ambient Operating Temperature		0	25	70[1)]	°C
T_C	Case Operating Temperature PMQFP64-2		0	tbd	tbd	°C
V_{DDL}	Digital 1.8 V	VDDL	1.67	1.8	1.94	V
V_{DDH}	Digital 3.3 V	VDDH	3.05	3.3	3.55	V
V_{DDAL}	Analog 1.8 V	VDDAL	1.67	1.8	1.94	V
V_{DDAH}	Analog 3.3 V	VDDAH	3.05	3.3	3.55	V
V_{SUP_DIF}	Voltage difference within supply domains of the same supply voltage		–	–	0.1	V
I_I	Input Current	RSTN, INP, INN, PDP, PDN, RES, ASEL, XI, TMS, TCK, TDI, SCL1, SDA1, MSTRT, MERR, SDA2, SCL2, UIO, IRQN,	tbd	tbd	tbd	mA
I_O	Output Current	SCL1, SDA1, MSTRT, MERR, SDA2, SCL2, UIO, IRQN, MCLK, MVAL, MD_0, MD_1, XO, AGC1, AGC2, MD_2, MD_3, MD_4, MD_5, MD_6, MD_7, TDO,	tbd	tbd	tbd	mA

1) A power-optimized board layout is recommended. The Case Operating Temperatures mentioned in the “Recommended Operating Conditions” must not be exceeded at worst case conditions of the application.

4.4.3. Characteristics

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
DC Electrical Characteristics							
I_{DDL}	Supply Current Digital 1.8 V	VDDL	–	161	tbd	mA	
I_{DDH}	Supply Current Digital 3.3 V	VDDH	–	3	tbd	mA	10 pF load on MPEG transport stream interface (parallel)
I_{DDAL}	Supply Current Analog 1.8 V	VDDAL	–	38	tdb	mA	
I_{DDAH}	Supply Current Analog 3.3 V	VDDAH	–	16	tbd	mA	
P_{TOT}	Total Power Consumption		–	420	tbd	mW	
$P_{STANDBY}$	Power Consumption Standby (= Power Down) Mode		–	8	tbd	mW	
Stand-by Mode							
t_{SETUP}	Setup Time From Standby (= Power Down) To Operation		–	–	6	ms	
Reset Input, RSTN							
t_{RESET}	Active Reset Time	RSTN	0.1	–	–	µs	
Digital Inputs							
Pad Type: 3.3 V Input/Output							
$V_{I, L}$	Input Voltage Low	ASEL, UIO, IRQN, SCL1, SDA1	–0.3	0	0.9	V	
$V_{I, H}$	Input Voltage High	ASEL, UIO, IRQN, SCL1, SDA1	2.2	3.3	3.6	V	
C_I	Input Capacitance	ASEL, UIO, IRQN, SCL1, SDA1		tbd		pF	
Pad Type: 3.3 V Input/Output (5 V tolerant)							
$V_{I, L}$	Input Voltage Low	SCL2, SDA2, AGC1, AGC2	–0.3	0	0.9	V	
$V_{I, H}$	Input Voltage High	SCL2, SDA2, AGC1, AGC2	2.2	3.3	5.4	V	
C_I	Input Capacitance	SCL2, SDA2, AGC1, AGC2		tbd		pF	

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Pad Type: 3.3 V Input (internal pull-up)							
$V_{I, L}$	Input Voltage Low	TDI, TMS, TCK, RSTN	–0.3	0	0.9	V	
$V_{I, H}$	Input Voltage High	TDI, TMS, TCK, RSTN	2.2	3.3	3.6	V	
C_I	Input Capacitance	TDI, TMS, TCK, RSTN	–	tbd		pF	
Digital Outputs							
Pad Type: 3.3 V Input/Output							
$V_{O, L}$	Output Voltage Low	UIO, IRQN, MCLK, MVAL, MD_0, MD_1, MD_2, MD_3, MD_4, MD_5, MD_6, MD_7, MSTRT, MERR, TDO, SCL1, SDA1	–	0	0.4	V	
$V_{O, H}$	Output Voltage High	UIO, IRQN, MCLK, MVAL, MD_0, MD_1, MD_2, MD_3, MD_4, MD_5, MD_6, MD_7, MSTRT, MERR, TDO, SCL1, SDA1	2.8	3.3	–	V	
C_o	Output Capacitance	UIO, IRQN, MCLK, MVAL, MD_0, MD_1, MD_2, MD_3, MD_4, MD_5, MD_6, MD_7, MSTRT, MERR, TDO, SCL1, SDA1	–	tbd	–	pF	
Pad Type: 3.3 V Input/Output (5 V tolerant)							
$V_{O, L}$	Output Voltage Low	SCL2, SDA2, AGC1, AGC2	–	0	0.4	V	
$V_{O, H}$	Output Voltage High	SCL2, SDA2, AGC1, AGC2	2.8	3.3	–	V	
C_o	Output Capacitance	SCL2, SDA2, AGC1, AGC2	–	tbd	–	pF	

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Analog IF Inputs							
Anti Alias Filter (= AAF) in							
$V_{IF, DC}$	IF Input Dc Bias Level	INP,INN	tbd	tbd	tbd	V	
$R_{IF, I}$	IF Input Resistance	INP,INN	–	2	–	kΩ	
$C_{IF, I}$	IF Input Capacitance	INP,INN	–	3	–	pF	
V_{IF}	IF Differential Input Range (Pk-pk)	INP,INN	tbd	tbd	tbd	V	
Analog-to-Digital Converter (= ADC) in							
$V_{IF, DC}$	IF Input Dc Bias Level	INP,INN	0.6	0.7	0.8	V	
$R_{IF, I}$	IF Input Resistance	INP,INN	–	tbd	–	kΩ	
$C_{IF, I}$	IF Input Capacitance	INP,INN	–	tbd	–	pF	
V_{IF}	IF Differential Input Range (Pk-pk)	INP,INN	1.4	1.5	1.6	V	
Peak Detector 2 (= PD2) in							
$V_{IF, DC}$	IF Input Dc Bias Level	PDP, PDN	tbd	tbd	tbd	V	
$R_{IF, I}$	IF Input Resistance	PDP, PDN	–	10	–	kΩ	
$C_{IF, I}$	IF Input Capacitance	PDP, PDN	–	tbd	–	pF	
V_{IF}	IF Differential Input Range (Pk-pk)	PDP, PDN	tbd	tbd	tbd	V	
Clock Input							
f_{XI}	External Clock Frequency	XI	tbd	4	tbd	MHz	
	External Clock Duty Cycle	XI	tbd	tbd	tbd	%	
$t_{XI, RISE}$	External Clock Rise Time	XI	–	tbd	–	ns	
$t_{XI, FALL}$	External Clock Fall Time	XI	–	tbd	–	ns	

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Crystal							
f_{XTAL-1}	Fundamental Frequency – 1	XI, XO	tbd	4.0	tbd	MHz	
f_{XTAL-3}	Fundamental Frequency – 3	XI, XO	tbd	20.00	tbd	MHz	
f_{MAX}/f_{XTAL}	Maximum Allowed Frequency Deviation	XI, XO	–50	–	50	ppm	
C_P	Load Capacitance	XI, XO	–	tbd	–	pF	
R_R	Series Resistance	XI, XO	–	50	tbd	W	
C_M	Motional Capacitance	XI, XO	tbd	–	tbd	fF	
C_O	Parallel Capacitance	XI, XO	–	–	tbd	pF	
$C_{L, EXT}$	External Load Capacitance To Ground	XI, XO	10	tbd	30	pF	

4.4.3.1. Serial Interface

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$f_{serial\_interface}$	Serial interface bus frequency	SCL1, SDA1, SCL2, SDA2	–	–	400	kHz	
$t_{HD, START}$	Serial interface start condition hold time	SCL1, SDA1, SCL2, SDA2	1.4	–	–	µs	
$t_{SU, STOP}$	Serial interface stop condition setup time	SCL1, SDA1, SCL2, SDA2	1.6	–	–	µs	

4.4.4. Timing Diagrams

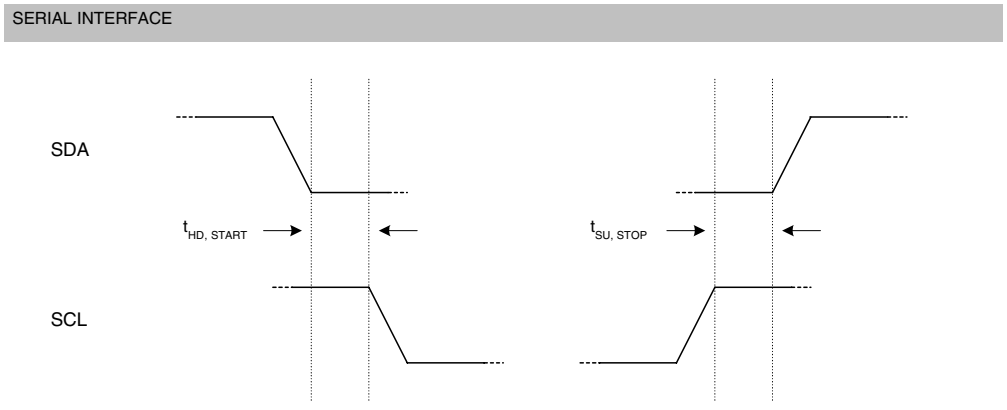


Fig. 4–1: Serial interface start and stop conditions

4.4.4.1. Detailed TS timing formulas (Parallel Mode)

Symbol	Parameter	Formula	Unit
$f_{usefull\ bit\text{-}rate}$ [1)]	Useful Bit-Rate		Mbit/s
$f_{clk,\ mclk}$	MCLK Clock Frequency	1/8 * $f_{usefull\ bit\text{-}rate}$	MHz
$t_{clk,\ mclk}$	MCLK Clock Period	$1/f_{clk,\ mclk}$	ns
$t_{clk\ low,\ mclk}$	MCLK Clock Period Low Time	$t_{clk,\ mclk}/2$	ns
$t_{clk\ high,\ mclk}$	MCLK Clock Period High Time	$t_{clk,\ mclk}/2$	ns
$t_{s,\ mval}$	MVAL Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ mval}$	MVAL Hold Time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{s,\ mstrt}$	MSTRT Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ mstrt}$	MSTRT Hold Time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{s,\ merr}$	MERR Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ merr}$	MERR Hold Time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{s,\ md\_[7:0]}$	MD_[7:0] Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ md\_[7:0]}$	MD_[7:0] hold time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
1) The useful bit-rate is guard interval, constellation, code rate and channel bandwidth dependent. See also ETS EN 300 744			

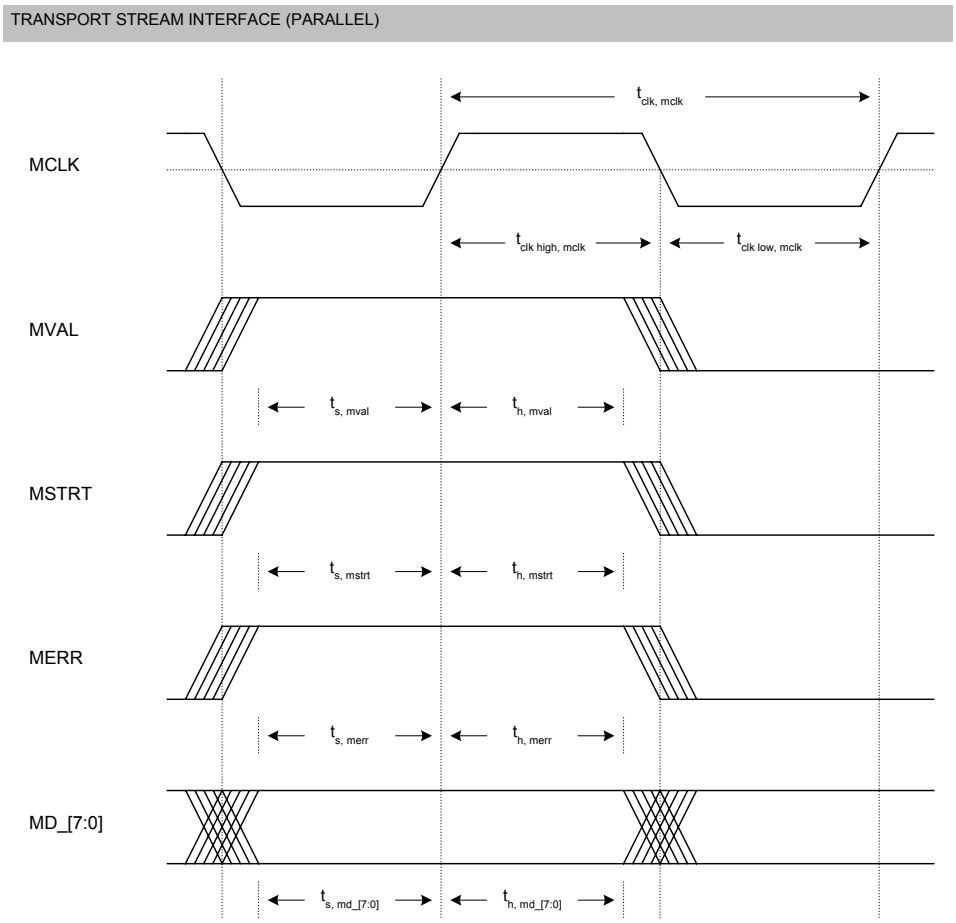


Fig. 4–2: Detailed TS timing (parallel mode)

Table 4–3: Detailed TS Timing (Parallel Mode)

Symbol	Pin Name	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
$f_{usefull\ bit\text{-}rate}$ [1)]		–	–	31.67	Mbit/s	guard interval 1/32, constellation 64-QAM, code rate 7/8, channel bandwidth 8 MHz
$f_{clk,\ mclk}$	MCLK	–	1/8 * $f_{usefull\ bit\text{-}rate}$	–	MHz	
$t_{clk,\ mclk}$	MCLK	–	$1/f_{clk,\ mclk}$	–	ns	10 pF load
$t_{clk\ low,\ mclk}$	MCLK	–	$t_{clk,\ mclk}/2$	–	ns	
$t_{clk\ high,\ mclk}$	MCLK	–	$t_{clk,\ mclk}/2$	–	ns	
$t_{s,\ mval}$	MVAL	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ mval}$	MVAL	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{s,\ mstrt}$	MSTRT	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ mstrt}$	MSTRT	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{s,\ merr}$	MERR	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ merr}$	MERR	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{s,\ md\_[7:0]}$	MD_[7:0]	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ md\_[7:0]}$	MD_[7:0]	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load

[1)] The useful bit-rate is guard interval, constellation, code rate and channel bandwidth dependent.
See also ETS EN 300 744

4.4.4.2. Detailed TS timing formulas (Serial Mode)

Symbol	Parameter	Formula	Unit
$f_{usefull\ bit\text{-}rate}$ [1)]	Useful Bit-Rate	–	Mbit/s
$f_{clk,\ mclk}$	MCLK Clock Frequency	8/8 * $f_{usefull\ bit\text{-}rate}$	MHz
$t_{clk,\ mclk}$	MCLK Clock Period	$1/f_{clk,\ mclk}$	ns
$t_{clk\ low,\ mclk}$	MCLK Clock Period low time	$t_{clk,\ mclk}/2$	ns
$t_{clk\ high,\ mclk}$	MCLK Clock Period high time	$t_{clk,\ mclk}/2$	ns
$t_{s,\ mval}$	MVAL Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ mval}$	MVAL Hold Time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{s,\ mstrt}$	MSTRT Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ mstrt}$	MSTRT Hold Time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{s,\ merr}$	MERR Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ merr}$	MERR Hold Time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{s,\ md\_[7:0]}$	MD_[0] Setup Time before active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns
$t_{h,\ md\_[7:0]}$	MD_[0] Hold Time after active MCLK edge	$t_{clk,\ mclk}/2 - x$	ns

1) The useful bit-rate is guard interval, constellation, code rate and channel bandwidth dependent.
See also ETS EN 300 744

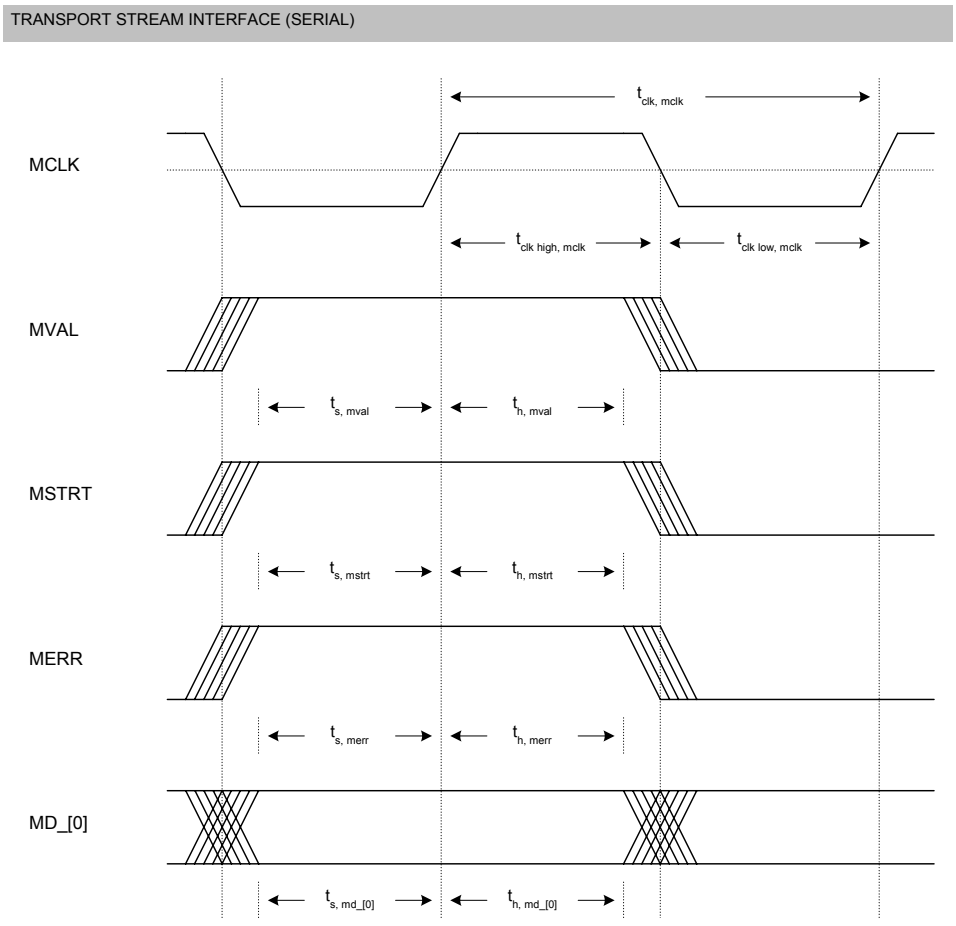


Fig. 4–3: Detailed TS timing (serial mode)

4.4.4.3. Detailed TS timing (Serial Mode)

Symbol	Pin Name	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
$f_{usefull\ bit\text{-}rate}$ [1)]		–	–	31.67	Mbit/s	guard interval 1/32, constellation 64-QAM, code rate 7/8, channel bandwidth 8 MHz
$f_{clk,\ mclk}$	MCLK	–	8/8 * $f_{usefull\ bit\text{-}rate}$	–	MHz	
$t_{clk,\ mclk}$	MCLK	–	$1/f_{clk,\ mclk}$	–	ns	10 pF load
$t_{clk\ low,\ mclk}$	MCLK	–	$t_{clk,\ mclk}/2$	–	ns	
$t_{clk\ high,\ mclk}$	MCLK	–	$t_{clk,\ mclk}/2$	–	ns	
$t_{s,\ mval}$	MVAL	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ mval}$	MVAL	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{s,\ mstrt}$	MSTRT	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ mstrt}$	MSTRT	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{s,\ merr}$	MERR	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ merr}$	MERR	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{s,\ md\_[7:0]}$	MD_[0]	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load
$t_{h,\ md\_[7:0]}$	MD_[0]	$t_{clk,\ mclk}/2 - 4$			ns	10 pF load

[1)] The useful bit-rate is guard interval, constellation, code rate and channel bandwidth dependent. See also ETS EN 300 744

4.4.4.4. AGC Interface

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$V_{IF,\ AGC}$	IF AGC range	AGC1	0	–	5.4	V	
$V_{RF,\ AGC}$	RF AGC range	AGC2	0	–	5.4	V	

5. Data Sheet History

1. Preliminary Data Sheet: “DRX 3975D Fourth-Generation COFDM”, Aug. 22, 2005, 6251-659-1PD. First release of the preliminary data sheet.

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