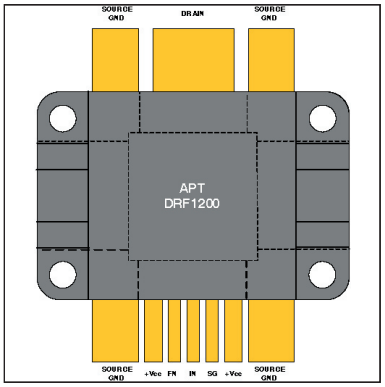
ADVANCED POWER TECHNOLOGY®

15V, 13A, 30MHz

MOSFET Driver Hybrid

The DRF1200 MOSFET driver hybrid. This hybrid includes a high power gate driver and the power MOSFET. It was designed to provide the system designer increased flexibility and lowered cost over a non-integrated solution.



DRIVER FEATURES

- Switching Frequency: DC TO 30MHz
- Low Pulse Width Distortion
- Single Power Supply
- 3V CMOS Schmitt Trigger Input 1V Hysteresis
- Drivers ⩾ 3nF

MOSFET FEATURES

- Switching Frequency: DC TO 30MHz
- Switching Speed 3-4ns
- B_{Vds} = 1kV
- I_{ds} = 13A avg.
- $R_{ds(on)} \leq$ 1 Ohm
- P_D = 350W

TYPICAL APPLICATIONS

- Class C, D and E RF Generators
- Switch Mode Power Amplifiers
- Pulse Generators
- Ultrasound Transducer Drivers
- Acoustic Optical Modulators

Driver Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply Voltage	18	V
V_{IN}	Input Single Voltage	5.5	

Driver Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	8		18	V
V_{IN}	Input Voltage		3		
$V_{IN(R)}$ [6]	Input Voltage Rising Edge	1.8		2.2	ns
$V_{IN(F)}$ [6]	Input Voltage Falling Edge	0.8		1.2	
I_{DDQ}	Quiescent Current		200		µA
I_O	Max Output Current		8.5		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance		3		
V_{IL}	Input Low	0.8		1.0	V
V_{IH}	Input High	1.9		2.2	
T_{DLY}	Time Delay (throughput)		38		ns

Driver Specifications T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typical RL	Typical CL	Max	Unit
t_r	Rise Time [2,3]	$15V_{DD}$		3.1	7.5		ns
t_f	Fall Time [2,3]	$15V_{DD}$		2.8	7.5		
T_D	Prop. Delay [2,4]	15V		33	38		
	Symmetry [1]	$15V_{DD}$ [3]		1.2			%

050-4913 Rev A 2-2006

MOSFET Absolute Maxumum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DSS}	Drain-Source Voltage		1000		V
I_D	Continuos Drain Current T_{HS} = 25°C		13		A
$R_{DS(on)}$	Drain-Source On State Resistance		0.90		Ω

Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
C_{iss}	Input Capacitance		2000		pF
C_{oss}	Output Resistance		165		
C_{rss}	Reverse Transfer Capacitance		75		

Thermal Characteristics

Symbol	Characteristic	Ratings	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance	0.13	°C/W
T_J	Operating and Storage Junction Temperature	175	°C
P_D	Maximum Power Dissipation	>100	W
P_{DC}	Total Power Dissipation @ T_C = 25°C	1050	

Test curcuit show on page 3.
All measurements were made with the Anti-Ring circuit activated unless noted.

① Symmetry is the percent difference in high and low FWHM times with a 50% duty cycle square wave input.
② R_L = 50Ω, C_L = 3000pF
③ 10% - 90% See Test Circuit
④ 50% - 50%, see Test Circuit
⑤ V_{DD} = 18V, C_L = 3000pF, F = 10MHz
⑥ Performance specified with this input.

APT reserves the right to change, without notice, the specifications and information contained herein.

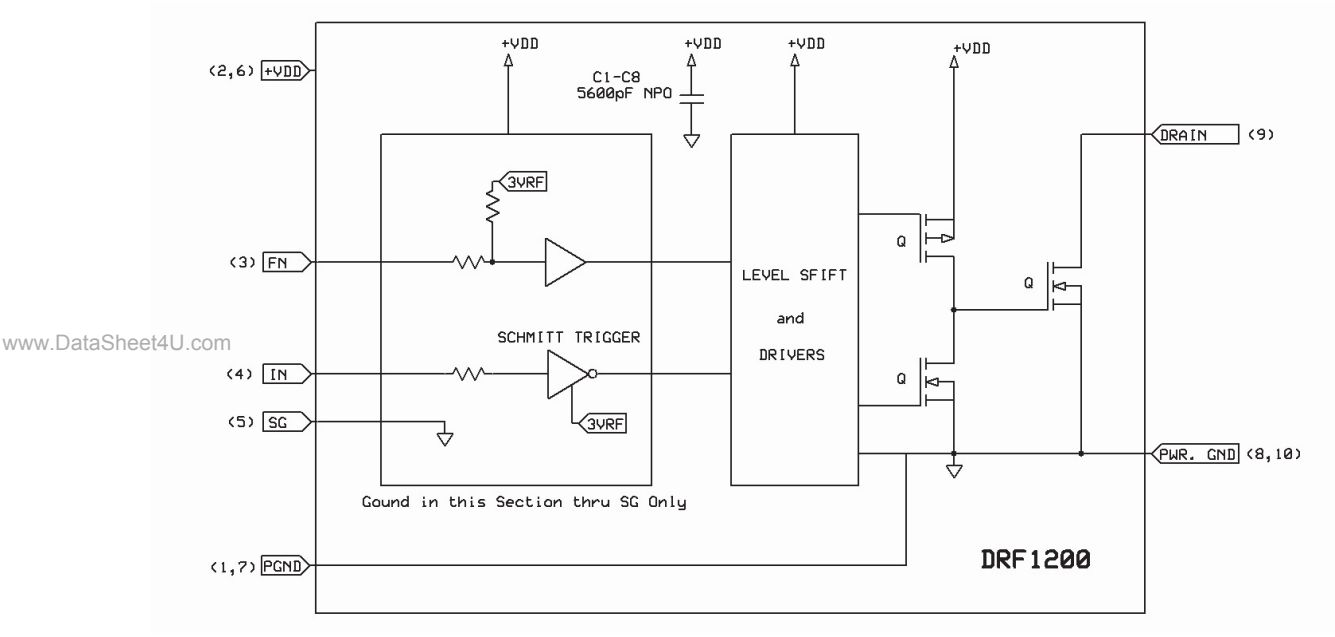


Figure 1, DRF1200 Simplified Ciruit Diagram

A Simplified DRF1200 Circuit Diagram is illustrated above. By including the driver high speed by-pass capacitors (C1-C8), their contribution to the internal parasitic loop inductance of the driver output is greatly reduced. This, coupled with the tight geometry of the hybrid, allows optimal the gate drive to the MOSFET. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground and the Anti-Ring Function, Provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency applications. The IN pin is the input for the control signal and is applied to a Schmitt Trigger. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. The P channel and N channel power drivers provide the high current to the gate of the MOSFET and the MOSFET drain is attached to the OUT pin (9).

Driver Control Logic

In (4) HIGH Driver	Driver Output LOW	MOSFET OFF Drain (9) HIGH
In (4) LOW Driver	Driver Output HIGH	MOSFET ON Drain (9) LOW

The FUNCTION, FN, pin (3) is used to disable the Anti-Ring function. It is recommended that the device be operated with this function enabled. Func. = Hi (+5V or Float) Anti-Ring on, Func. = Low (0V or GND.) Anti-ring off.
On the Output side are the POWER GROUND connections pin 8 and pin 10. The DRAIN connection is pin 9. It is suggested that output currents be restricted to these pins by design.

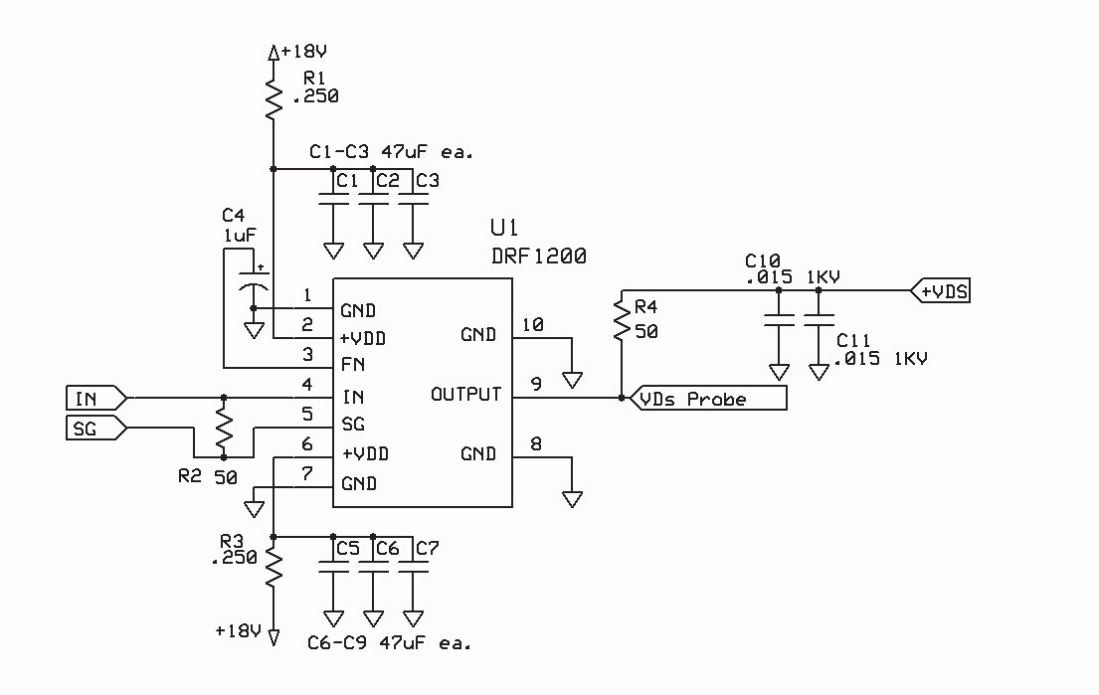


Figure 2, Test Circuit

The Test Circuit illustrated above was used to evaluate the DRF1200 (available as an evaluation Board DRF1200 EVAL). The input control signal is applied to the DRF1200 via IN(4) and SG(5) pins using RG188. This provides excellent noise immunity and control of the signal ground currents.

The FN pin is very sensitive and unwanted signals can cause erratic behavior, Therefore FN pin is heavily by-passed on the Evaluation board, see FN (3) above.

The +VDD inputs (2,6) are By-Passed (C1-C3, C5-C7), this is in addition to the internal bypassing mentioned previously. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load.
A 50Ω (R4) load is used evaluate the output performance of the DRF1200.

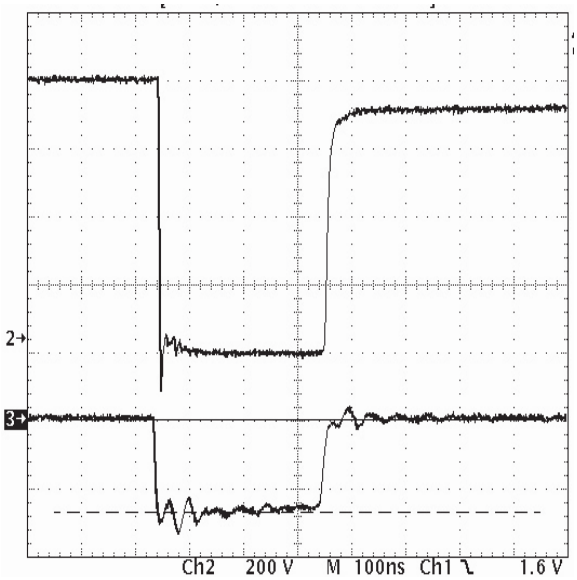


Figure 3, Drain & Current Waveforms

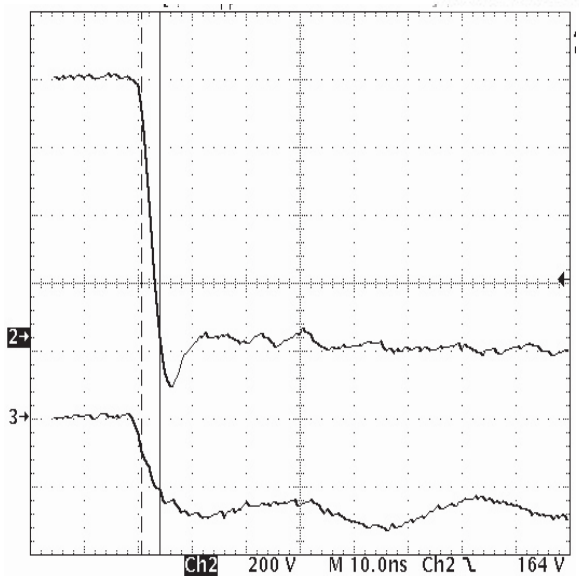


Figure 4, Drain Fall Time

In Figure 3 we see a drain voltage fall of 800V and the current rise of 13.6A in a 50Ω Load. The drain voltage fall time is 3.4ns 10% to 90% as shown in Figure 4.

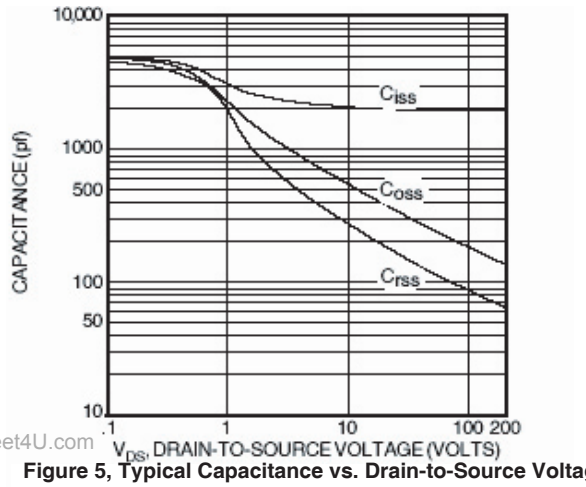


Figure 5, Typical Capacitance vs. Drain-to-Source Voltage

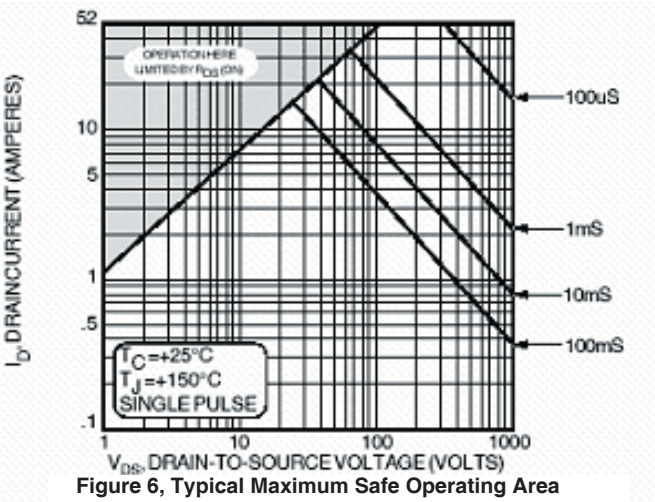


Figure 6, Typical Maximum Safe Operating Area

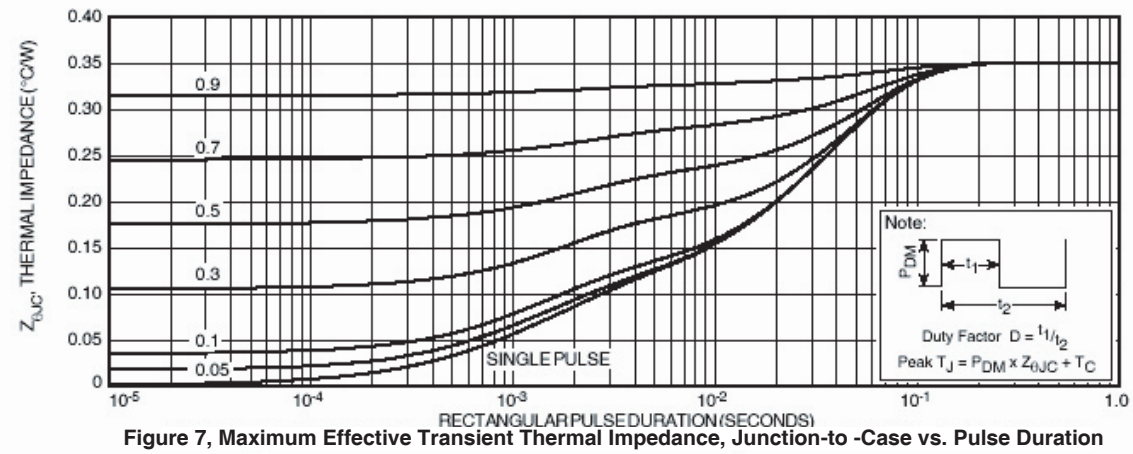


Figure 7, Maximum Effective Transient Thermal Impedance, Junction-to -Case vs. Pulse Duration

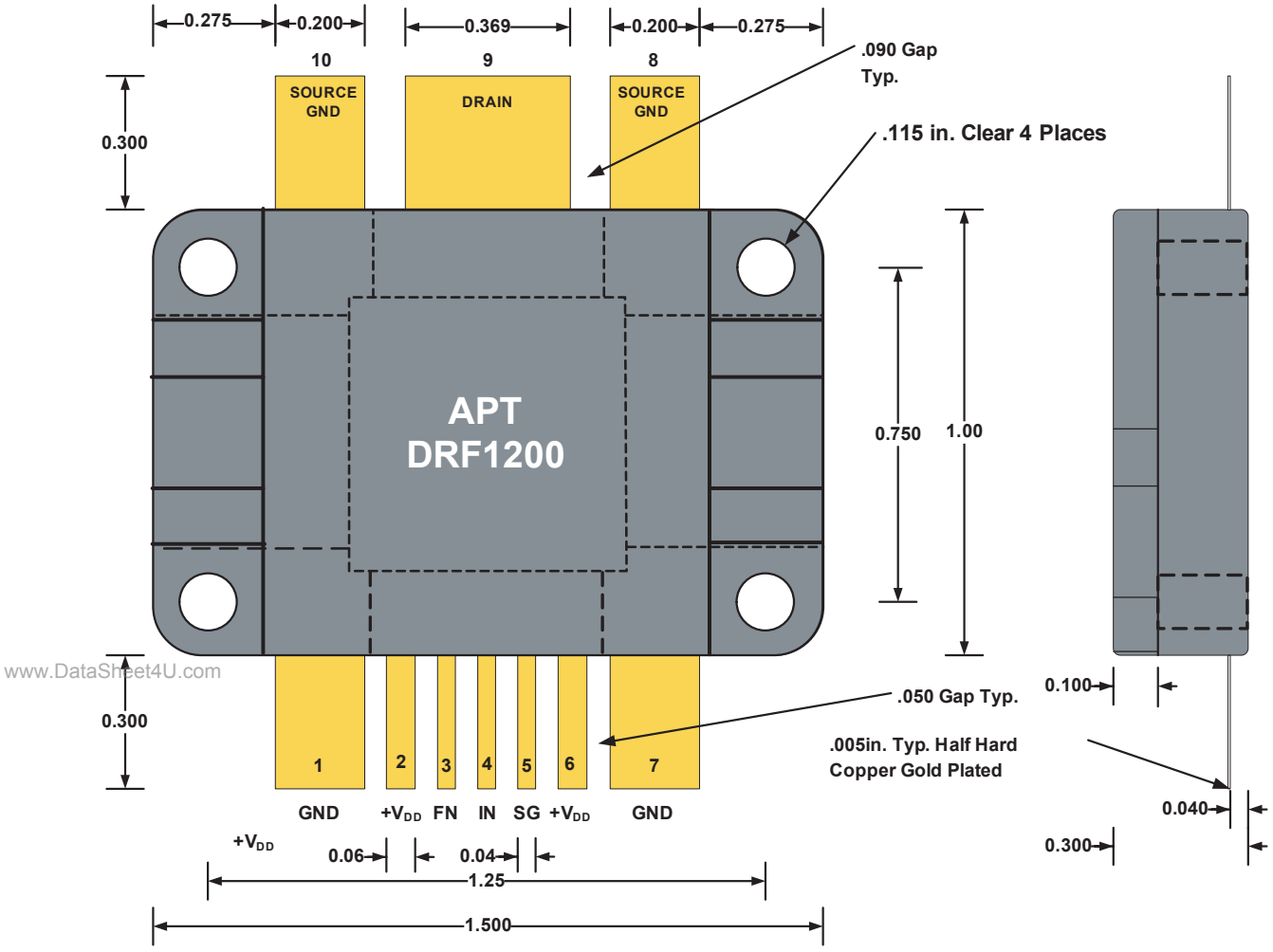


Figure 8, DRF1200 Mechanical Outline

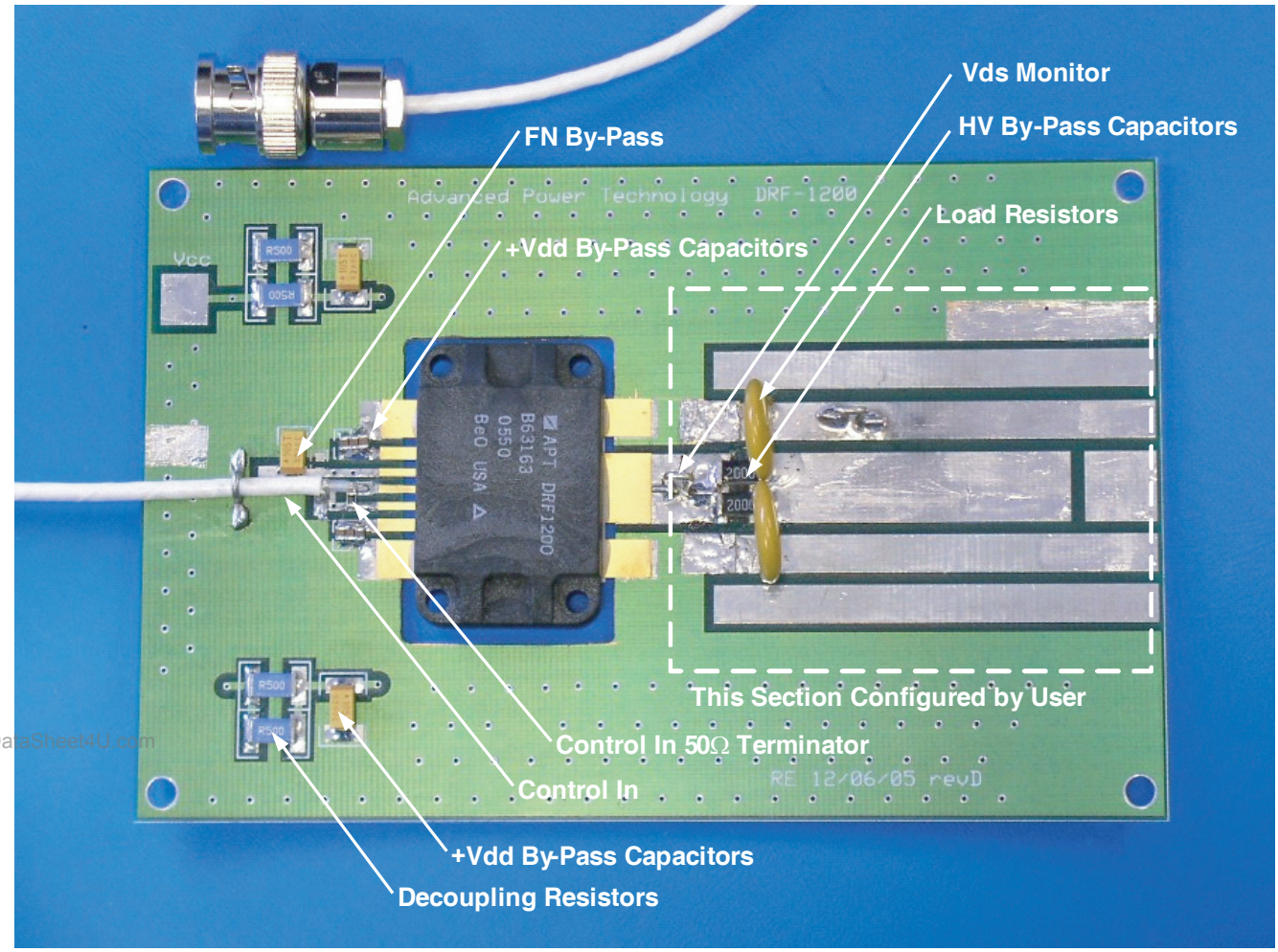


Figure 9, DRF1200 Eval Board

The DFR1200 is a high power device and must have adequate cooling for full power operation

Evaluation Boards are provided to facilitate the circuit design process by allowing the end user to quickly evaluate the performance of our components under a specific and single set of conditions. They are not intended to be used as a sub assembly in any final product(s). Care has been taken to insure that the Evaluation Boards are assembled to correctly represent the test circuit included in the component data sheet. There is no warranty of these Evaluation Boards beyond workmanship and materials.

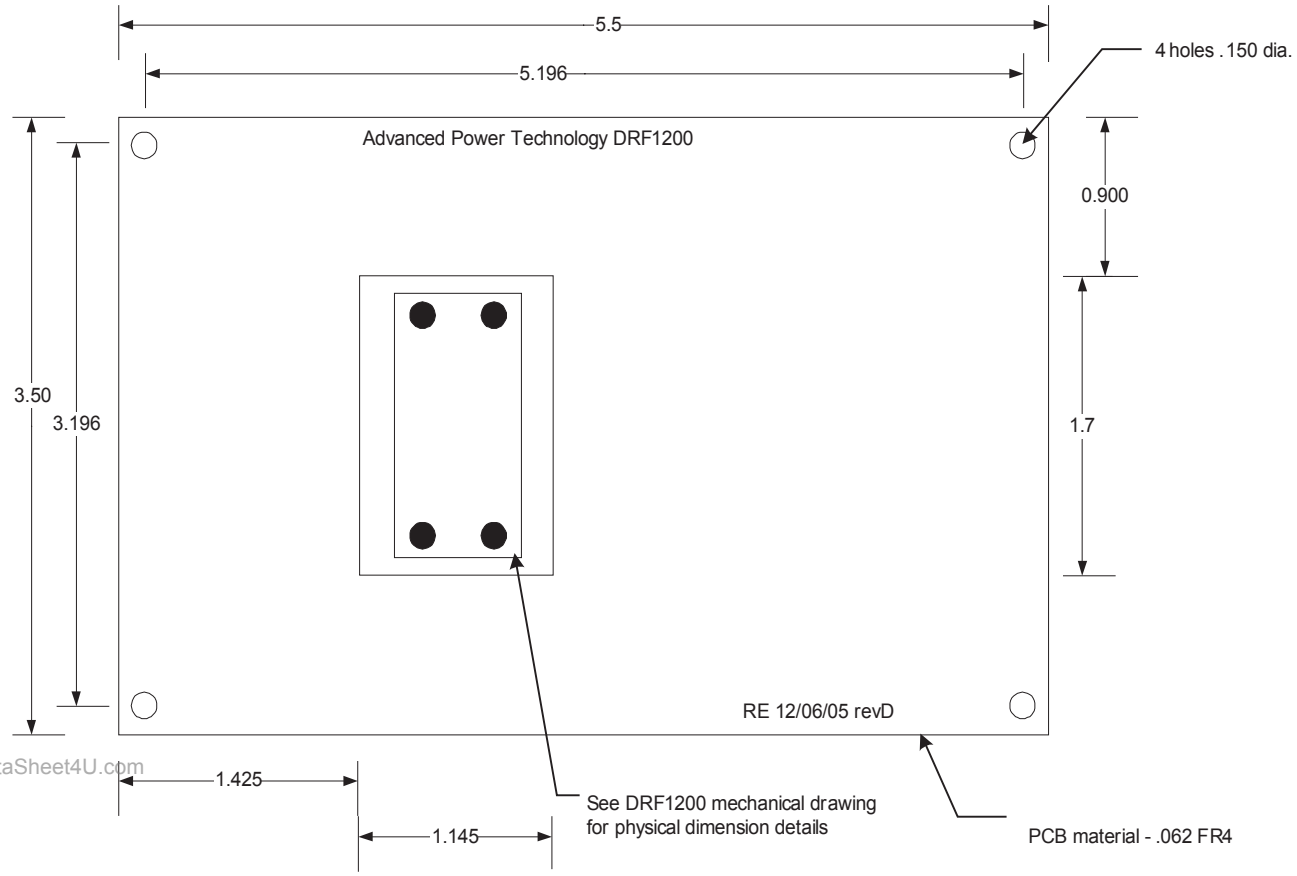


Figure 10, DRF1200 Eval Board Mechanical

Mounting instructions for Flangeless Packages

Heat sink mounting of any device in the Flangeless Package family follows the same process details outlined in this document.

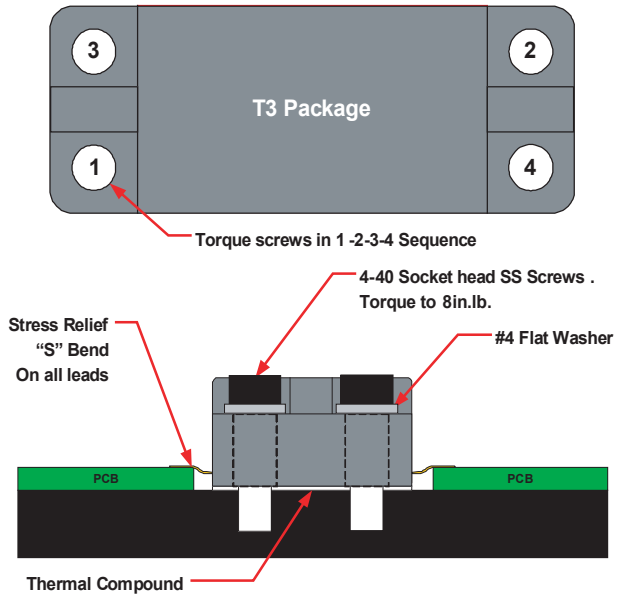


Figure 11, Top and Side View of a T3 device

Heat Sink Surface:

1. The heat sink surface should be smooth, free of nicks and burs; in addition it should be flat to ≤.001in./in TIR, (Total Indicator Run out) and be finished to ~ 68µ CLA, (Center Line Average).
2. Must be free of solder balls, metal shavings and any foreign objects or material.

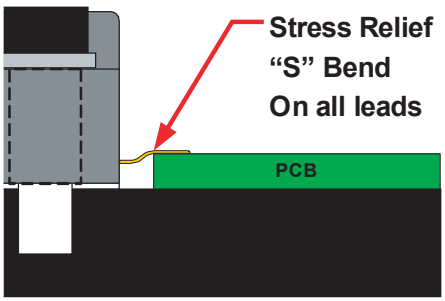


Figure 12, Stress Relief bend

Device Preparation:

1. The leads should be prepared with an "s" bend, as shown in Figure 10 prior to mounting on the heat sink
2. The BeO surface of the device must be free of any foreign objects or material.
3. The BeO surface must be coated with a thin and uniform film of thermal compound.
4. For commercial manufacturing the suggested method for thermal compound application is to apply the compound using a screen printer. This process insures consistent and repeatable performance with minimum effort.

Mechanical Attachment:

1. The four screws (1-2-3-4), as shown in Figure 11, should be installed and seated, then torqued to one-half the specification, in the sequence shown. First screw 1 then screw 2, 3 and 4.
2. Then complete the process by tightening to the full specification in the same manner.
3. The torque spec is 8in.lb. ±1lb. (0.9Nm)

Lead Attachment:

1. The leads may now be soldered to the PCB
2. Maximum lead temperature must not exceed 300°C for 10s.
3. For lead free use 96.5 % tin, 3% silver, and 0.5% copper.
4. Non-lead Free use 2% Silver, 62% Tin, 36% lead (sn62).