Non-isolated Quasi-Resonant Buck LED Power Switch with OVP

FEATURES

- **Proprietary Output OVP Protection**
- **Integrated with 500V MOSFET**
- **No Auxiliary Winding Needed**
- **Quasi-Resonant for High Efficiency**
- **Built-in Thermal Foldback**
- **Built-in Charging Circuit for Fast Start-Up**
- **±4% CC Regulation**
- **Very Low VDD Operation Current**
- **Built-in AC Line CC Compensation**
- **Build in Protections:**
  - **LED Short/Open Protection**
  - **On-Chip Thermal Fold-back (OTP)**
  - **Cycle-by-Cycle Current Limiting**
  - **Leading Edge Blanking (LEB)**
  - **Pin Floating Protection**
  - **VDD UVLO**
- **Available with SOP8 Package**

APPLICATIONS

- **LED Lighting**

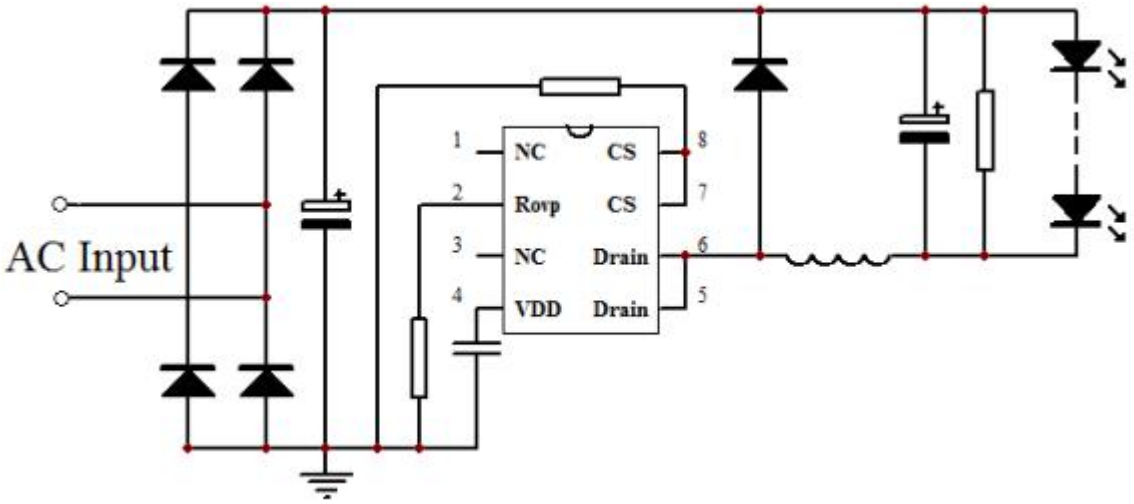
GENERAL DESCRIPTION

DP9130 is a highly integrated power switch with Quasi-Resonant Buck (QR-Buck) constant current (CC) control for LED lighting applications. The IC has built in output Over Voltage Protection (OVP).

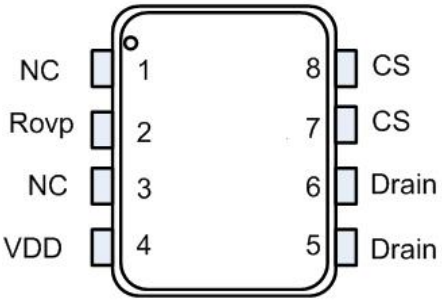
DP9130 combines a 500V power MOSFET switch with a power controller in one chip. The IC also integrates high voltage startup/IC supply circuit and a novel transformer demagnetization circuit, which eliminates transformer auxiliary winding. The IC adopts Quasi-Resonant control for high efficiency.

DP9130 integrates functions and protections of Current Limit and Leading Edge Blanking, Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Thermal Foldback (OTP), Output OVP, LED Open/Short Protection, etc.

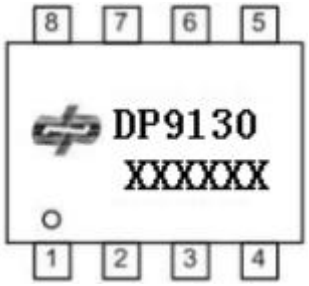
TYPICAL APPLICATION CIRCUIT



Pin Configuration



Marking Information



DP9130 for product name;

XXXXXX : The first X reresents the last year,2014 is 4; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said; The last two X represents the wafer batch code.

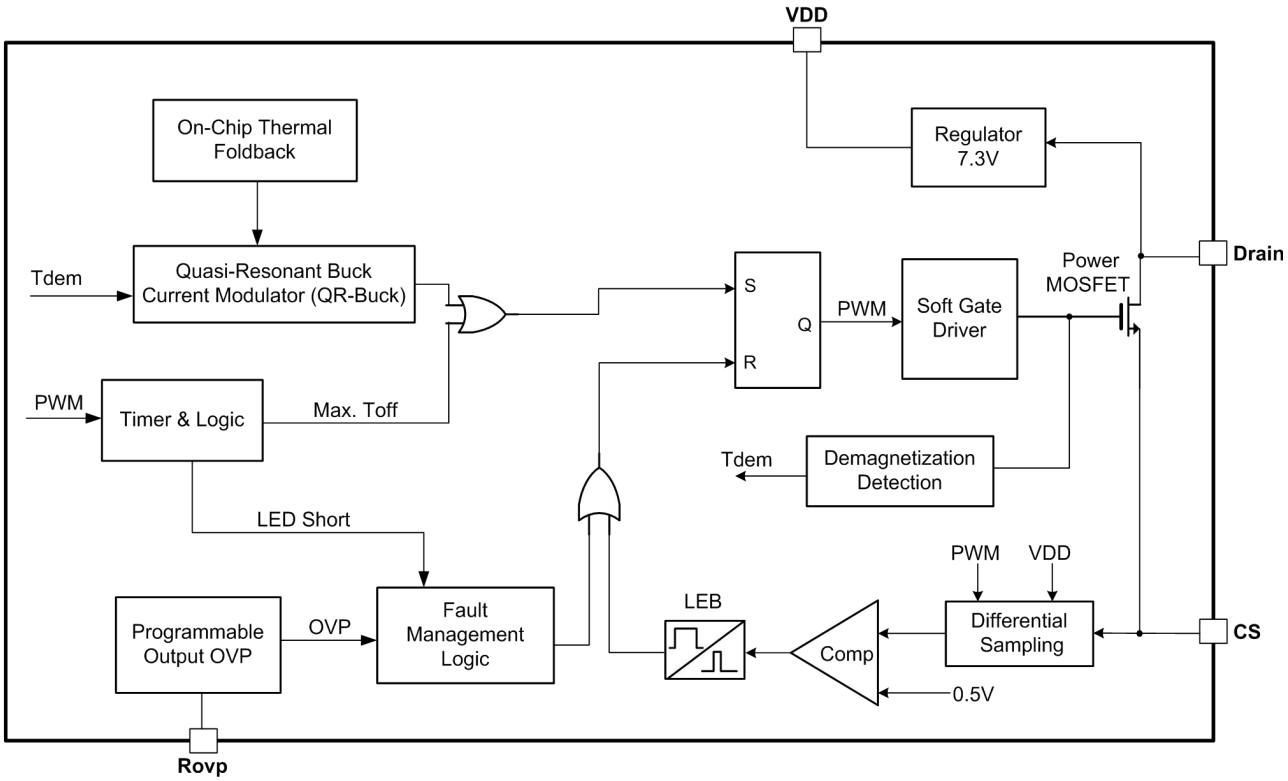
Output Power Table

Part Number	Package	Output Current for 90-265Vac		Output Current for 176-265Vac		Minimum Output Voltage
		36V output	72V output	150V output	200V output	
DP9130	SOP8	180 mA	150 mA	120 mA	100 mA	15V

Pin Description

Pin Number	Pin Name	I/O	Description
1	NC	-	No Connection.
2	Rovp	I	Over Voltage Protection Setting Pin. Connect a Resistor to System GND.
3	NC	-	No Connection.
4	VDD	P	Power Supply Pin of the Chip.
5-6	Drain	I	Internal Power MOSFET Drain.
7-8	CS	P	The Ground of the IC. This pin is also used for peak current control.

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	8.5	V
Drain pin	-0.3 to 500	V
Rovp pin	-0.3 to 8.5	V
Package Thermal Resistance (SOP8)	165	℃/W
Maximum Junction Temperature	175	℃
Operating Temperature Range	-40 to 105	℃
Storage Temperature Range	-65 to 150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	℃

Electrical Characteristics (Ta = 25℃, If Not Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_ST}	Startup Current	VDD=6.5V		700		uA
I_{VDD_Op}	Operation Current			140	260	uA
V_{DD_Op}	VDD Operation Voltage		6.8	7.3	7.8	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			5.3		V
Timing Section						
Ton_max	Maximum On Time			32		us
T_{off_min}	Minimum OFF Time			2.5		us
T_{off_max}	Maximum OFF Time			300		us
T_{dem_OVP}	Off Time OVP Trigger Threshold			5		us

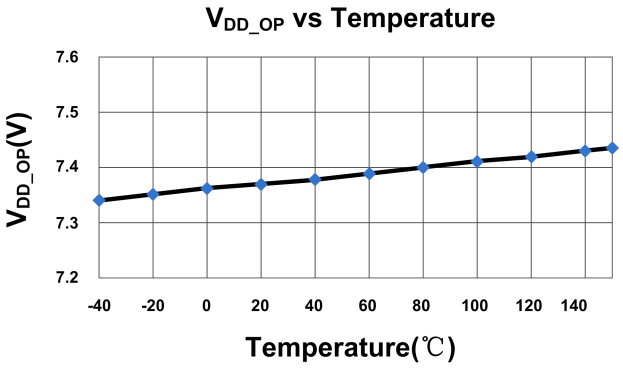
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV
T_{D_OCP}	Over Current Detection and Control Delay			100		ns
Output OVP Section (Rovp Pin)						
V_{ROVP}	Rovp Pin Floating Voltage			5.7		V
Over Temperature Protection						
T_{SD}	Thermal Foldback Trigger Point	(Note 3)		165		℃
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		500			V
R_{dson}	Static Drain-Source On Resistance	I(Drain)=50mA		12		ohm

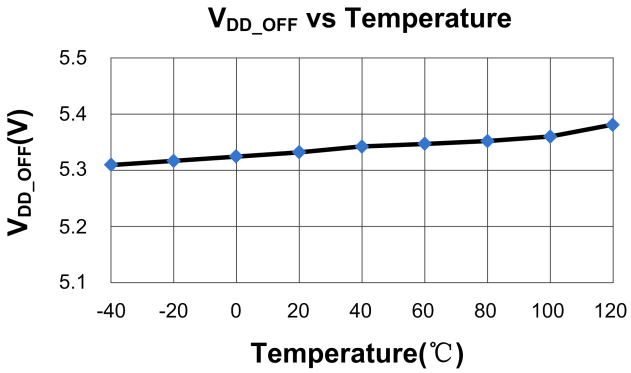
Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

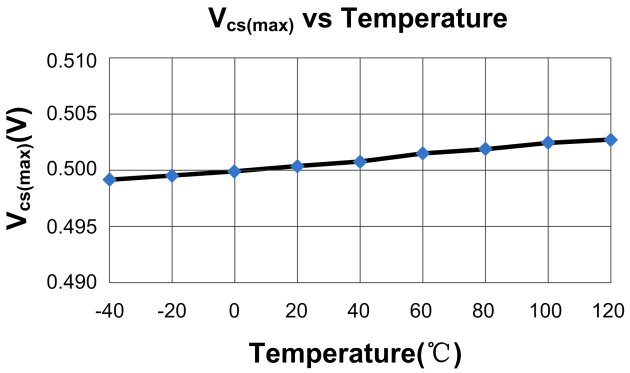
Note2. The device is not guaranteed to function outside its operating conditions.

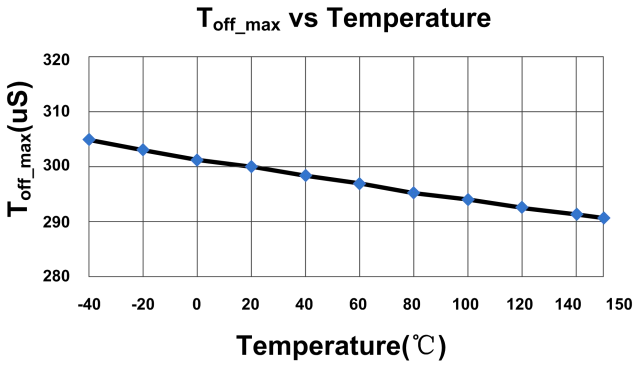
Note3. Guaranteed by design.

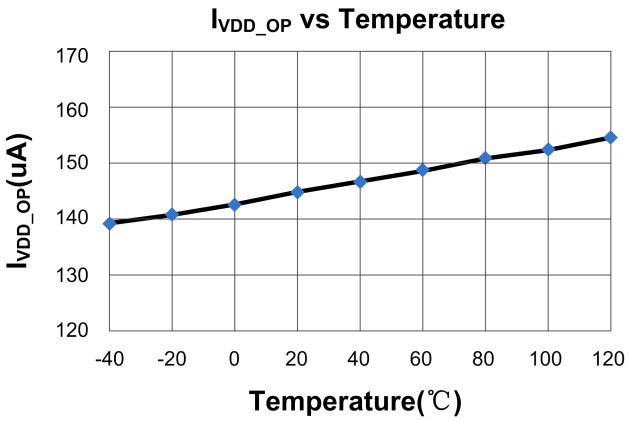
Characterization Plots











Operation Description

DP9130 combines a high voltage power MOSFET switch with a power controller in one chip. The built-in high precision CC control with high level protection features makes it suitable for LED lighting applications.

- **7.3V Regulator**

In DP9130, the 7.3V regulator charges VDD hold-up capacitor to 7.3V by drawing a current from the voltage on the Drain pin, whenever the internal power MOSFET is off. When the power MOSFET is on, the charging device runs off of the energy stored in the VDD hold-up capacitor. Extremely low IC power consumption allows DP9130 to operate continuously from the current drawn from the Drain pin. A capacitor value about 1uF is sufficient for both high frequency decoupling and energy storage.

- **Very Low Operation Current**

The operating current in DP9130 is as small as 140uA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

- **Demagnetization Detection without Auxiliary Winding**

In DP9130, the transformer core demagnetization is detected by monitoring the coupling current flowing through the parasitic capacitor Crss between the drain and gate of power MOSFET. When the transformer is fully demagnetized, the Drain voltage evolution is governed by the resonating energy transfer between the transformer inductor and the global capacitance present on the Drain. These voltage oscillations create current oscillation in the parasitic capacitor Crss. A negative current takes place during the decreasing part of the Drain oscillation, and a positive current during the increasing part. The transformer demagnetization time corresponds to the inversion of the current by detecting this point, as shown in Fig.1

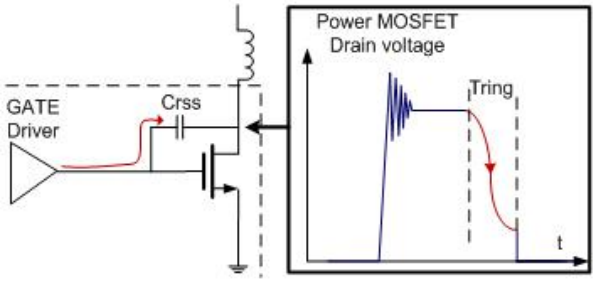


Fig.1

- **Quasi Resonant Buck (QR-Buck) Constant Current Control**

In QR-Buck mode, the IC keeps CS peak current constant and starts new PWM cycle with valley switching. Therefore, high precision CC and high conversion efficiency can be achieved simultaneously. The average LED regulation output current is given by:

$$I_{Buck\_CC\_OUT}(mA) \cong \frac{1}{2} \times \frac{500mV}{Rcs(\Omega)}$$

In the equation above,

Rcs--- the sensing resistor connected between the CS pin to Buck system GND.

- **Minimum and Maximum OFF Time**

In DP9130, a minimum OFF time (typically 2us) is implemented to suppress ringing when the power MOSFET is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance. The maximum OFF time in DP9130 is typically 250us.

- **Programmable Output Over Voltage Protection (OVP)**

In DP9130, the over voltage protection can be

programmed by connecting a resistor between Rovp in and **system GND**. When the LED is open circuit, the output voltage increases gradually, and the demagnetization time gets shorter. The OVP voltage can be calculated by:

$$V_{OVP}(V) \cong \frac{I_{PK} \times L}{T_{DEM\_OVP}}$$
$$= \frac{500mV \times L}{Rcs(\Omega) \times 14.4us} \times \left(1 + \frac{160K}{R_{OVP}(\Omega)}\right)$$

In the equation above,

L--- Inductance of Buck Inductor.

T_{DEM_OVP} ----demagnetization time when OVP is triggered.

I_{PK} ----peak current of inductor.

- **Auto-Restart and LED Open Loop Protection**

In the event of LED output OVP occurs, the IC enters into auto-restart and VDD oscillation mode begins, wherein the power MOSFET is disabled. In VDD oscillation mode, the VDD hold-up capacitor voltage will periodically ramp up and down between 5.3V and 7.3V with a digital counter counting the oscillation cycle. When 32 cycles had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system will resume normal operation.

- **Current Limit and Leading Edge Blanking**

The current limit circuit samples the differential voltage between VDD and CS, as shown in “Block Diagram”. When the sampled differential voltage exceeds the internal threshold (500mV), the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

- **On Chip Thermal Fold-back (OTP)**

DP9130 integrates thermal fold-back function. When the IC temperature is over 165℃, the system output regulation current is gradually reduced, as shown in Fig.2. Thus, the output power and thermal dissipation are also reduced. In this way, the system temperature is limited and system reliability is also improved.

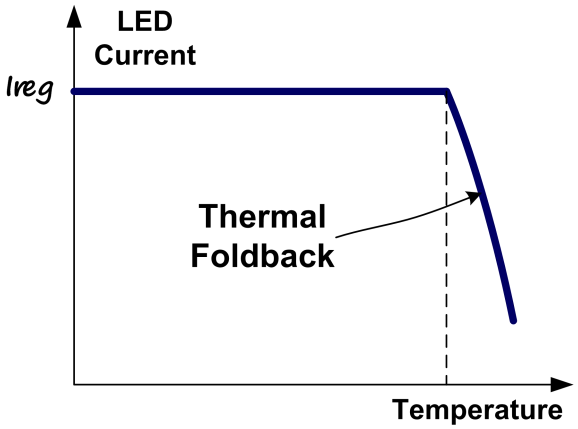


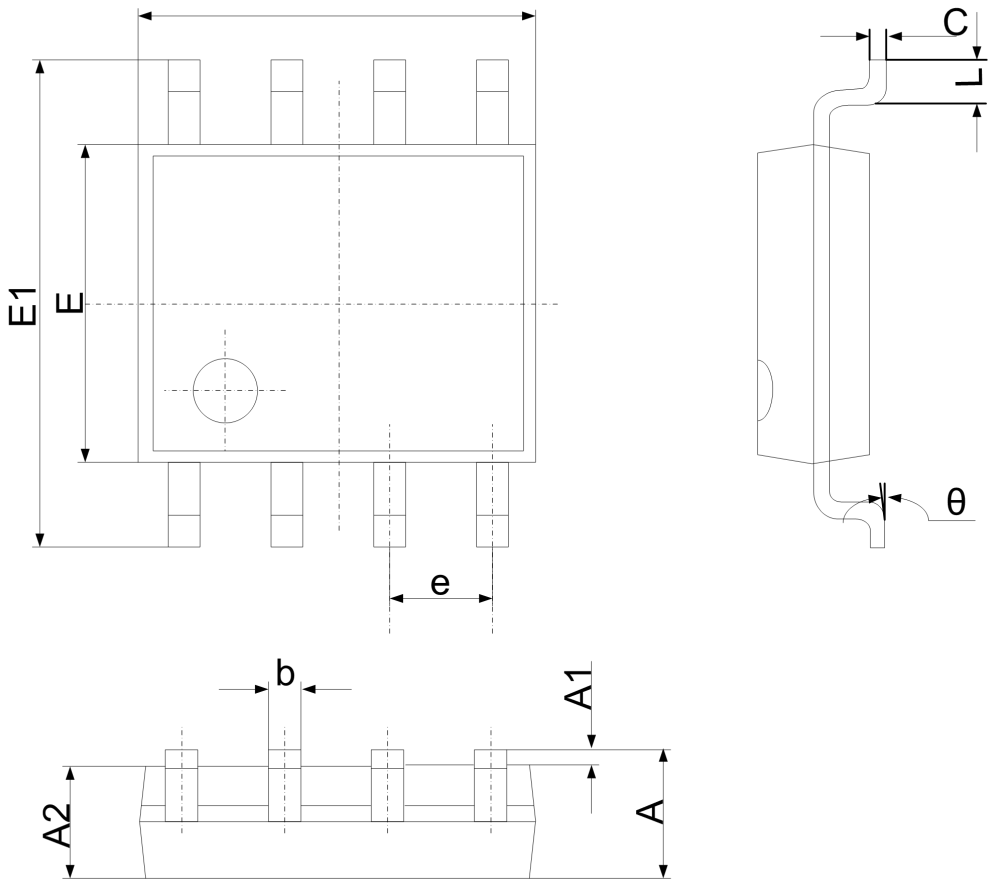
Fig.2

- **Soft Totem-Pole Gate Driver**

DP9130 has a soft totem-pole gate driver with optimized EMI performance.

Package Dimension

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°