National Semiconductor

ADVANCE INFORMATION
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DP83220
CDL™ Twisted Pair FDDI Transceiver Device

General Description

The Copper Data Link (CDL) Transceiver is an integrated circuit designed to interface directly with the National Semiconductor FDDI Chip Set or other FDDI PHY silicon, allowing low cost FDDI compatible data links over copper based media. The DP83220 Transceiver, with the proper compensation selected, will allow links of up to 100 meters over both Shielded Twisted Pair (STP) and Datagrade unshielded Twisted Pair (DTP). CDL surpasses a Bit Error Rate (BER) of $<1 \times 10^{-12}$ over both STP and DTP. The CDL is designed to meet the SDDI specification for FDDI transmission across Type 1 STP cable when used in conjunction with the appropriate transformer/filter module from Pulse Engineering.

Features

- Fully compatible with current FDDI PHY standard
- Fully compatible with the SDDI PMD specification
- Requires a single +5V supply
- Isolated TX and RX power supplies for minimum noise coupling
- Allows use of Type 1 STP and Category 5 DTP cables
- No Transmit Clock required
- Loopback feature for board diagnostics
- Link Detect input provided

Block Diagram

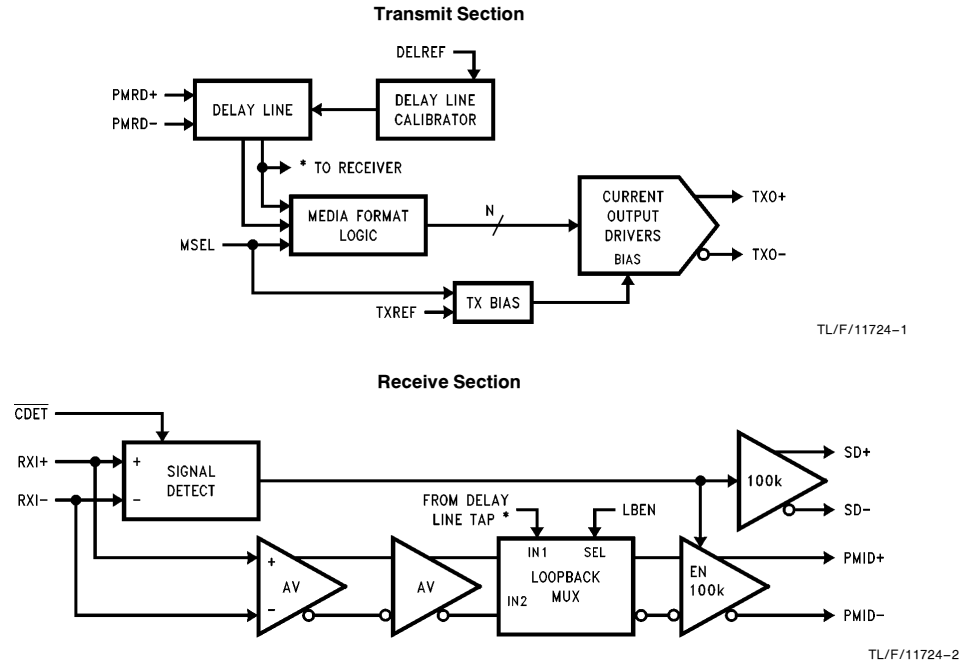


FIGURE 1. DP83220 Transceiver Block Diagram

1.0 Functional Description

The CDL Transceiver consists of nine major functional blocks as shown in *Figure 1.* The Transmit section includes the following: the Delay Line, the Delay Line Calibrator, the Media Format Logic, and the Current Output Driver circuitry with its bias circuitry. The Delay Line accepts the NRZI encoded data from the PMRD± pins and provides a short ''memory'' of the bit that preceded the bit currently being transmitted. The Delay Line Calibrator allows the use of an external resistor which governs the time calibration of the delay line. The Delay Line outputs the data via taps which are tied to the Media Format Logic. The encoding logic is dependent on the state of the Media Select pin. The encoded data is routed to the Current Output Driver, through the TXO± output pins and transformer coupled to the media.

The Receive section consists of the following: a differential input amplifier, Signal Detect circuitry, a Loopback Multiplexer, and differential 100K output drivers for data and Signal Detect. The Receive signal is input to the RXI± pins from the receive isolation transformer. The input signal is sensed by the Signal Detect circuit. The input signal also drives a differential input amplifier whose output is coupled to the Loopback Mux logic. The 'sel' input which is driven by LBEN controls which data stream, RXI± or Loopback data, is routed to the differential 100K Output Driver. When in Loopback mode, the Signal Detect output driver is forced true. When receiving data from copper media, the signal detect circuit provides valid states to the Signal Detect output driver depending on the amplitude of the incoming signal and also allows the PMID± outputs to switch. Cable Detect is the final gating function for data reception. If no media is detected, the transceiver will generate a logic low Signal Detect which will inhibit data reception by the PHY.

1.1 SDDI OPERATION

The CDL allows full compatibility with the current SDDI specification. By allowing the MSEL pin to float, which forces the pin to $V_{CC}/2$ internally, the SDDI mode of operation is selected. The appropriate transmit voltage amplitude must also be set by selecting a value of 2.6 kΩ for the TXREF resistor.

Finally, it is important to note that the CDL must be used in conjunction with the Pulse Engineering 8.3 magnetics module in order to conform to the current SDDI specification. No special terminations are required in connecting the Pulse Engineering 8.3 module to the CDL. (Refer to the typical SDDI schematic, *Figure 9.*)

2.0 Pinout Summary

Signal	Pin No.	Description	Type
V_{CC}	13, 26	V_{CC}	Supply
GND	14, 22	GND	Supply
RXV_{CC}	4, 27	Receive V_{CC}	Supply
RXGND	3, 28	Receive GND	Supply
TXV_{CC}	5, 11	Transmit V_{CC}	Supply
TXGND	7, 10	Transmit GND	Supply
$EXTV_{CC}$	23	External V_{CC}	Supply
RXI±	2, 1	Receive Data Inputs	Current In
PMID±	25, 24	Physical Media Indicate Data	ECL Out
PMRD±	15, 16	Physical Media Request Data	ECL In
TXO±	9, 8	Transmit Data Outputs	Current Out
SD±	20, 21	Signal Detect Outputs	ECL Out
TXREF	6	Transmit Amplitude Reference	Current Out
DELREF	12	Delay Line Calibration Reference	Current Out
LBEN	19	Loopback Enable	CMOS In
MSEL	17	Media Select	3-Level Select
$\overline{CDET}$	18	Cable Detect Bar	CMOS Schmitt Trigger In

3.0 Pin Definitions

V_{CC} (13,26): Positive power supply for the 100K ECL compatible circuitry. The Transceiver operates from a single +5 V_{DC} power supply.

GND (14,22): Return path for the 100K ECL compatible circuitry power supply.

RXV_{CC} (4,27): Positive power supply for the small signal receive circuitry. This power supply is intentionally separated from others to eliminate receive errors due to coupled supply noise.

RXGND (3,28): Return path for the receive power supply circuitry. This Power supply return is intentionally separated from others to eliminate receive errors due to coupled supply noise.

TXV_{CC} (5,11): Positive power supply required by the analog portion of the transmit circuitry. This power supply is intentionally separated from the others to prevent supply noise from coupling to the transmit outputs.

TXGND (7,10): Return path for the analog transmit power supply circuitry. This supply return is intentionally separated from others to prevent supply noise from being coupled to the transmit outputs.

$EXTV_{CC}$ (23): Positive power supply for receiver output circuitry.

RXI± (2,1): Balanced differential line receiver inputs. Signals meeting the input threshold for a given media type are output through PMID± as differential ECL.

PMID± (25,24): 100K ECL compatible differential outputs used as the source of the receive data for the DP83231 Clock Recover Device (CRD™).

PMRD± (15,16): Differential 100K compatible 4B5B NRZI transmit data inputs originating from the DP83251/55 Physical Layer Device (PLAYER™).

TXO± (9,8): Differential current driver outputs precompensated for twisted pair cable.

SD± (20,21): Differential 100K ECL compatible Signal Detect outputs indicating that a valid signal is present at the RXI± inputs.

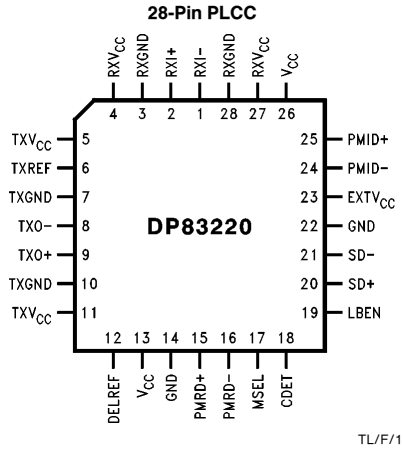
DELREF (12): A resistor is connected between this pin and GND. The value of this resistor controls the current into the delay line calibrator which, in turn controls the delay time of the delay line.

TXREF (6): A resistor is connected between this pin and TXGND. The value of this resistor controls the signal amplitude of the TXO± data which drives the twisted pair.

LBEN (19): TTL compatible CMOS Loopback Enable input pin selects the internal loopback path which effectively routes the PMRD± data to the PMID± differential outputs.

MSEL (17): The Media Select input controls the compensation and output current required to drive to 100 meters of either STP or DTP media. This is a tri-level control pin. When forced to a low voltage, STP compensation is selected. Forcing a high voltage level will select the DTP compensation mode. Forcing a median voltage allows the device to operate in the transparent mode by deasserting pre-emphasis.

$\overline{CDET}$ (18): The Cable Detect input is provided to support the option of external Cable Detection circuitry. With $\overline{CDET}$ low, the CDL transceiver functions normally. When $\overline{CDET}$ is high, the signal detect output is forced low which inhibits data reception by the PHY. The exception is in the case of Loop Back, where Signal Detect is forced high regardless.



Order Number DP83220V
See NS Package Number V28A

FIGURE 2. Pin Configuration

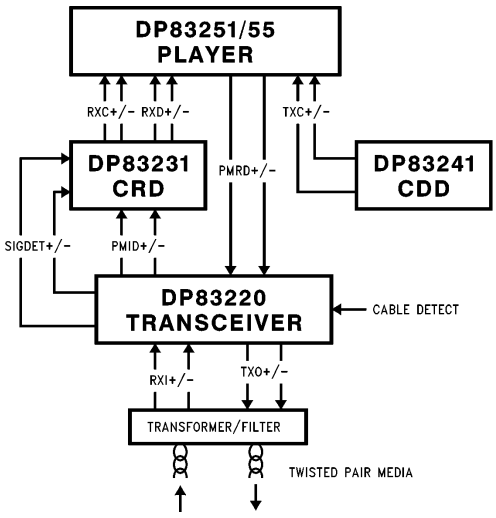


FIGURE 3. System Connection Diagram

4.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Logic Power	Referenced to GND	−0.5		6.0	V
RXV_{CC}	Received Power	Referenced to RXGND	−0.5		6.0	V
TXV_{CC}	Transmit Power	Referenced to TXGND	−0.5		6.0	V
$EXTV_{CC}$	ECL Output Power	Referenced to GND	−0.5		6.0	V
I_{ECL}	DC Output Current (High)				−50	mA
ESD				TBD		
$T_{storage}$	Storage Temperature		−65		+150	°C

4.1 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
T_A	Operating Temperature		0	25	70	°C
P_D	Power Dissipation			600		mW

4.2 DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IHt}	TTL High Level Input		2.0			V
V_{ILt}	TTL Low Level Input				0.8	V
$V_{IHschmitt}$	Schmitt High Level Input		3.7			V
$V_{ILschmitt}$	Schmitt Low Level Input				1.5	V
V_{IHmsel}	MSEL High Level Input		3.7			V
V_{ILmsel}	MSEL Low Level Input				1.5	V
V_{IMmsel}	MSEL Middle Level Input			$V_{CC}/2$		V
V_{IHe}	ECL High Level Input		$V_{CC} - 1165$		$V_{CC} - 870$	mV
V_{ILe}	ECL Low Level Input		$V_{CC} - 1830$		$V_{CC} - 1475$	mV
V_{OHe}	ECL High Level Output	Refer to *Figure 4*	$V_{CC} - 1035$		$V_{CC} - 870$	mV
V_{OLe}	ECL Low Level Output	Refer to *Figure 4*	$V_{CC} - 1830$		$V_{CC} - 1605$	mV
I_{CC1}		Refer to *Figure 4*		90		mA
I_{CCT}	Total Supply Current	Refer to *Figure 4*		145		mA
I_{TXO1}	Transmit Current 1	Transmit Current / 100Ω Z_O			20	mA
I_{TXO2}	Transmit Current 2	Transmit Current / 150Ω Z_O			15	mA
SD_{THon}	Sig Det Turn-On Threshold	Refer to *Figure 5,* Note 1	60			mV
SD_{THoff}	Sig Det Turn-Off Threshold	Refer to *Figure 5,* Note 1			15	mV

4.3 AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{TXr/f}$	TX Driver Rise and Fall	Into 25Ω in Parallel with 50 pF		1.6		ns
$t_{TXr/f}$	TX Driver Rise and Fall	Into 37.5Ω in Parallel with 50 pF		2.5		ns
t_{TXpd}	TX Propagation Delay	From PMRD± to TXO±		6		ns
t_{RXpd}	RX Propagation Delay	From RXI± to PMID±		10		ns
T_{TXskew}	TX Driver Skew			0		ps

Note 1: Subject to change.

4.0 Electrical Characteristics (Continued)

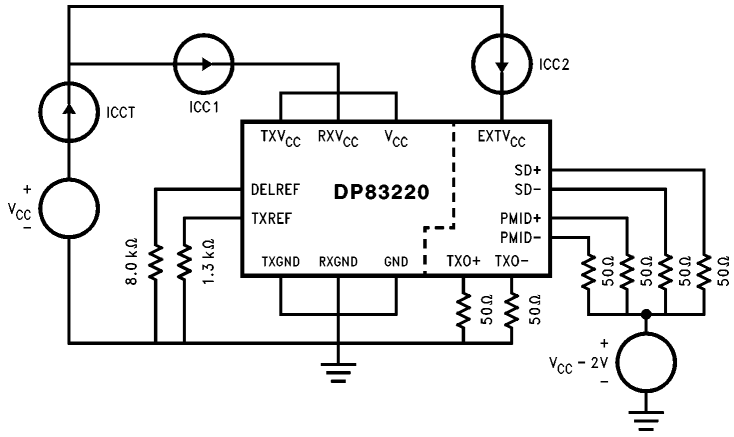


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FIGURE 4. I_{CC} Diagram

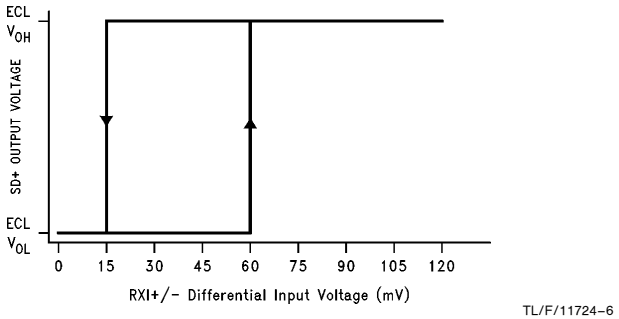

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FIGURE 5. Signal Detect Threshold

4.0 Electrical Characteristics (Continued)

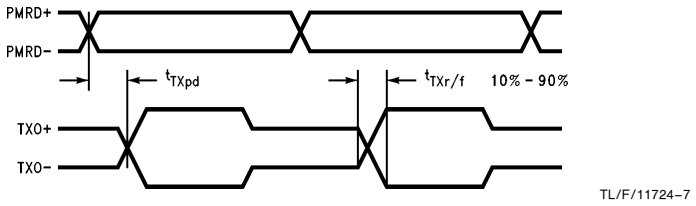

FIGURE 6. Transmit Timing

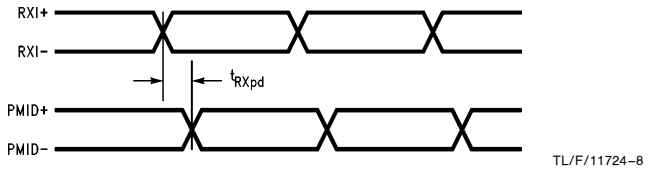

FIGURE 7. Receive Timing

4.0 Electrical Characteristics (Continued)

4.3 TRANSMIT DATA AND CURRENT DRIVER OUTPUT

TXDn	TXDn − 1	$I_{TXO}+$	$I_{TXO}-$
0	0	$(I_1)\ I_{max}$	$(I_2)\ I_{max}$
0	1	$(I_1 + I_2)\ I_{max}$	0
1	0	0	$(I_1 + I_2)\ I_{max}$
1	1	$(I_2)\ I_{max}$	$(I_1)\ I_{max}$

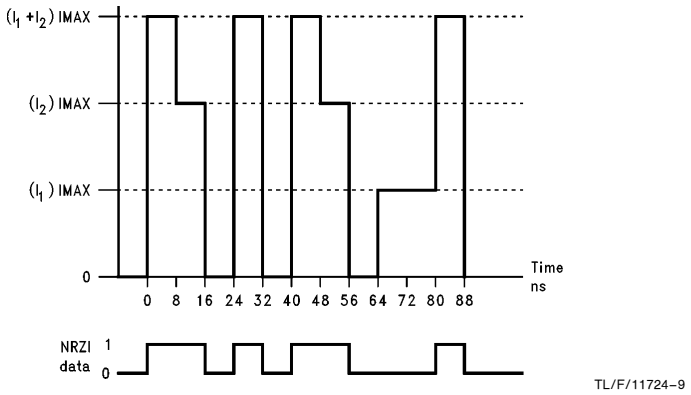

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FIGURE 8. Typical Pre-Emphasized Current Waveform, $I_{TXO}+$

TABLE I. Media Select

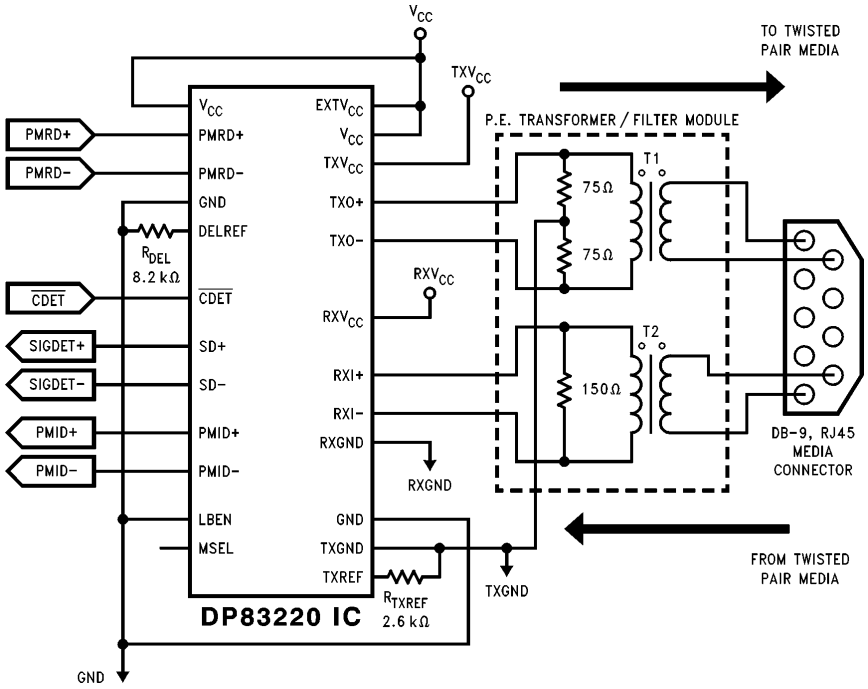
Mode	MSEL
STP	<1.5V
DTP	>3.7V
SDDI	Float

TABLE II. Data Paths and Signal Detect

LBEN	$\overline{CDET}$	Data @ PMID ±	SD +
0	1	RXI ±	0
0	0	RXI ±	1
1	1	PMRD ±	1
1	0	PMRD ±	1

Note: This table assumes that minimum signal's levels required by Signal Detect have been met.

4.0 Electrical Characteristics (Continued)



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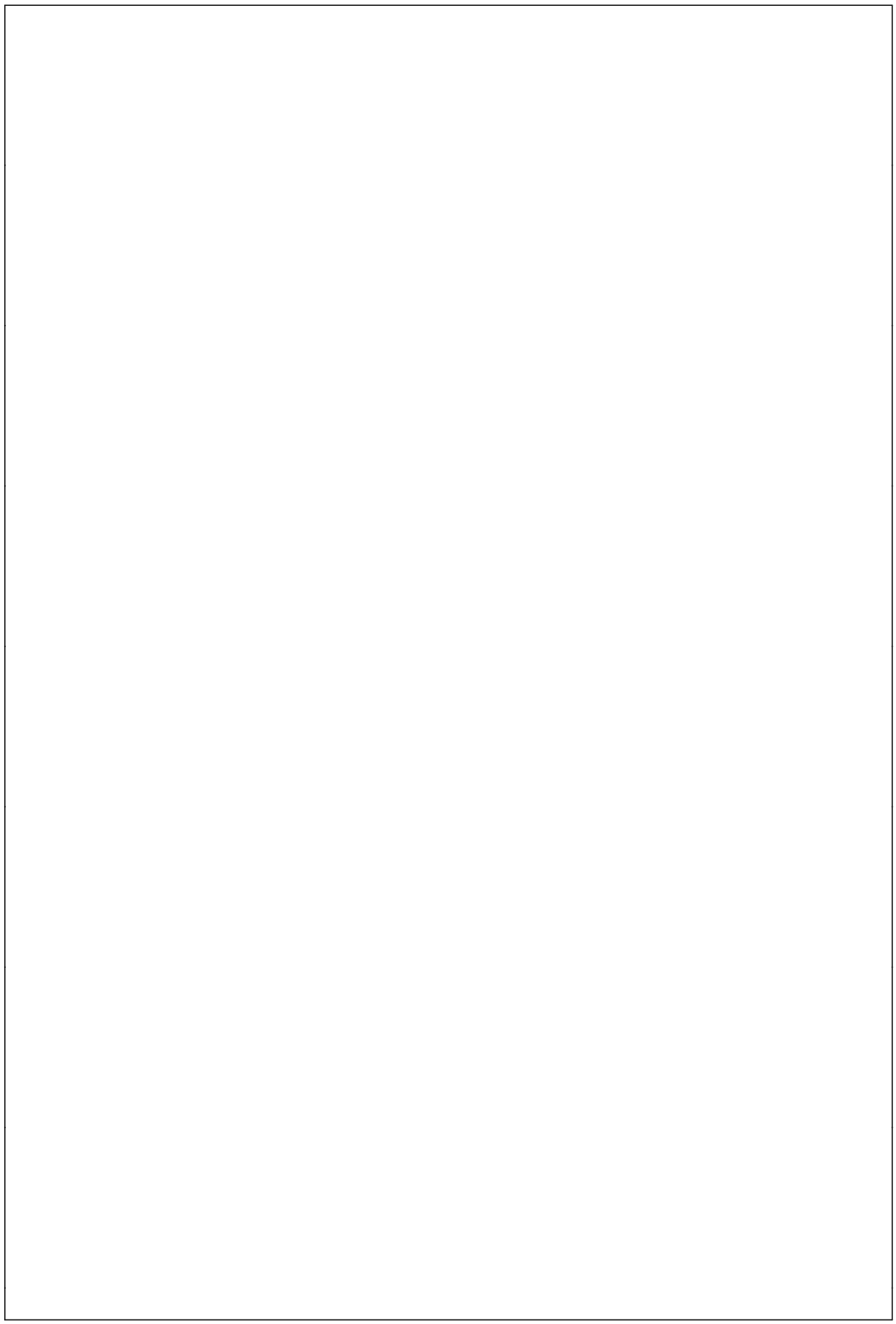
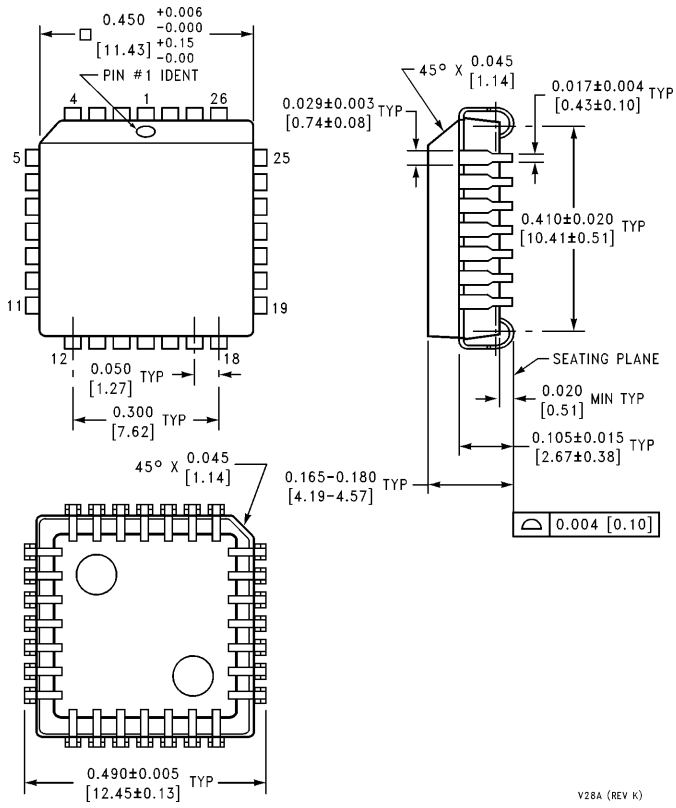
Refer to the Pulse Engineering datasheet for detailed information on the 8.3 SDDI magnetics module.

FIGURE 9. Typical Schematic for SDDI Application



Physical Dimensions inches (millimeters)



28-Pin Plastic Leaded Chip Carrier (V)
Order Number DP83220V
NS Package Number V28A

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