National Semiconductor

Bus Transceivers

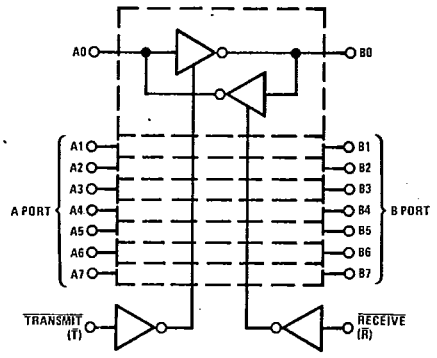
T-52-31

DP7307/DP8307 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

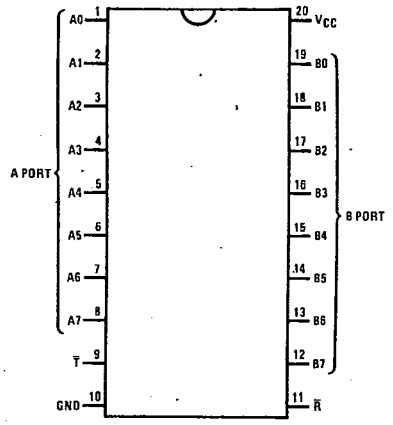
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DP7307J, DP8307J or DP8307N
See NS Package J20A or N20A

Logic Table

CONTROL INPUTS		RESULTING CONDITIONS	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7307	4.5	5.5	V
DP8307	4.75	5.25	V
Temperature (T_A)			
DP7307	−55	125	°C
DP8307	0	70	°C

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DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	DP8307			0.8	V
			DP7307			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA (8307)		0.35	0.5	V
			$I_{OL} = 8$ mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_O = 0V$, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V$, V_{CC} = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B Port (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	DP8307			0.8	V
			DP7307			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_O = 0V$, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V$, V_{CC} = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IL} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA

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DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8307			0.8	V
			DP7307			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		-0.1	-0.25	mA
			$\overline{T}$		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = -12 mA			-0.8	-1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 2.0V, V_{CC} = max			70	100	mA
		$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2V, V_{CC} = max			100	150	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 30 pF		25	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 5k, C4 = 30 pF		24	35	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 8	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	23 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 18	40 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		25 16	35 25	ns ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

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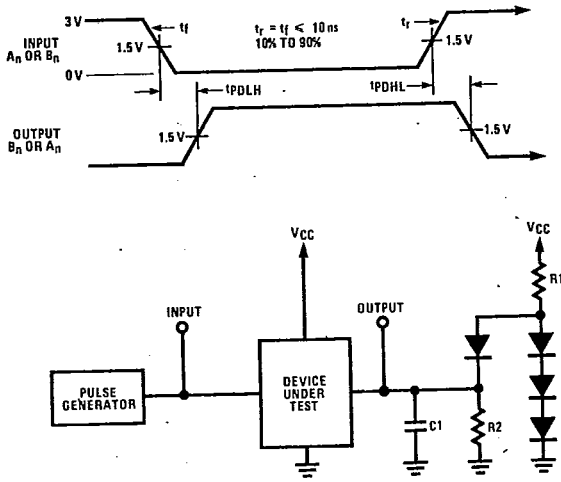
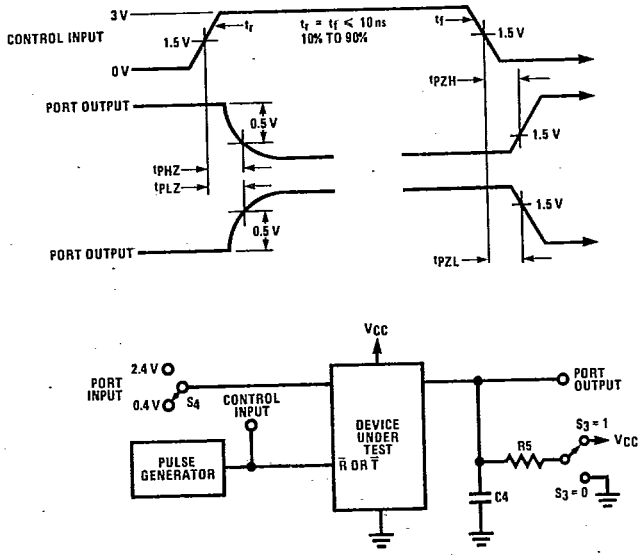
Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

FIGURE A. Propagation Delay from A port to B port or from B port to A port



NOTE: C4 INCLUDES TEST FIXTURE CAPACITANCE.
PORT INPUT IS IN A FIXED LOGICAL CONDITION. SEE AC TABLE.

Figure B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port