

DP8303A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

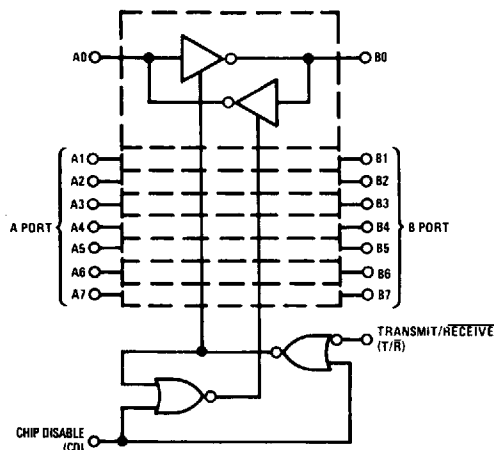
This family of high speed Schottky 8-bit TRI-STATE bidirectional transceivers are designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/Receive (T/R) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 are featured with Transmit (T) and Receive (R) control inputs.

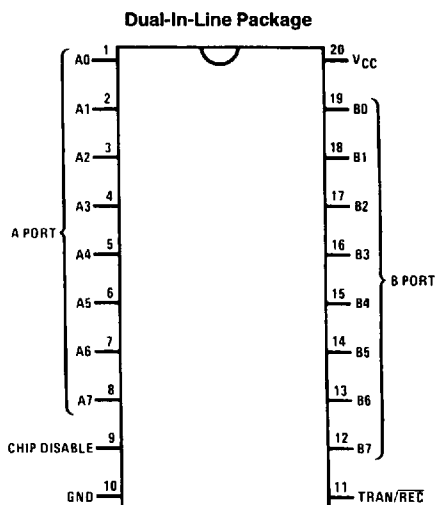
Features

- 8-bit directional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/Receive and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



TL/F/5856-1



TL/F/5856-2

Top View
Order Number DP8303AN
See NS Package Number N20A

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/Receive	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V

Maximum Power Dissipation* at 25°C

Cavity Package	1667 mW
Molded Package	1832 mW

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C.

Storage Temperature	-65°C to +150°C
Lead Temperature (soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8303A	4.75	5.25	V
Temperature (T_A)			
DP8303A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V _{IH}	Logical “1” Input Voltage	CD = V _{IL} , T/ \overline{R} = 2.0V		2.0			V
V _{IL}	Logical “0” Input Voltage	CD = V _{IL} , T/ \overline{R} = 2.0V				0.7	V
V _{OH}	Logical “1” Output Voltage	CD = T/ \overline{R} = V _{IL} V _{IL} = 0.5V	I _{OH} = −0.4 mA I _{OH} = −3 mA	V _{CC} − 1.15 2.7	V _{CC} − 0.7 3.95		V V
V _{OL}	Logical “0” Output Voltage	CD = T/ \overline{R} = V _{IL} V _{IL} = 0.5V	I _{OL} = 16 mA I _{OL} = 8 mA		0.35 0.3	0.5 0.4	V V
I _{OS}	Output Short Circuit Current	CD = V _{IL} , T/ \overline{R} = V _{IL} , V _O = 0V, V _{CC} = Max, (Note 4)		−10	−38	−75	mA
I _{IH}	Logical “1” Input Current	CD = V _{IL} , T/ \overline{R} = 2.0V, V _{IH} = 2.7V			0.1	80	μA
I _I	Input Current at Maximum Input Voltage	CD = 2.0V, V _{CC} = Max, V _{IH} = 5.25V				1	mA
I _{IL}	Logical “0” Input Current	CD = V _{IL} , T/ \overline{R} = 2.0V, V _{IN} = 0.4V			−70	−200	μA
V _{CLAMP}	Input Clamp Voltage	CD = 2.0V, I _{IN} = −12 mA			−0.7	−1.5	V
I _{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V _{IN} = 0.4V V _{IN} = 4.0V			−200 80	μA μA
B PORT (B0–B7)							
V _{IH}	Logical “1” Input Voltage	CD = V _{IL} , T/ \overline{R} = V _{IL}		2.0			V
V _{IL}	Logical “0” Input Voltage	CD = V _{IL} , T/ \overline{R} = V _{IL}				0.7	V
V _{OH}	Logical “1” Output Voltage	CD = V _{IL} , T/ \overline{R} = 2.0V V _{IL} = 0.5V	I _{OH} = −0.4 mA I _{OH} = −5 mA I _{OH} = −10 mA	V _{CC} − 1.15 2.7 2.4	V _{CC} − 0.8 3.9 3.6		V V V
V _{OL}	Logical “0” Output Voltage	CD = V _{IL} , T/ \overline{R} = 2.0V	I _{OL} = 20 mA I _{OL} = 48 mA		0.3 0.4	0.4 0.5	V V
I _{OS}	Output Short Circuit Current	CD = V _{IL} , T/ \overline{R} = 2.0V, V _O = 0V, V _{CC} = Max, (Note 4)		−25	−50	−150	mA
I _{IH}	Logical “1” Input Current	CD = V _{IL} , T/ \overline{R} = V _{IL} , V _{IH} = 2.7V			0.1	80	μA
I _I	Input Current at Maximum Input Voltage	CD = 2.0V, V _{CC} = Max, V _{IH} = 5.25V				1	mA
I _{IL}	Logical “0” Input Current	CD = V _{IL} , T/ \overline{R} = V _{IL} , V _{IN} = 0.4V			−70	−200	μA
V _{CLAMP}	Input Clamp Voltage	CD = 2.0V, I _{IN} = −12 mA			−0.7	−1.5	V
I _{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V _{IN} = 0.4V V _{IN} = 4.0V			−200 +200	μA μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS CD, T/\bar{R}						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.7	V
I_{IH}	Logical "1" Input Current	$V_{IH} = 2.7V$		0.5	20	μA
I_I	Maximum Input Current	$V_{CC} = \text{Max}, V_{IH} = 5.25V$			1.0	mA
I_{IL}	Logical "0" Input Current	$V_{IL} = 0.4V$		-0.1	-0.25	mA
		T/ \bar{R}		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12 \text{ mA}$		-0.8	-1.5	V
POWER SUPPLY CURRENT						
I_{CC}	Power Supply Current	$CD = 2.0V, V_{IN}, V_{CC} = \text{Max}$		70	100	mA
		$CD = 0.4V, V_{INA} = T/\bar{R} = 2V, V_{CC} = \text{Max}$		100	150	mA

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4V, T/\bar{R} = 0.4V$ (Figure A) $R1 = 1k, R2 = 5k, C1 = 30 \text{ pF}$		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4V, T/\bar{R} = 0.4V$ (Figure A) $R1 = 1k, R2 = 5k, C1 = 30 \text{ pF}$		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	$B0 \text{ to } B7 = 2.4V, T/\bar{R} = 0.4V$ (Figure C) $S3 = 1, R5 = 1k, C4 = 15 \text{ pF}$		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	$B0 \text{ to } B7 = 0.4V, T/\bar{R} = 0.4V$ (Figure C) $S3 = 0, R5 = 1k, C4 = 15 \text{ pF}$		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	$B0 \text{ to } B7 = 2.4V, T/\bar{R} = 0.4V$ (Figure C) $S3 = 1, R5 = 1k, C4 = 30 \text{ pF}$		20	30	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	$B0 \text{ to } B7 = 0.4V, T/\bar{R} = 0.4V$ (Figure C) $S3 = 0, R5 = 5k, C4 = 30 \text{ pF}$		19	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4V, T/\bar{R} = 2.4V$ (Figure A) $R1 = 100\Omega, R2 = 1k, C1 = 300 \text{ pF}$		12	18	ns
		$R1 = 667\Omega, R2 = 5k, C1 = 45 \text{ pF}$		7	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4V, T/\bar{R} = 2.4V$ (Figure A) $R1 = 100\Omega, R2 = 1k, C1 = 300 \text{ pF}$		15	20	ns
		$R1 = 667\Omega, R2 = 5k, C1 = 45 \text{ pF}$		9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	$A0 \text{ to } A7 = 2.4V, T/\bar{R} = 2.4V$ (Figure C) $S3 = 1, R5 = 1k, C4 = 15 \text{ pF}$		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	$A0 \text{ to } A7 = 0.4V, T/\bar{R} = 2.4V$ (Figure C) $S3 = 0, R5 = 1k, C4 = 15 \text{ pF}$		8	15	ns
t_{PLZB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	$A0 \text{ to } A7 = 2.4V, T/\bar{R} = 2.4V$ (Figure C) $S3 = 1, R5 = 100\Omega, C4 = 300 \text{ pF}$		25	35	ns
		$S3 = 1, R5 = 667\Omega, C4 = 45 \text{ pF}$		16	25	ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	$A0 \text{ to } A7 = 0.4V, T/\bar{R} = 2.4V$ (Figure C) $S3 = 0, R5 = 1k, C4 = 300 \text{ pF}$		22	35	ns
		$S3 = 0, R5 = 5k\Omega, C4 = 45 \text{ pF}$		14	25	ns

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$ (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT/RECEIVE MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/\bar{R} to A Port	$CD = 0.4V$ (Figure B) $S1 = 1, R4 = 100\Omega, C3 = 5 pF$ $S2 = 1, R3 = 1k, C2 = 30 pF$		23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/\bar{R} to A Port	$CD = 0.4V$ (Figure B) $S1 = 0, R4 = 100\Omega, C3 = 5 pF$ $S2 = 0, R3 = 5k, C2 = 30 pF$		23	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/\bar{R} to B Port	$CD = 0.4V$ (Figure B) $S1 = 1, R4 = 100\Omega, C3 = 300 pF$ $S2 = 1, R3 = 300\Omega, C2 = 5 pF$		23	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/\bar{R} to B Port	$CD = 0.4V$ (Figure B) $S1 = 0, R4 = 1k, C3 = 300 pF$ $S2 = 0, R3 = 300\Omega, C2 = 5 pF$		27	35	ns

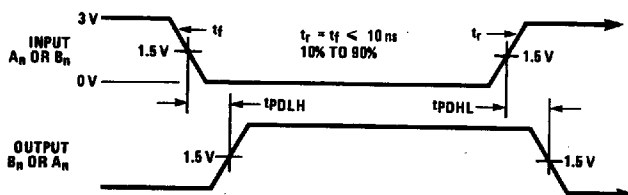
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for $V_{CC} = 5V$ and $T_A = 25^\circ C$.

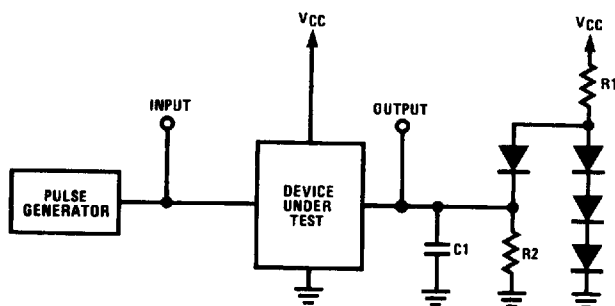
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



TL/F/5856-3



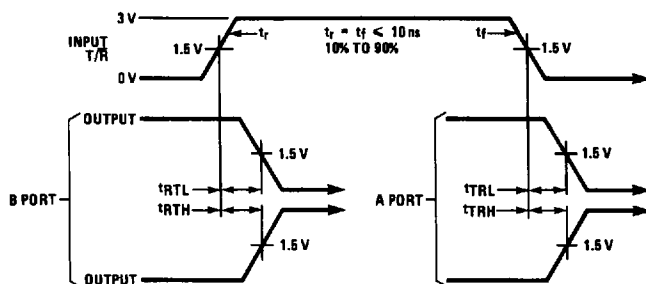
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Note: C1 includes test fixture capacitance.

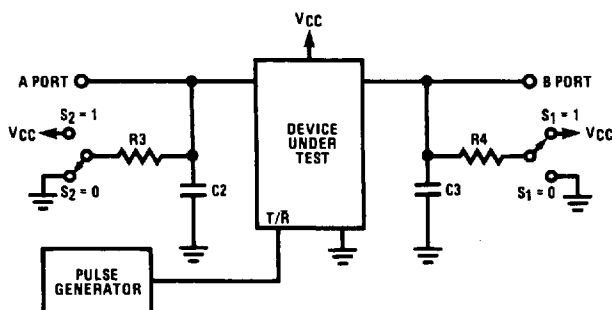
FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (Continued)

DP8303A



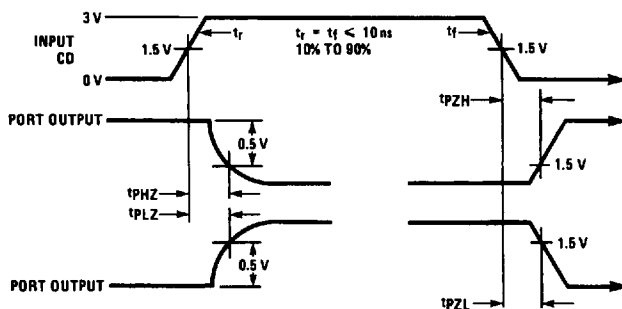
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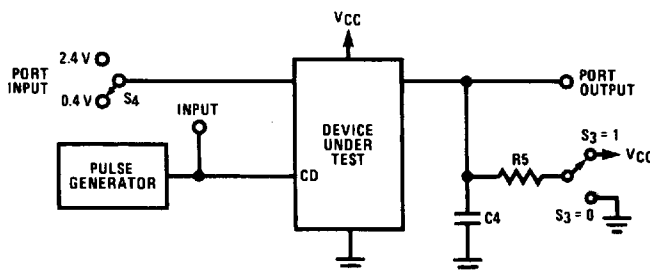
Note: C_2 and C_3 include test fixture capacitance.

TL/F/5856-6

FIGURE B. Propagation Delay from T/R to A Port or B Port



TL/F/5856-7



Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

TL/F/5856-8

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port