FEATURES

- **Low Cost Solution Built-in 800V power BJT**
- **Quasi-Resonant Primary Side Regulation (QR-PSR) Control with High Efficiency**
- **Multi-Mode PSR Control**
- **Fast Dynamic Response**
- **Built-in Dynamic Base Drive**
- **Audio Noise Free Operation**
- **±4% CC and CV Regulation**
- **Low Standby Power <70mW**
- **Programmable Cable Drop Compensation (CDC) in CV Mode**
- **Built-in AC Line & Load CC Compensation**
- **Build in Protections:**
  - **Short Load Protection (SLP)**
  - **Cycle-by-Cycle Current Limiting**
  - **Leading Edge Blanking (LEB)**
  - **Pin Floating Protection**
  - **VDD OVP & UVP & Clamp**
  - **Over temperature protection(OTP)**
- **Available with DP2525G Versions in SOP-7 Package**

APPLICATIONS

- **Battery Chargers for Cellular Phones**
- **AC/DC Power Adapter and LED Lightings**

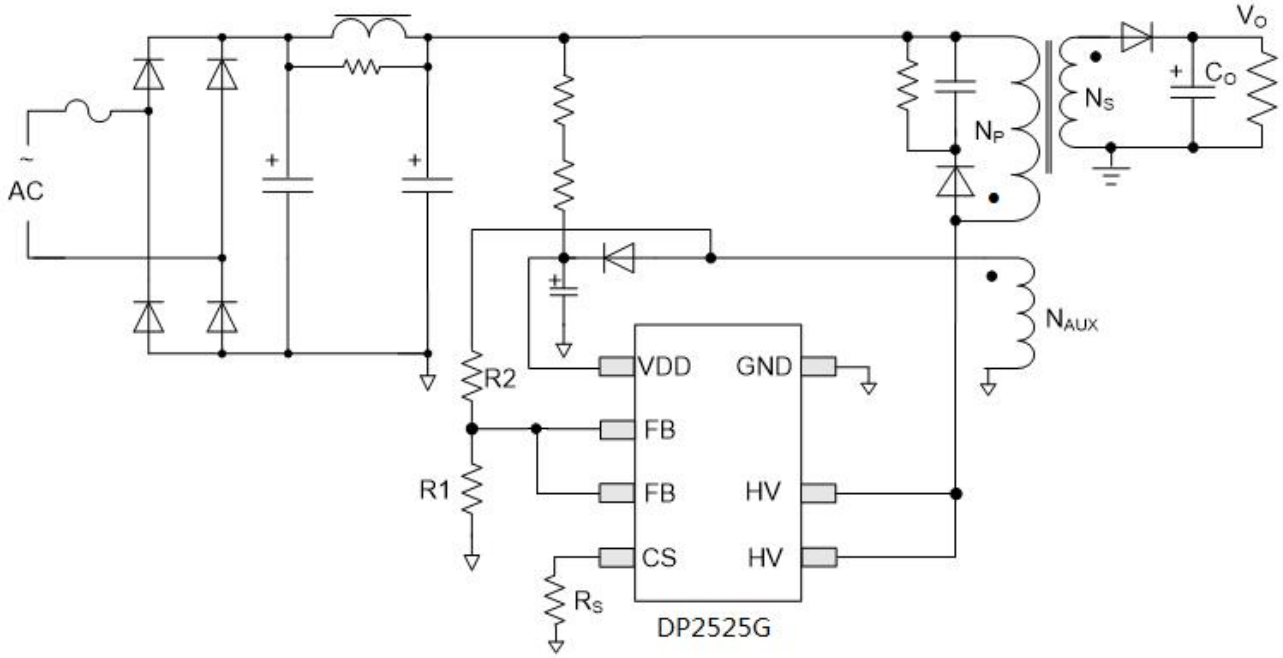
GENERAL DESCRIPTION

DP2525G is a high performance Quasi Resonant (QR) Primary Side Regulation (PSR) PWM power switch with high precision CV/CC control ideal for charger applications.

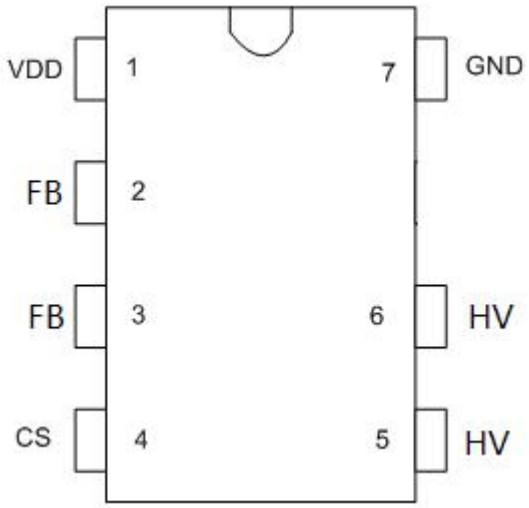
In CV mode, DP2525G adopts Multi Mode QR Control which uses the hybrid of AM (Amplitude Modulation) mode and (Frequency Modulation) FM mode to improve system efficiency and reliability. In CC mode, the IC uses PFM control with line and load CC compensation. The IC can achieve fast dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

DP2525G integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), On-Chip Thermal Shutdown, VDD Clamping, etc.

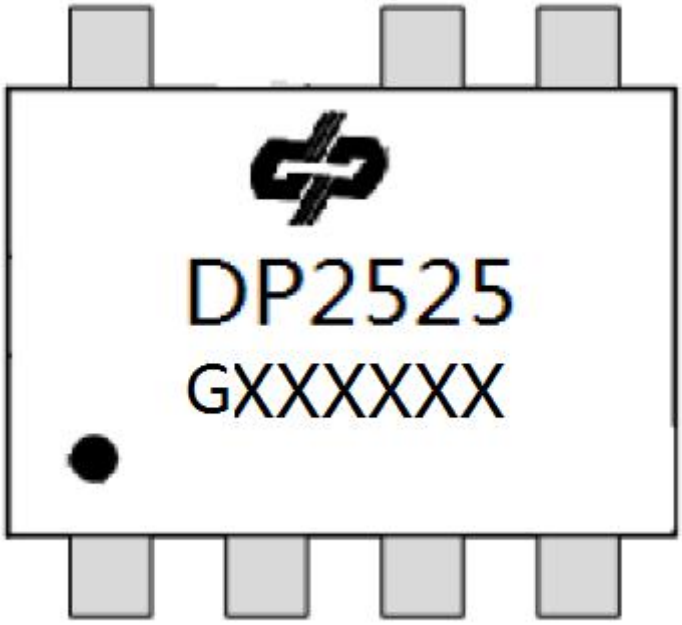
TYPICAL APPLICATION CIRCUIT



Pin Configuration



Marking Information



DPXXXX for product name;

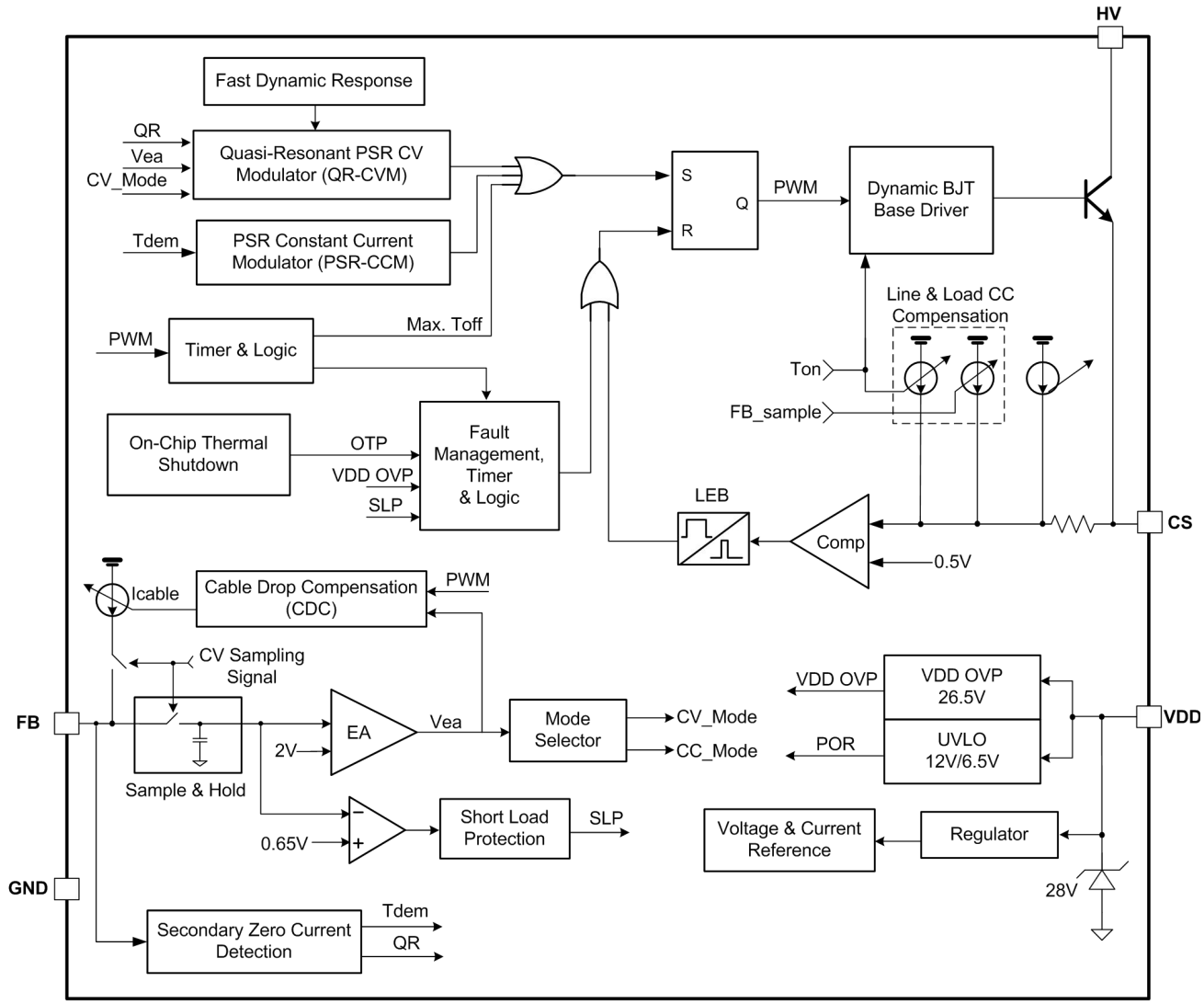
GXXXXXX The G represents the version; The first X reresents the last year,2014 is 4; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said; The last two X represents the wafer batch code.

Pin Description (DP2525G)

Pin Number	Pin Name	I/O	Description
1	VDD	P	Power Supply Pin of the Chip.
2	FB	I	System feedback pin which regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of

			the auxiliary winding.
3	NC	NC	
4	CS	I	Current Sense Input Pin.
5,6	HV	O	The Power BJT Collector
7	GND	P	The Ground of the IC

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
HV PIN Maximum Voltage	800	V
HV PIN DC Current @DP2525G	1300	mA
VDD DC Supply Voltage	30	V
VDD DC Clamp Current	10	mA
CS, BASE voltage range	-0.3 to 7	V
FB voltage range	-0.7 to 7	V
RθJA (℃/W) (SOP7)	90	ºC/W
Maximum Junction Temperature	150	ºC
Operating Temperature Range	-40 to 85	ºC
Storage Temperature Range	-65 to 150	ºC
Lead Temperature (Soldering, 10sec.)	260	ºC
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	7 to 24	V
Operating Ambient Temperature	-40 to 85	ºC
Maximum Switching Frequency @ Full Loading	70	kHz
Minimum Switching Frequency @ Full Loading	35	kHz

ELECTRICAL CHARACTERISTICS (T_A = 25ºC, VDD=20V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin			3	20	uA
I_{VDD_Op}	Operation Current			0.8	1.5	mA
$I_{VDD\_standby}$	Standby Current			0.5	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		10.5	12	13.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		5.5	6.5	7	V
V_{DD_OVP}	VDD OVP Threshold		24	26.5	29	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	$I(V_{DD})$ = 7 mA	26	28	30	V
Control Function Section (FB Pin)						

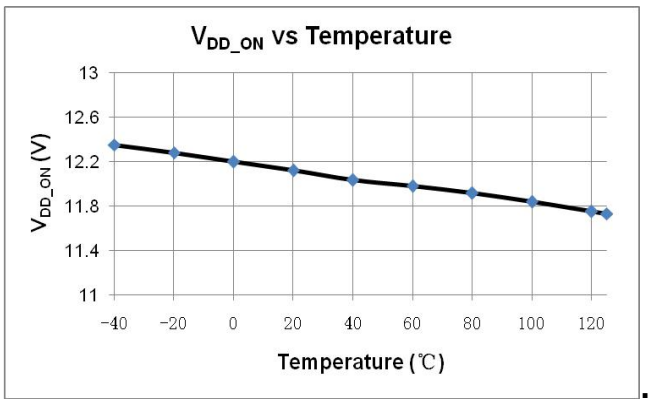
V_{FBREF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.03	V
V_{FB_SLP}	Short Load Protection (SLP) Threshold			0.65		V
T_{FB_Short}	Short Load Protection (SLP) Debounce Time	(Note 3)		36		ms
V_{FB_DEM}	Demagnetization Comparator Threshold			25		mV
T_{off_min}	Minimum OFF time	(Note 3)		2		us
T_{on_max}	Maximum ON time	(Note 3)		20		us
T_{off_max}	Maximum OFF time			5		ms
I_{Cable_max}	Maximum Cable Drop Compensation(CDC) Current			60		uA
T_{SW} /T_{DEM}	Ratio between Switching Period and Demagnetization Time in CC Mode			7/4		
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV
T_{D_OC}	Over Current Detection and Control Delay			100		ns
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 3)	---	155	--	ºC
T_{RC}	Thermal Recovery	(Note 3)		140	--	ºC
BJT Section (HV Pin)						
VCEO	Collector-Emitter voltage			480		V
VCBO	Collector-Base voltage			800		V

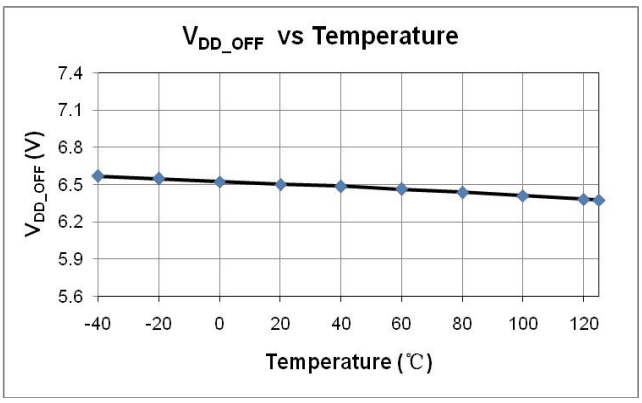
Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

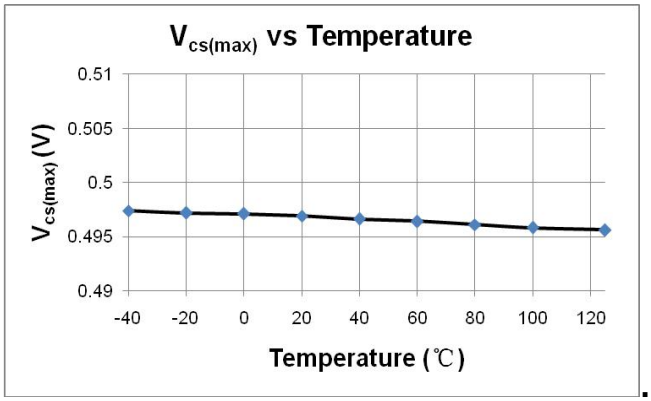
Note2. The device is not guaranteed to function outside its operating conditions.

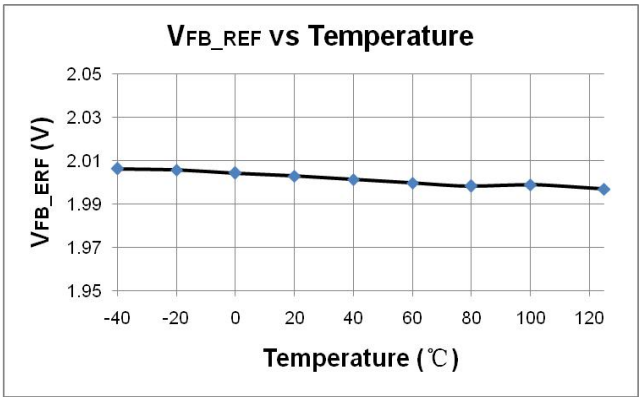
Note3. Guaranteed by the Design.

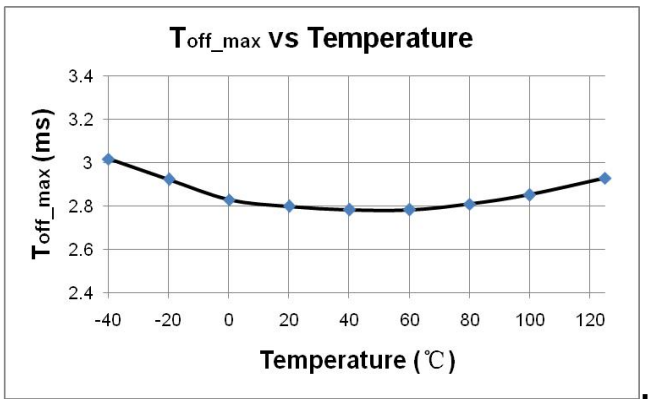
CHARACTERIZATION PLOTS

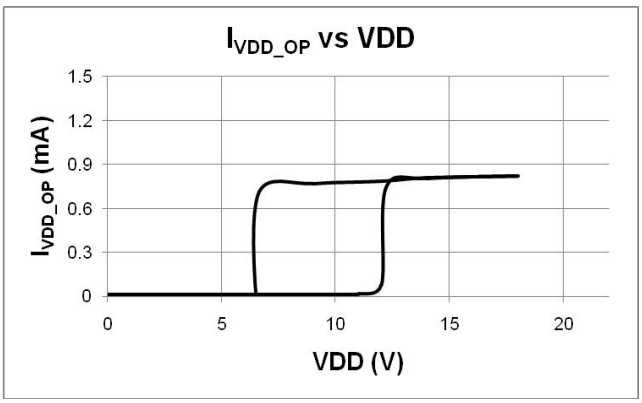












PERATION DESCRIPTION

DP2525G is a high performance, multi mode, highly integrated Quasi Resonant Primary Side Regulation (QR-PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

- **System Start-Up Operation**

Before the IC starts to work, it consumes only startup current (typically 3uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches UVLO turn-on voltage of 12V (typical), DP2525G begins switching and the IC operation current is increased to be 0.8mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

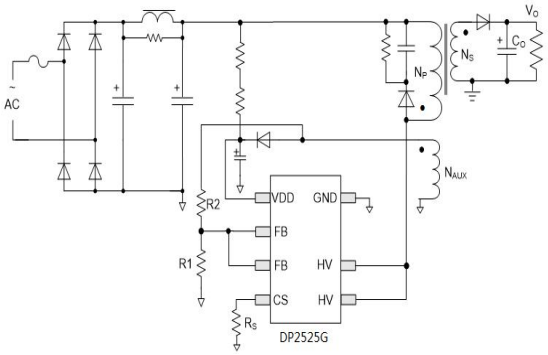


Fig.1

Once DP2525G enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 500uA typically, which helps to reduce the standby power loss.

- **Quasi Resonant PSR CV Modulation (QR-CVM)**

In Primary Side Regulation (PSR) control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates the timing waveform of CV sampling signal, demagnetization signal (DEM) and quasi-resonant (QR) trigger signal in DP2525G. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the Quasi Resonant PSR CV Modulator (QR-CVM) for CV regulation. A valley is selected to trigger new PWM cycle by the output of the QR-CVM bock, which is determined by the load. The internal reference voltage for EA is trimmed to 2V with high accuracy.

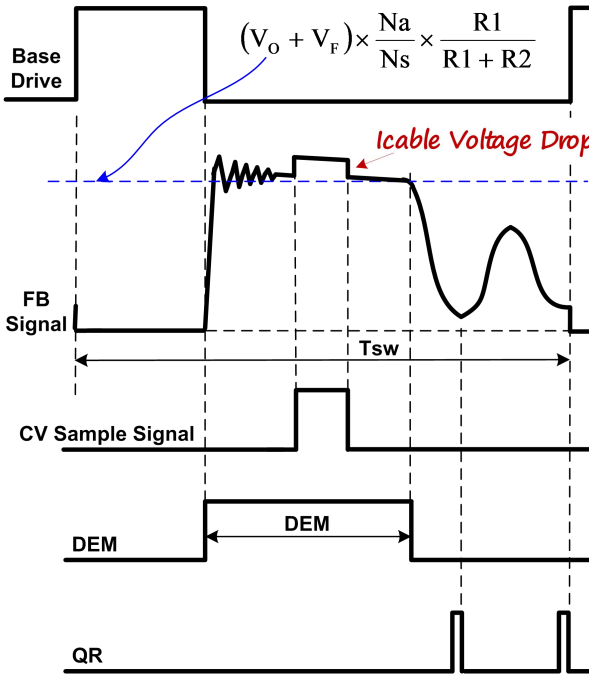


Fig.2

During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for “demagnetization plateau”, where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the

auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively.

When heavy load condition, the Mode Selector (as shown in "**Block Diagram**") based on EA output will switch to CC Mode automatically.

- **PSR Constant Current Modulation (PSR-CCM)**

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp(max), as shown in Fig.3.

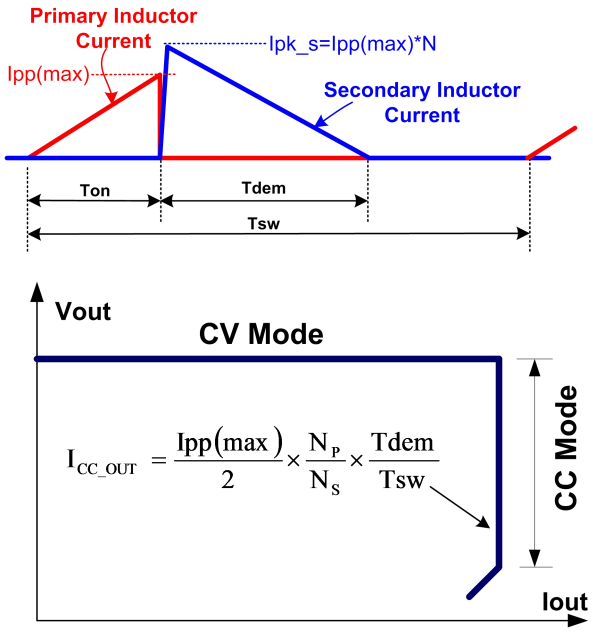


Fig.3

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3. When the average output current Iout reaches the regulation reference in the Primary Side Constant Current Modulator (PSR-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

In DP2525G, the ratio between Tdem and Tsw in CC mode is **4/7**. Therefore, the average output current can be expressed as:

$$I_{CC\_OUT}(mA) \cong \frac{2}{7} \times N \times \frac{500mV}{Rcs(\Omega)}$$

In the equation above,

N----The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power BJT emitter to GND.

- **Multi Mode Control in CV Mode**

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in DP2525G which is shown in the Fig 4.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.

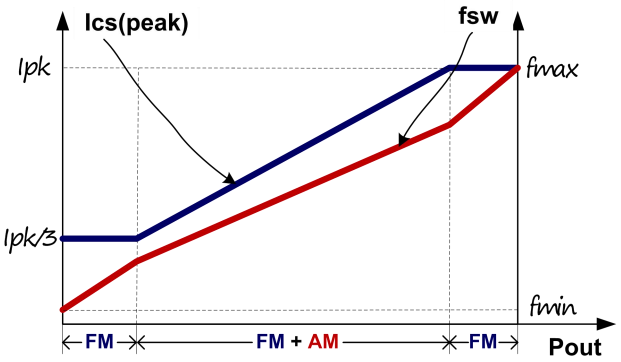


Fig.4

- **Programmable Cable Drop Compensation (CDC) in CV Mode**

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In DP2525G, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in Fig.), the cable loss compensation can be programmed. The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

For example, R1=3K Ω , R2=18K Ω , The percentage of maximum compensation is given by:

$$\frac{\Delta V(cable)}{Vout} = \frac{60uA \times (3K//18K)}{2V} \times 100\% = 7.7\%$$

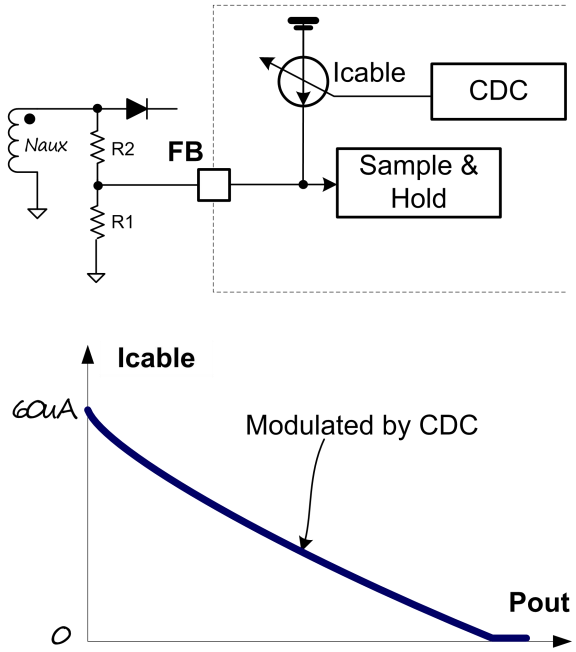


Fig.5

- **Optimized Dynamic Response**

In DP2525G, the dynamic response performance is optimized to meet USB charge requirements.

- **On Chip Thermal Shutdown (OTP)**

When the IC temperature is over 155 °C, the IC shuts down. Only when the IC temperature drops to 140 °C, IC will restart.

- **Audio Noise Free Operation**

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation. In DP2525G, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **Dynamic BJT Base Drive**

DP2525G drives a power BJT with dynamic base drive control to optimize efficiency. The BJT base

drive current ranges from 12mA to 35mA (typical), and is dynamically controlled according to the power supply load change. The higher the output power, the higher the based current. Specifically, the base current is related to CS peak voltage, as shown in Fig.6

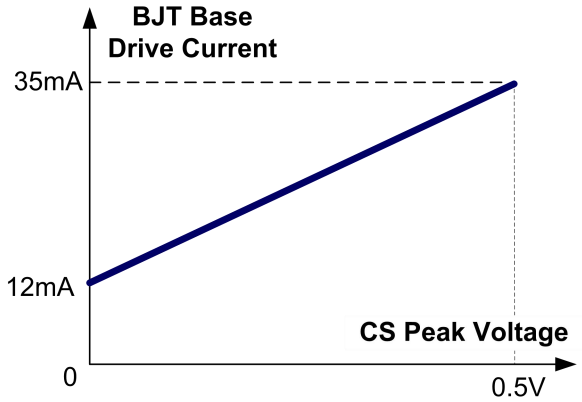


Fig.6

- **Short Load Protection (SLP)**

In DP2525G, the output is sampled on FB pin and then compared with a threshold of UVP (0.65V typically) after an internal blanking time (10ms typical).

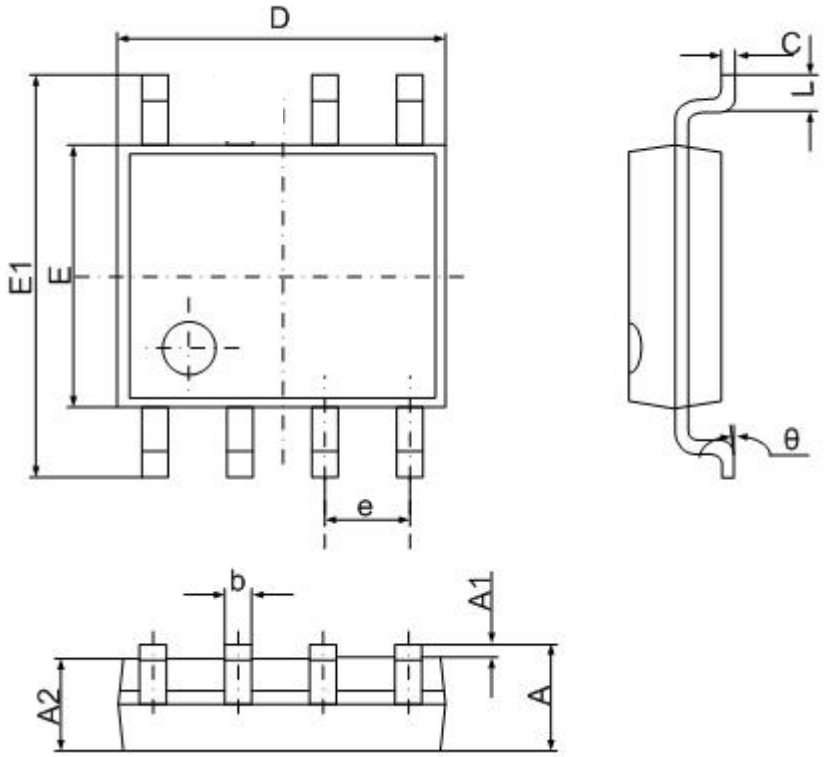
In DP2525G, when sensed FB voltage is below 0.6V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 26.5V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 6.5V) and then the system will restart up again. An internal 28V (typical) zener clamp is integrated to prevent the IC from damage.

Package Dimension

SOP7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max		Min
A	1.350	1.750	A	1.350
A1	0.100	0.250	A1	0.100
A2	1.350	1.550	A2	1.350
b	0.330	0.510	b	0.330
c	0.170	0.250	c	0.170
D	4.700	5.100	D	4.700
e	1.270（BSC）	0.050（BSC）	e	1.270（BSC）
E1	5.800	6.200	E1	5.800
E	3.800		4.000	
L	0.400	1.270	L	0.400
θ	0°	8°	θ	0°