# Product Specification

- **Product Name: AMOLED**
- **Model Name: DO0206FMST01**
- **Description: 2.06 inch (410 x 502)**

| Proposed by | | | Customer's Approval |
|---|---|---|---|
| Designed | Checked | Approved | |
| | | | |

**Document Revision History**

| Rev. No. | Date | Contents | Remark |
|---|---|---|---|
| 0.0 | 2024-03-15 | -.Initial issue | Preliminary |
| 0.1 | 2024-03-20 | -.Correction of recommended connector type (in block diagram) | |
| | | | |
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| | | | |
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# 1.General Description:

- Driving Mode: Active Matrix.
- Color Mode: Full Color (65K/262K/16.7M color)
- Display Format: 2.06" (410 x 502)
- Display Driver IC : ICNA3311(CO5300) or Compatible
- Touch Driver IC : FT3168 or Compatible
- Display Interface: SPI 3-wire/ SPI 4-wire/QSPI/MIPI-DSI 1Lane
- Touch Interface: IIC [ Slave Addr A[6:0]---0X38]
- Application: Handheld & PDA
- RoHS Compatible

# 2.Mechanical Data

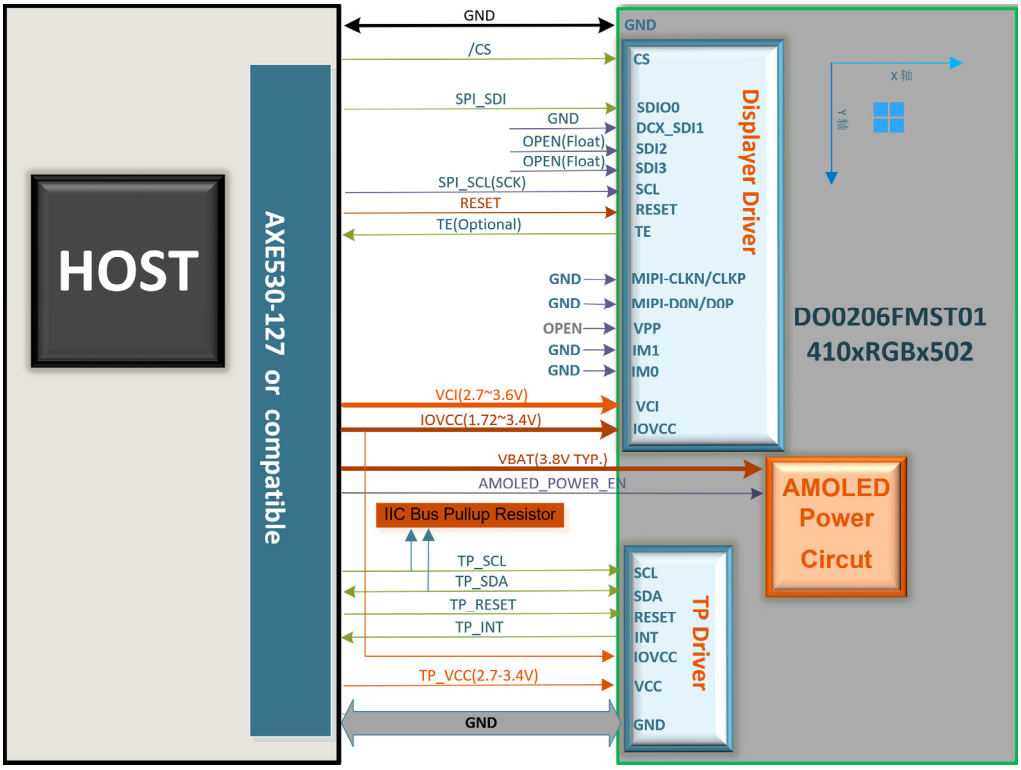
| Item | Specification | unit |
|---|---|---|
| Display Mode | AMOLED | - |
| Dimensional outline<br>[ Without Cover Lens ] | 34.79(W) x 43.14(H) x0.8 (T) | mm |
| Number of dots | 410(W) x RGB x 502 (H) | dots |
| Active area | 33.09(W) x 40.51(H) | mm |
| Diagonal Inch | 2.06 | inch |
| Pixel pitch | 81*81 | μm |
| Weight | TBD | g |

***See attached drawing for details.**

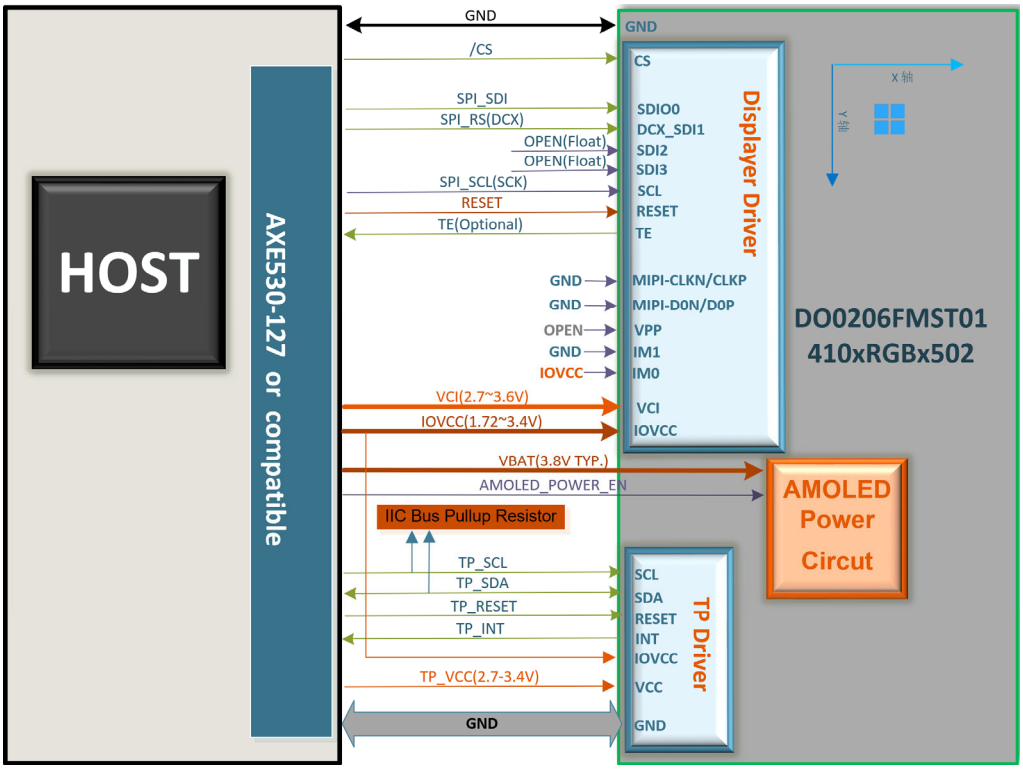
# 3.Block Diagram

DO0206FMST01 support various interfaces, and interfaces are selected by the **IM[1:0]** pins.

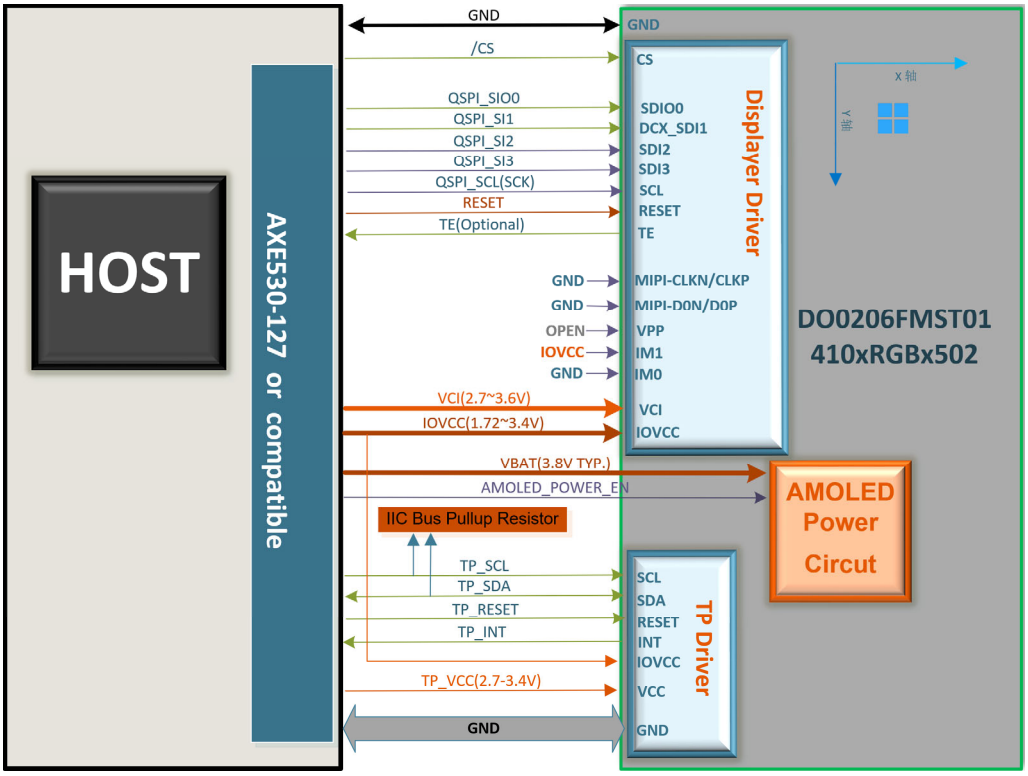
**A:** If IM1=GND,IM0=GND, DO0206FMST01 set to **spi-3wire interface**



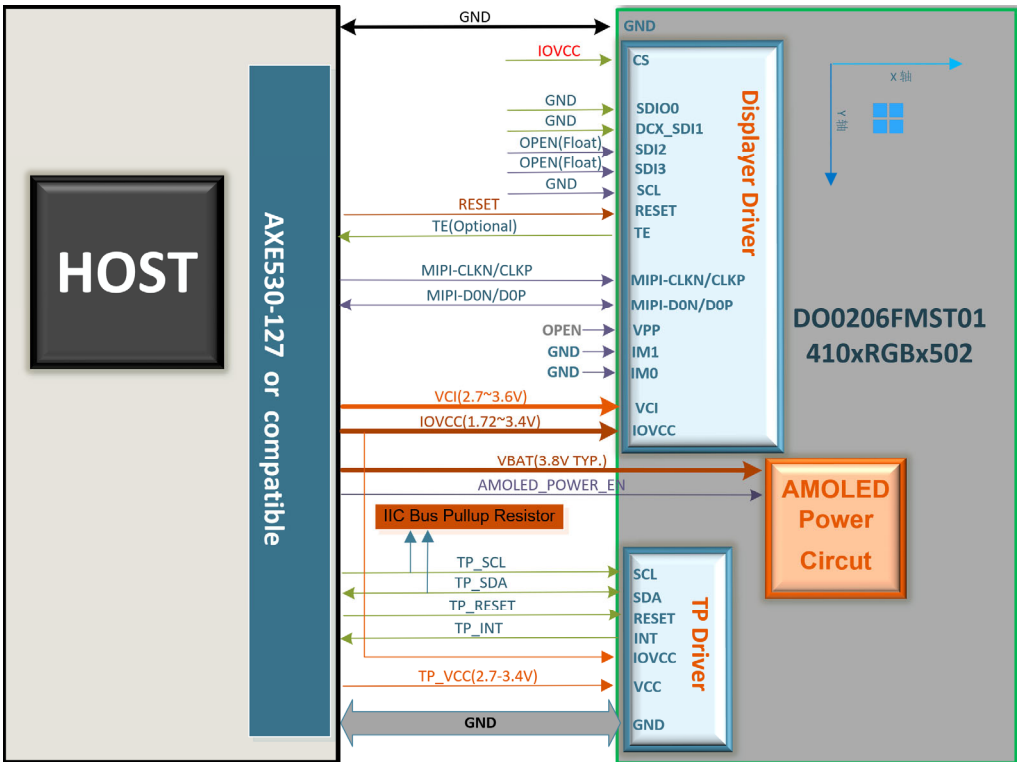

**B:** If IM1=GND,IM0=IOVCC, DO0206FMST01 set to **spi-4wire interface**



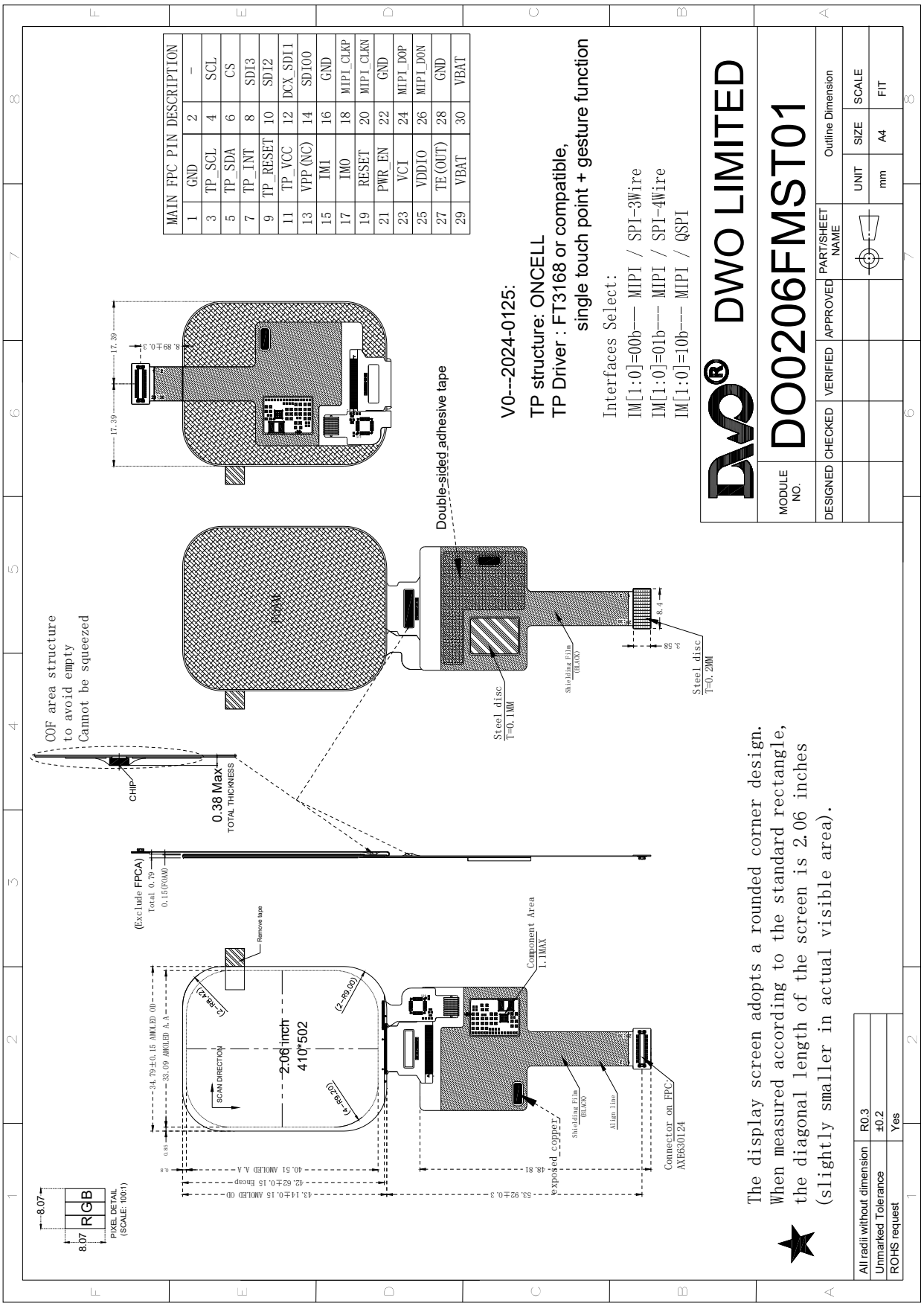
**C:** If IM1=IOVCC,IM0=GND, DO0206FMST01 set to **QSPI interface**




**D:** If IM1=GND,IM0=GND, CS=IOVCC, DO0206FMST01 set to **MIPI-DSI interface**



# 4.Dimension


MAIN FPC PIN DESCRIPTION
1 GND 2 –
3 TP_SCL 4 SCL
5 TP_SDA 6 CS
7 TP_INT 8 SDI3
9 TP_RESET 10 SDI2
11 TP_VCC 12 DCX_SDI1
13 VPP(NC) 14 SDIO0
15 IM1 16 GND
17 IM0 18 MIPI_CLKP
19 RESET 20 MIPI_CLKN
21 PWR_EN 22 GND
23 VCI 24 MIPI_D0P
25 VDDIO 26 MIPI_D0N
27 TE(OUT) 28 GND
29 VBAT 30 VBAT
V0---2024-0125:
TP structure: ONCELL
TP Driver : FT3168 or compatible,
single touch point + gesture function
Interfaces Select:
IM[1:0]=00b— MIPI / SPI-3Wire
IM[1:0]=01b— MIPI / SPI-4Wire
IM[1:0]=10b— MIPI / QSPI
DWO LIMITED
MODULE NO.
DO0206FMST01
DESIGNED
CHECKED
VERIFIED
APPROVED
PART/SHEET NAME
Outline Dimension
UNIT mm
SIZE A4
SCALE FIT
Double-sided adhesive tape
FOAM
Steel disc T=0.1MM
Steel disc T=0.2MM
Shielding Film (BLACK)
COF area structure
to avoid empty
Cannot be squeezed
CHIP
0.38 Max
TOTAL THICKNESS
(Exclude FPCA) Total 0.79
0.15(FOAM)
Remove tape
Component Area 1.1MAX
2.06 inch
410*502
SCAN DIRECTION
34.79±0.15 AMOLED OD
33.09 AMOLED A.A
40.51 AMOLED A.A
42.62±0.15 Hsap
43.14±0.15 AMOLED OD
48.81
53.92±0.3
exposed copper
Align line
Connector on FPC: AXE630124
PIXEL DETAIL (SCALE: 100:1)
8.07
RGB
All radii without dimension R0.3
Unmarked Tolerance ±0.2
ROHS request Yes
The display screen adopts a rounded corner design.
When measured according to the standard rectangle,
the diagonal length of the screen is 2.06 inches
(slightly smaller in actual visible area).

# 5.Pin Description

Recomend Connector : AXE530-127.(AXE630124 on AMOLED)

| NO. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | GND | P | Ground Terminal |
| 3 | TP_SCL | I | Touch Panel Clock Input. Communication Voltage follow IOVCC<br>If not used, please open this pin. |
| 5 | TP_SDA | I/O | Touch Panel Data Input and output.<br>Communication Voltage follow IOVCC<br>If not used, , please open this pin. |
| 7 | TP_INT | O | Touch Panel Interrupt Output.<br>If not used, please open this pin. |
| 9 | TP_RESET | I | TP Reset signal Input.<br>Communication Voltage follow IOVCC<br>If not used, , please open this pin. |
| 11 | TP_VCC | P | Analog Voltage for TP Driver (2.7~3.4V) |
| 13 | VPP(NC) | P | OTP Power Supply(Let it open). |
| 15 | IM1 | I | Interface type selection |
| 17 | IM0 | I | Interface type selection |
| 19 | RESET | I | AMOLED Reset signal Input |
| 21 | PWR_EN | I | Power IC enable control pin. |
| 23 | VCI_IN | P | Analog Voltage for Display Driver (2.7~3.6V) |
| 25 | VDDIO(IOVCC) | P | Driver IC(Touch + Display) Digital I/O Power Supply(1.72~3.4V) |
| 27 | TE | O | Tearing Effect |
| 29 | VBAT | P | Battery Voltage 3.8V TYP. (2.9-4.5V) |
| NO. | Pin Name | I/O | Description |
| 2 | - | - | |
| 4 | SCL | I | SCL: A synchronous clock signal in SPI I/F. |
| 6 | CS | I | Chip select input pin (“Low” enable) SPI I/F.<br>If not used(MIPI Interface), please connect these pin to IOVCC. |
| 8 | SDI3 | I | Serial Data Input in QSPI,data Lane 3.<br>If not used, please open this pin. |
| 10 | SDI2 | I | Serial Data Input in QSPI,data Lane 2.<br>If not used, please open this pin. |
| 12 | DCX_SDI1 | I/O | Serial Data Input in QSPI,data Lane 2.<br>Serial Data Output in SPI_3Wire/ SPI_4Wire<br>Data Input Signal at Dual Input Mode.<br>Display data / command selection in SPI 4-wire I/F.<br>D/CX = ”0” : Command;<br>D/CX = ”1” : Display data or Parameter |

| | | | |
|---|---|---|---|
| | | | If not used, please open this pin. |
| 14 | SDIO0 | I/O | Serial Data Input in QSPI,data Lane 0.<br>Serial Data intput in SPI_3Wire/ SPI_4Wire<br>Data Input Signal at Dual Input Mode.<br>RDX : Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface.<br>If not used, please connect these pins to GND. |
| 16 | GND | P | Ground Terminal |
| 18 | MIPI_CLKP | I | Differential clock signals if MIPI interface.<br>If not used, please connect these pins to GND. |
| 20 | MIPI_CLKN | I | Differential clock signals if MIPI interface.<br>If not used, please connect these pins to GND. |
| 22 | GND | P | Ground Terminal |
| 24 | MIPI_D0P | I/O | Differential data signals if MIPI interface.<br>If not used, please connect these pins to GND. |
| 26 | MIPI_D0N | I/O | Differential data signals if MIPI interface.<br>If not used, please connect these pins to GND. |
| 28 | GND | P | Ground Terminal |
| 30 | VBAT | P | Battery Voltage 3.8V TYP. (2.9-4.5V) |

# 6. DC Characteristics

Test Conditions :Voltage Referenced to VSS=0V, IOVCC = 1.8V, VCC=3.3V,VBAT=3.3V,TA = 25℃
Unless otherwise specified

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage (Display) | | VCC | | 2.7 | 3.3 | 3.5 | V |
| | | IOVCC | | 1.65 | 1.8 | 3.4 | V |
| | | BAT | - | 2.9 | 3.8 | 4.5 | V |
| Input voltage | 'L' level | VIL | IOVCC=1.7V ~3.3V | GND | - | 0.2*IOVCC | V |
| | 'H' level | VIH | | 0.8*IOVCC | - | IOVCC | V |
| Output voltage | 'L' level | VOL | I(OH)=-1mA I(OL)=+1mA | GND | - | 0.2*IOVCC | V |
| | 'H' level | VOH | | 0.8*IOVCC | - | IOVCC | V |
| Current (Display) | Sleep out mode | $I_{VCC}$ | Full white display, 350nits, | - | 2.9 | - | mA |
| | | $I_{IOVCC}$ | | - | 2.8 | - | mA |
| | | $I_{VBAT}$ | | - | 46 | 80(600) | mA |
| | Sleep in mode | $I_{VCC}$ | | - | 300 | 500 | uA |
| | | $I_{IOVCC}$ | | - | 300 | 500 | uA |
| | | $I_{VBAT}$ | | | 10 | 150 | uA |
| | Deep Standby Mode | $I_{VCC}$ | | - | TBD | TBD | uA |
| | | $I_{IOVCC}$ | | - | TBD | TBD | uA |
| | | $I_{VBAT}$ | | | 10 | 30 | uA |
| Frame Frequency | | $f_{FRM}$ | | - | 60 | - | Hz |

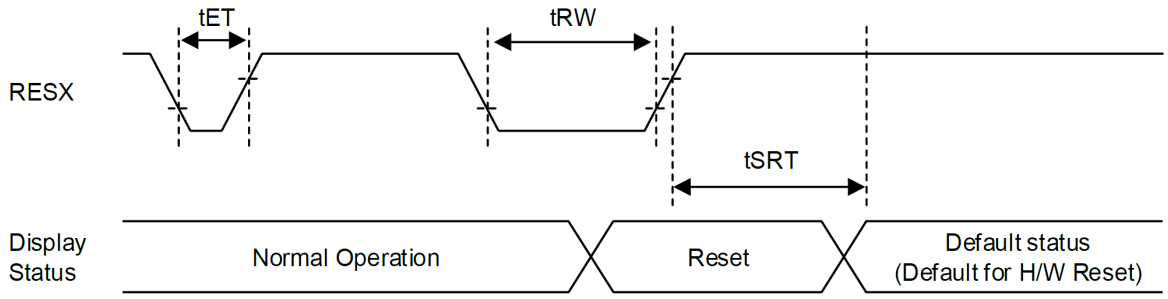
Test Conditions :Voltage Referenced to VSS=0V, TP_IOVCC = 1.8V, TP_VCC=3.3V, TA = 25℃
Unless otherwise specified

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage (Display) | | VCC | | 2.75 | 2.8 | 3.5 | V |
| | | IOVCC | | 1.65 | 1.8 | 3.35 | V |
| Input voltage | 'L' level | VIL | IOVCC=1.65V ~3.3V | GND | - | 0.3*IOVCC | V |
| | 'H' level | VIH | | 0.7*IOVCC | - | IOVCC | V |
| Output voltage | 'L' level | VOL | I(OH)=-1mA I(OL)=+1mA | GND | - | 0.3*IOVCC | V |
| | 'H' level | VOH | | 0.7*IOVCC | - | IOVCC | V |
| Current (Touch) | Sleep out mode | $I_{VCC}$ | | - | 0.5 | - | mA |
| | | $I_{IOVCC}$ | | - | 1.5 | - | mA |
| | monitor mode | $I_{VCC}$ | | - | 30 | 50 | uA |
| | | $I_{IOVCC}$ | | - | 30 | 50 | uA |
| | Sleep Mode | $I_{VCC}$ | | - | 10 | 20 | uA |
| | | $I_{IOVCC}$ | | - | 10 | 20 | uA |
| Sensor acceptable clock | | ftx | | - | 100 | - | KHz |

# 7.AC characteristics

## 7-1 Reset Timing

### Reset timing characteristic



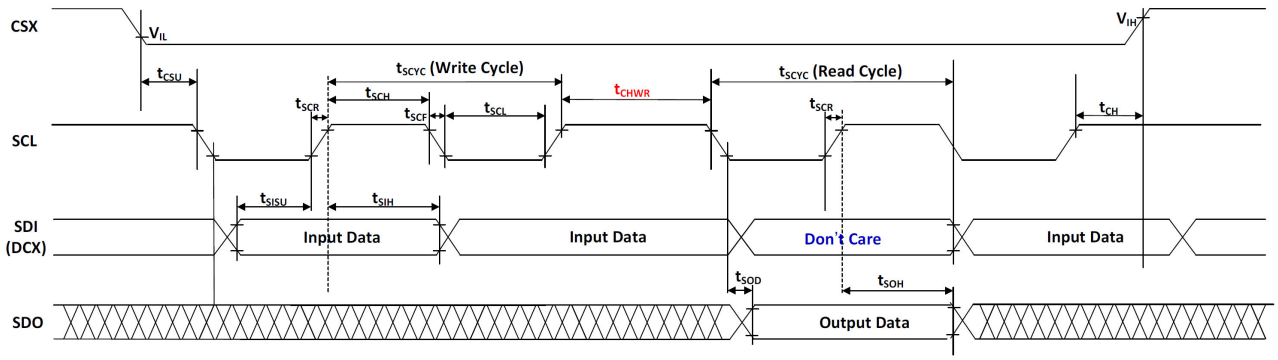

VSS=0V, VDDIO=1.7V to 3.3V, VCI=2.5V to 3.3V,Ta = -30 to 70℃

| Parameter | Symbol | Pad | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Reset low pulse width | tRW | RESX | 10 | – | – | µs | – |
| Secure reset completion time | tSRT | RESX | – | – | 5 | ms | Reset during Sleep In mode |
| | | RESX | – | – | 150 | | Reset during Sleep Out mode |
| Reset un-reacted pulse width | tET | RESX | | | 5 | µs | – |

## 7-2 SPI Timing

### SPI-3Wire/ SPI-4Wire Interface Characteristics

3/4-wire SPI



| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock cycle | $t_{SCYC}$ | Write | 20 | | | ns |
| | | Read | 300 | | | ns |
| Clock high pulse width | $t_{SCH}$ | Write | 6.5 | | | ns |
| | $t_{SCH}$ | Read | 140 | | | ns |
| Clock low pulse width | $t_{SCL}$ | Write | 6.5 | | | ns |
| | $t_{SCL}$ | Read | 140 | | | ns |
| Clock rise time | $t_{SCR}$ | 0.2*VDDI -> 0.8*VDDI | | | 3.5 | ns |
| Clock fall time | $t_{SCF}$ | 0.8*VDDI -> 0.2*VDDI | | | 3.5 | ns |
| Chip select setup time | $t_{CSU}$ | | 10 | | | ns |
| Chip select hold time | $t_{CH}$ | | 10 | | | ns |
| Data input setup time | $t_{SISU}$ | To $V_{IL}$ of SCL's rising edge | 5 | | | ns |
| Data input hold time | $t_{SIH}$ | | 5 | | | ns |
| Access time of output data | $t_{SOD}$ | From $V_{IL}$ of SCL's falling edge | | | 120 | ns |
| Hold time of output data | $t_{SOH}$ | From $V_{IH}$ of SCL's rising edge | 5 | | | ns |
| Transition time from Write cycle to Read cycle | $t_{CHWR}$ | From $V_{IH}$ of SCL's rising edge | 150 | | | ns |

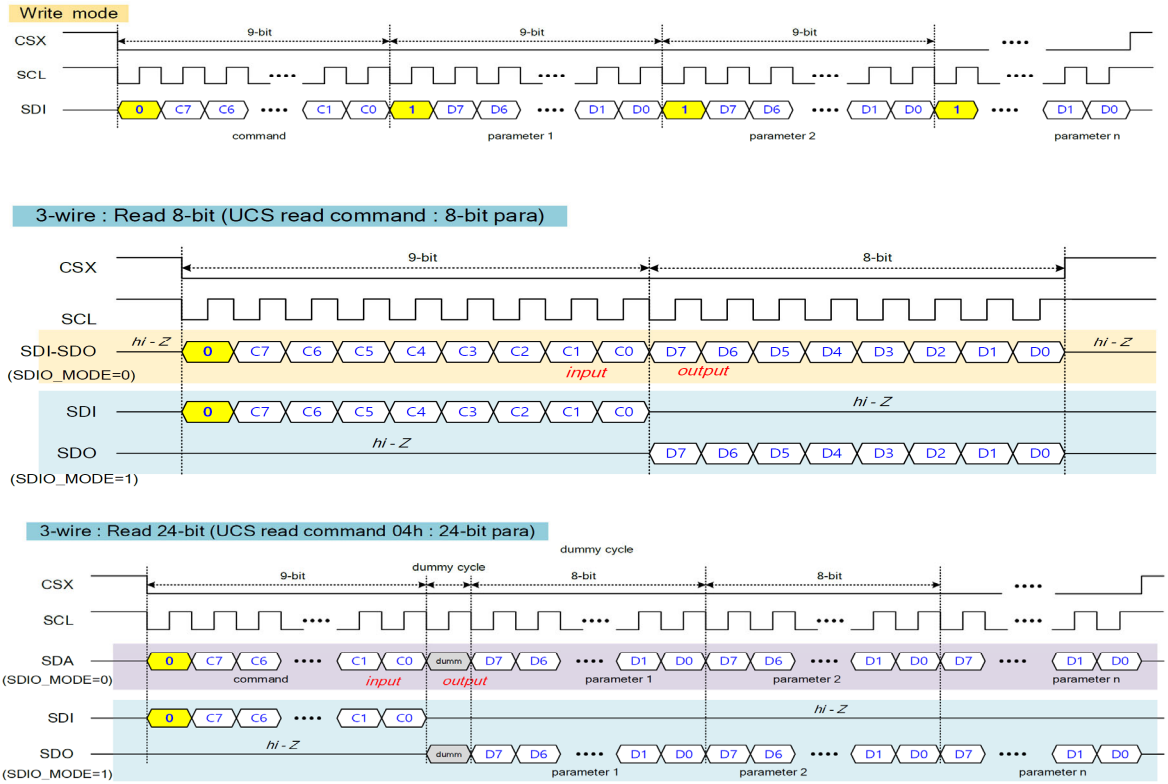
Notes:

(1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.

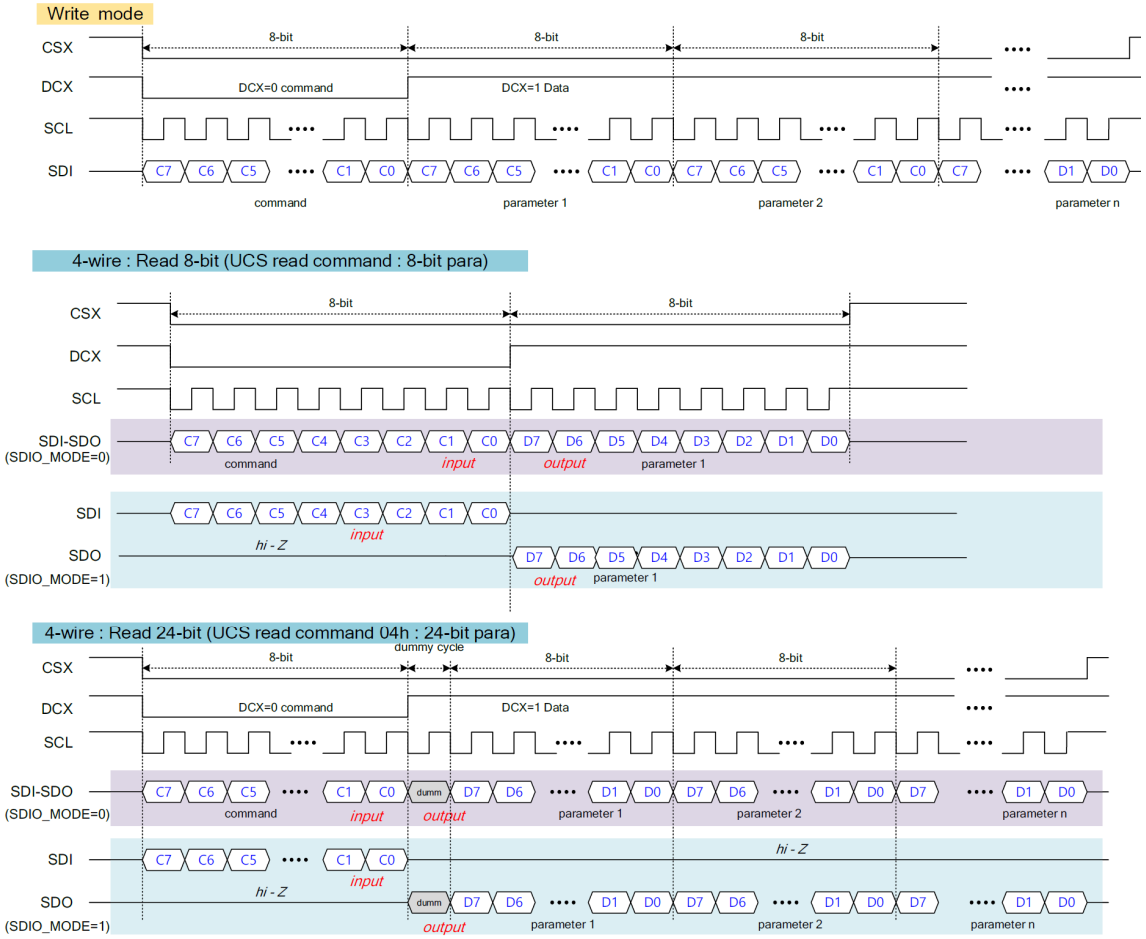
(2) For the 4-wire SPI, the DCX's timing is the same as input data.

(3) Ta = -30°C to 70°C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, and VSS=0V

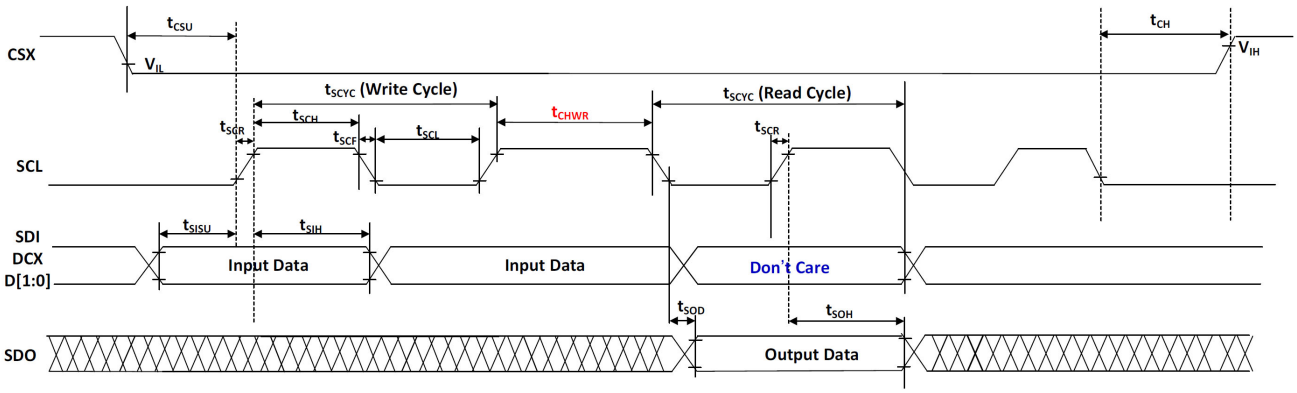
## SPI-3 Wire (9-Bit) Interface Protocol – Register Write and Read



## SPI-4 Wire (8-Bit) Interface Protocol – Register Write and Read




## 7-3 QSPI Interface Characteristics




Note: The max SCL frequency for each pixel data format is specified as the below table.

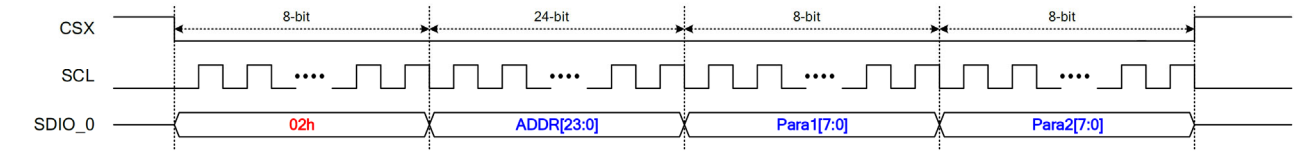
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V

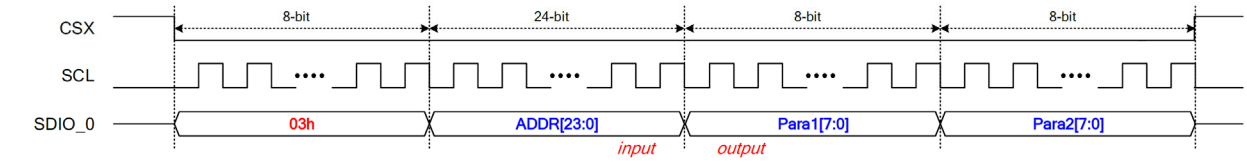
# QSPI Timing

## Quad SPI Interface Protocol – Register Read and Write

Command Write

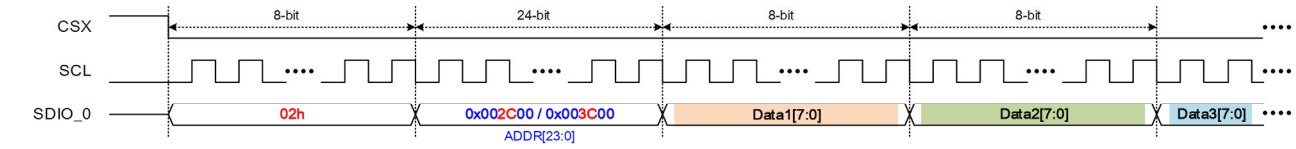



Command Read

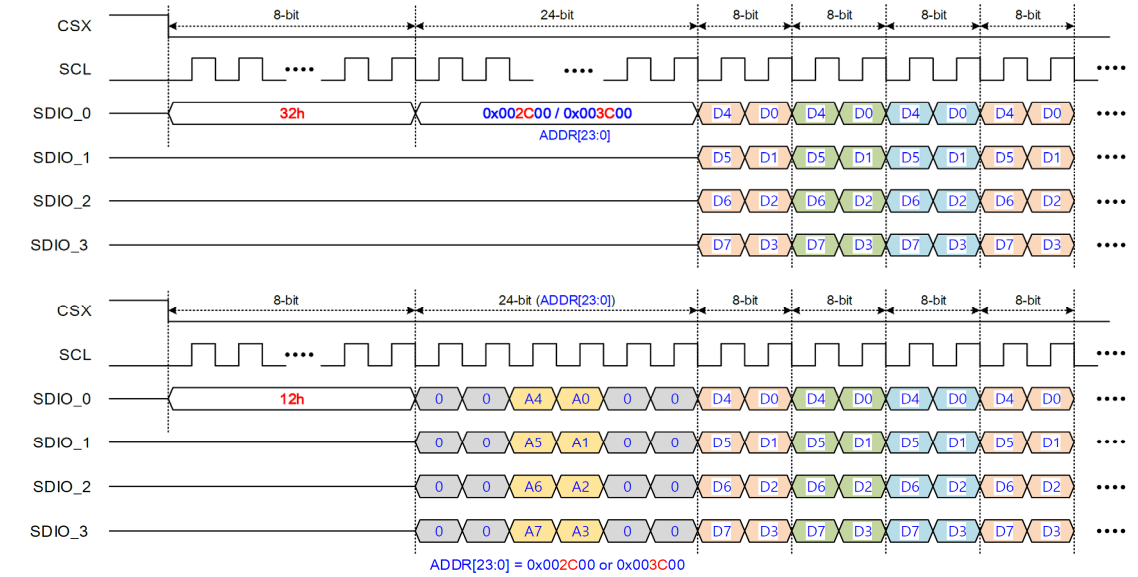



## Quad SPI Interface Protocol – Pixel Interface

1-Wire Pixel Write




4-Wire Pixel Write

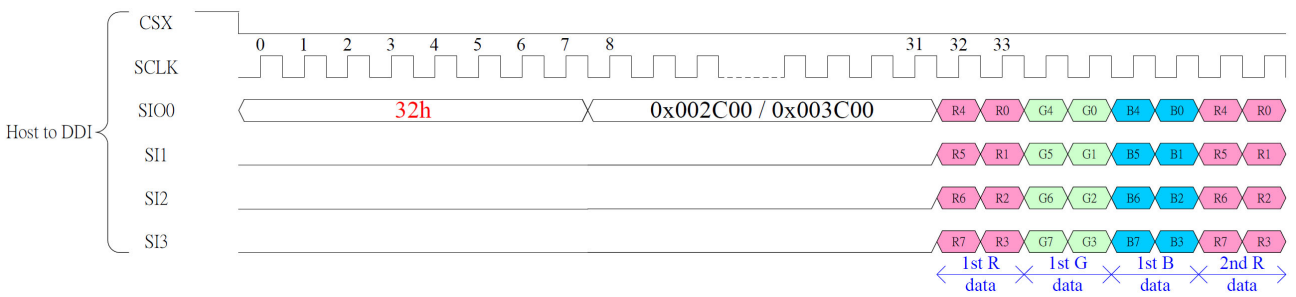




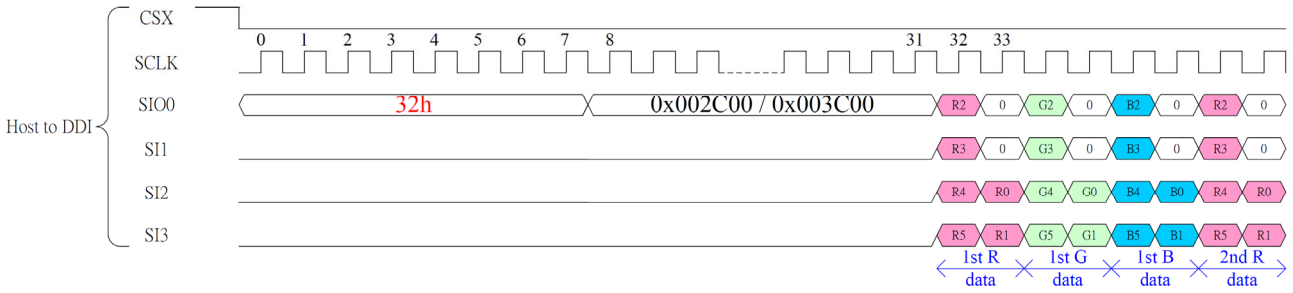


### SPI-4Lanes Pixel Write Data Waveform

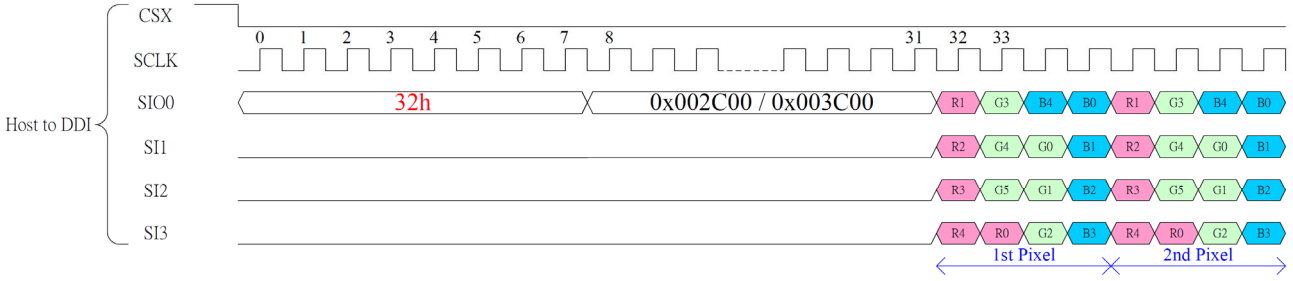
### RGB888 – 4-Lanes



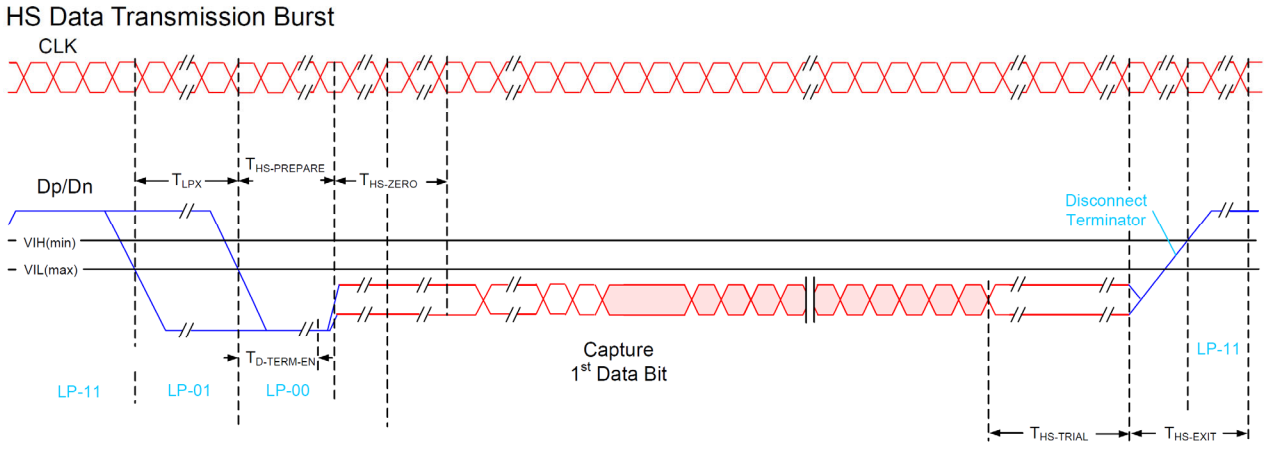
**RGB666 – 4-Lanes**



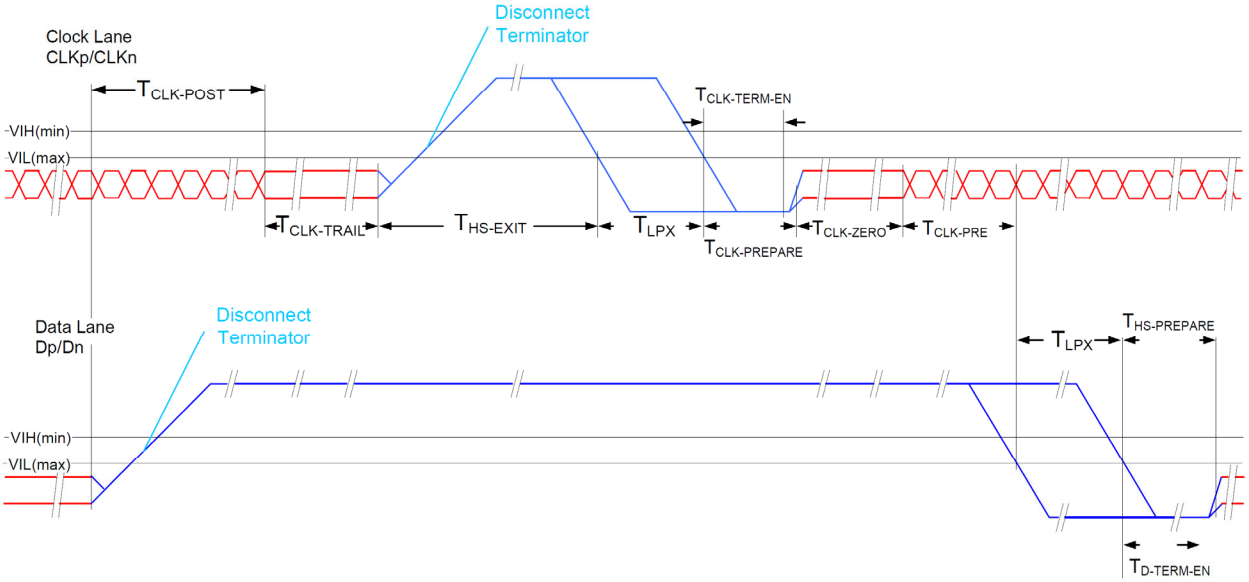

**RGB565 – 4-Lanes**




# 7-4 MIPI-DSI 1 lane Interface Characteristics



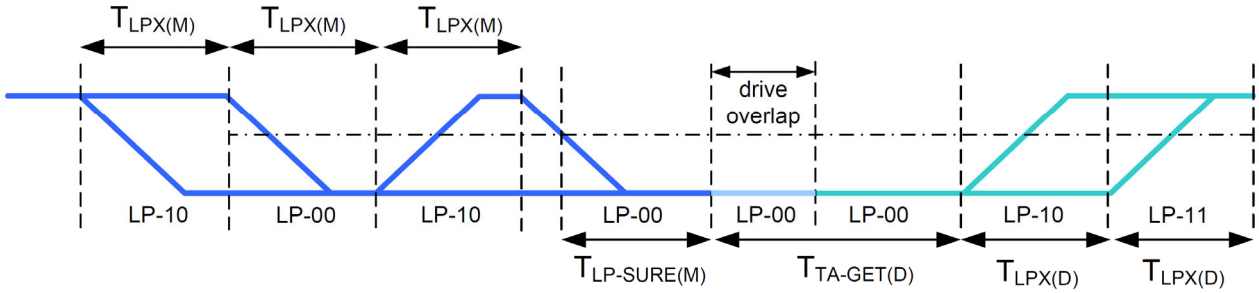
HS clock transmission



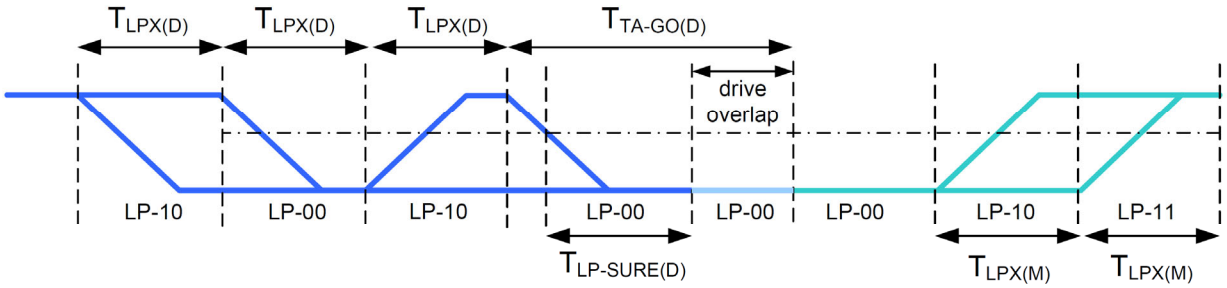

Timing Parameters:

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$ . | 60ns + 52*UI | | | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | **300** | | | ns |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ . | Time for Dn to reach $V_{TERM-EN}$ | | 38 | ns |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ . | Time for Dn to reach $V_{TERM-EN}$ | | 35 ns +4*UI | |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40ns + 4*UI | | 85 ns + 6*UI | ns |
| **$T_{HS-PREPARE}$ + $T_{HS-ZERO}$** | **$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.** | **145ns + 10*UI** | | | **ns** |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | 60ns + 4*UI | | | ns |

Turnaround Procedure




Bus turnaround (BAT) from MPU to display module timing




Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{LPX(M)}$ | Transmitted length of any Low-Power state period of MCU to display module | 50 | | **150** | ns | 1,2 |
| $T_{TA-SURE(M)}$ | Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(M)}$ | | $2*T_{LPX(M)}$ | ns | 2 |
| $T_{LPX(D)}$ | Transmitted length of any Low-Power state period of display module to MCU | 50 | | **150** | ns | 1,2 |
| $T_{TA-GET(D)}$ | Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | | $5*T_{LPX(D)}$ | | ns | 2 |
| $T_{TA-GO(D)}$ | Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | | $4*T_{LPX(D)}$ | | ns | 2 |
| $T_{TA-SURE(D)}$ | Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(D)}$ | | $2*T_{LPX(D)}$ | ns | 2 |

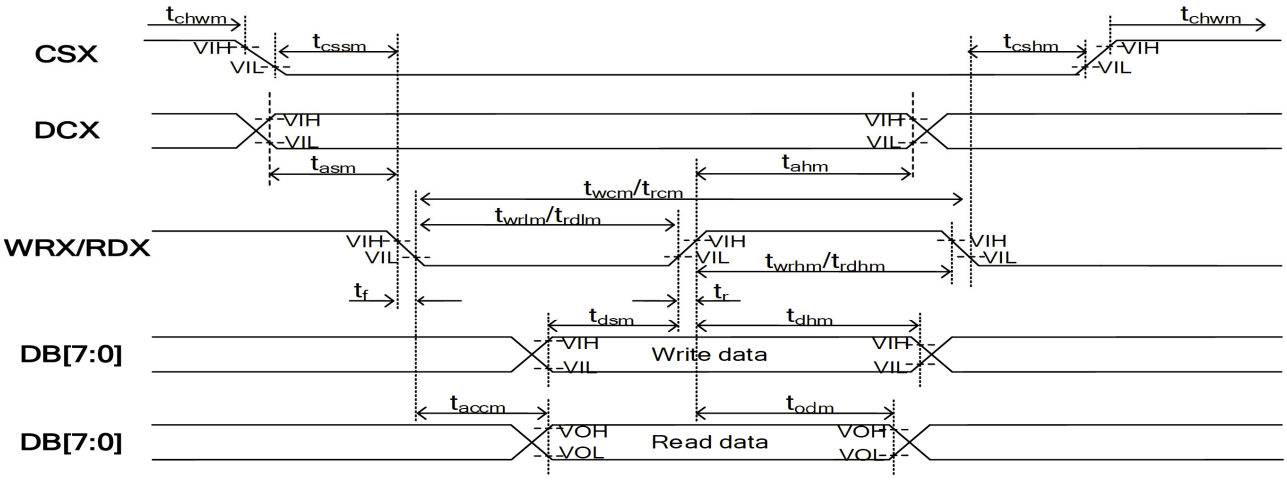
NOTE:

1. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from

the specified values due to asymmetrical rise and fall times.

2. Transmitter-specific parameter

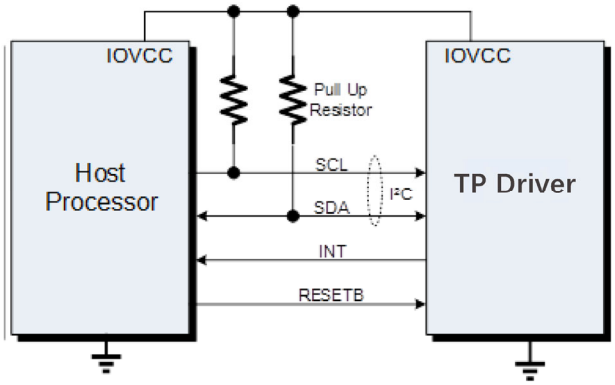
## 7-5 i8080-8Bits Interface Characteristics



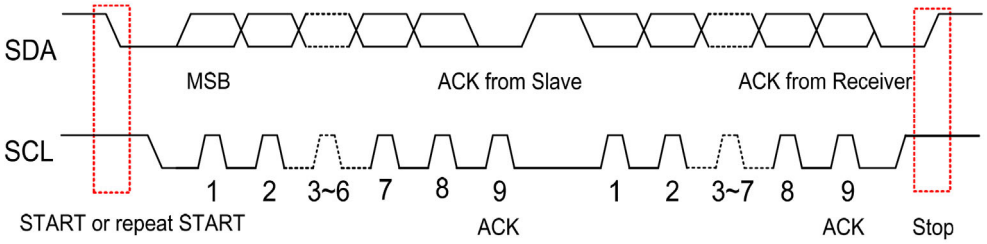

| Characteristic | Symbol | | Specification | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Chip select setup time | CSX | $t_{cssm}$ | 10 | – | ns |
| Chip select hold time | | $t_{cshm}$ | 10 | – | ns |
| Chip select “High” pulse width | | $t_{chwm}$ | 20 | – | ns |
| Address setup time | DCX | $t_{asm}$ | 10 | – | ns |
| Address hold time(Write/Read) | | $t_{ahm}$ | 10 | – | ns |
| Write cycle time | WRX (Write) | $t_{wcm}$ | 20 | – | ns |
| WRX “High” period (Write) | | $t_{wrhm}$ | 10 | – | ns |
| WRX “Low” period (Write) | | $t_{wrlm}$ | 10 | – | ns |
| Read cycle time (Register Read) | RDX (Register Read) | $t_{rcm}$ | 100 | – | ns |
| RDX “High” period (Register Read) | | $t_{rdhm}$ | 50 | – | ns |
| RDX “Low” period (Register Read) | | $t_{rdlm}$ | 50 | – | ns |
| Read cycle time (Memory Read) | RDX (Memory Read) | $t_{rcm}$ | 200 | – | ns |
| RDX “High” period (Memory Read) | | $t_{rdhm}$ | 100 | – | ns |
| RDX “Low” period (Memory Read) | | $t_{rdlm}$ | 100 | – | ns |
| Data setup time | DB[7:0] | $t_{dsm}$ | 10 | – | ns |
| Data hold time | | $t_{dhm}$ | 10 | – | ns |
| Access time | DB[7:0] | $t_{accm}$ | – | 40 | ns |
| Output disable time | | $t_{odm}$ | 20 | – | ns |
| Rise/Fall time | - | $t_r/t_f$ | – | 1 | ns |

# 7-6 Touch Panel(TP) IIC Timing Characteristics

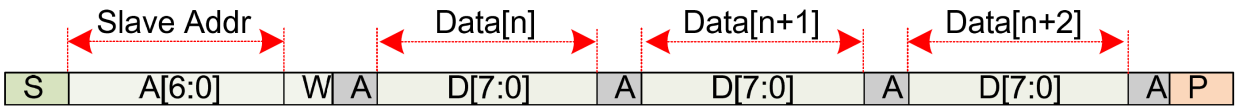
The TP driver communicates to the host through the IIC interface and follows the IIC protocol. IIC bus utilize the SCL and SDA, a two-wire synchronous communication interface and can operate at a maximum bit rate of 400kbps.



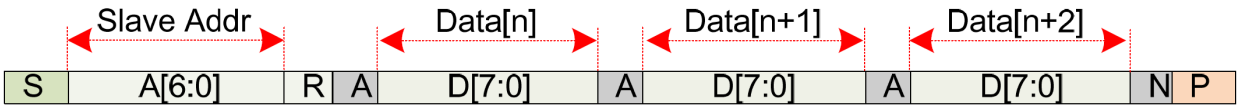

## IIC Serial Data Transfer Format




## IIC Interface Timing




**IIC Master Write, Slave Read**




**IIC Master Read, Slave Write**

**TP Driver IC Slave Addr A[6:0]---0X38**

| Mnemonics | Description |
|---|---|
| S | $I^2C$ Start or $I^2C$ Restart |
| A[6:0] | Slave address |
| R/W | READ/WRITE bit, '1' for read, '0'for write |
| A(N) | ACK(NACK) |
| P | STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet) |

## IIC Timing Characteristics

| Parameter | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| SCL frequency (fast mode support) | 0 | 100 | 0 | 400 | KHz |
| Clock low period | 4.7 | - | 1.3 | - | us |
| Clock high period | 4.0 | - | 0.6 | - | us |
| Bus free time between a STOP and START condition | 4.7 | - | 1.3 | - | us |
| Hold time (repeated) START condition | 4.0 | - | 0.6 | - | us |
| Data setup time | 250 | - | 100 | - | ns |
| Setup time for a repeated START condition | 4.7 | - | 0.6 | - | us |
| Setup Time for STOP condition | 4.0 | - | 0.6 | - | us |

**TP I/O Communication Voltage follow IOVCC**

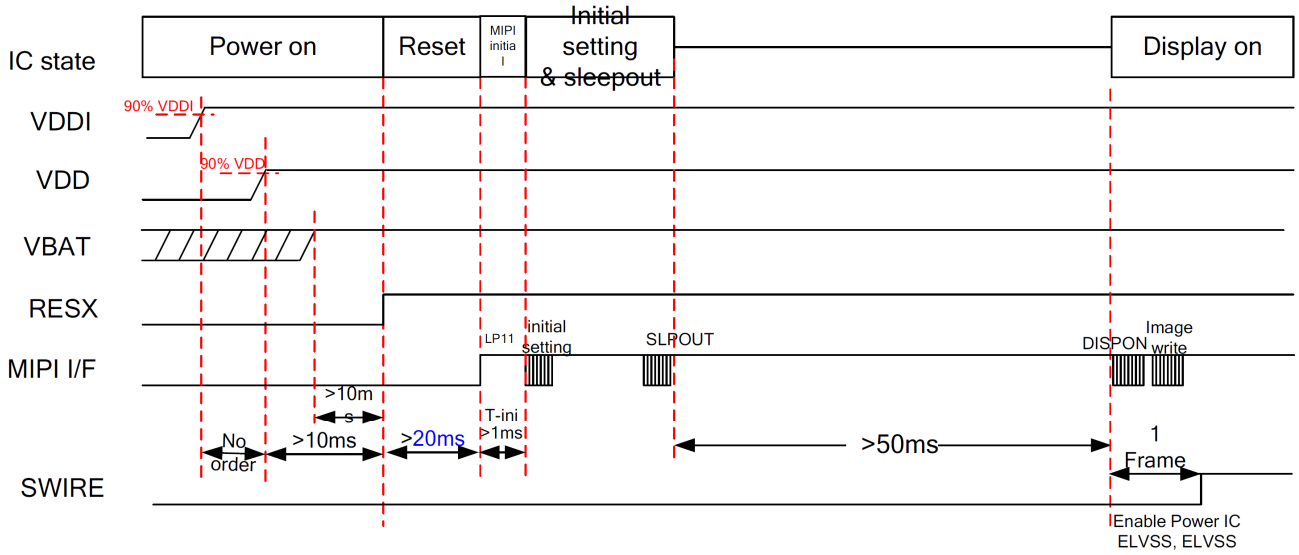
## TP DC Characteristics

| Item | Symbol | Test Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input high-level voltage | VIH | | 0.7 × IOVCC | - | IOVCC | V | |
| Input low -level voltage | VIL | | -0.3 | - | 0.3 × IOVCC | V | |
| Output high -level voltage | VOH | IOH=－0.1mA | 0.7 × IOVCC | - | - | V | |
| Output low -level voltage | VOL | IOH=0.1mA | - | - | 0.3 × IOVCC | V | |
| I/O leakage current | ILI | Vin=0~AVDD | -1 | - | 1 | μA | |
| Current consumption （Normal operation mode） | Iopr | AVDD=2.8V Ta=25℃ MCLK=15MHz | - | 1.5 | - | mA | |
| Current consumption （Monitor mode） | Imon | AVDD=2.8V Ta=25℃ MCLK=15MHz | - | 30 | - | μA | |
| Current consumption （Sleep mode） | Islp | AVDD=2.8V Ta=25℃ | - | 10 | - | μA | |
| Power Supply voltage | AVDD | | 2.8 | - | 3.6 | V | |

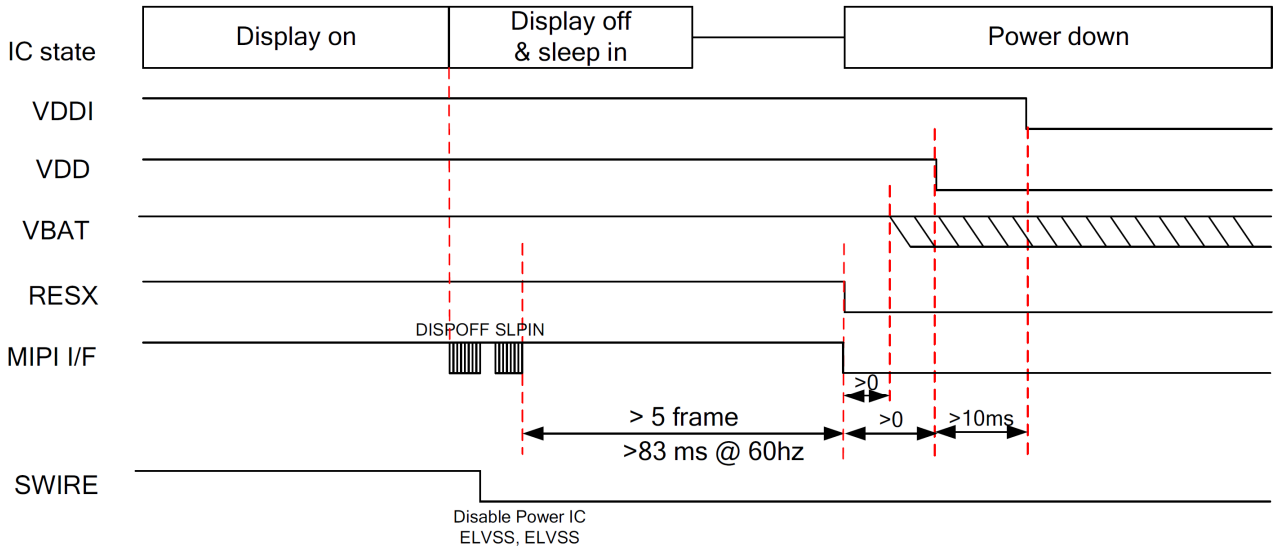
# 8.Recommended Operating Sequence

## 8.1 Power on/off sequence and timing

Power On sequence

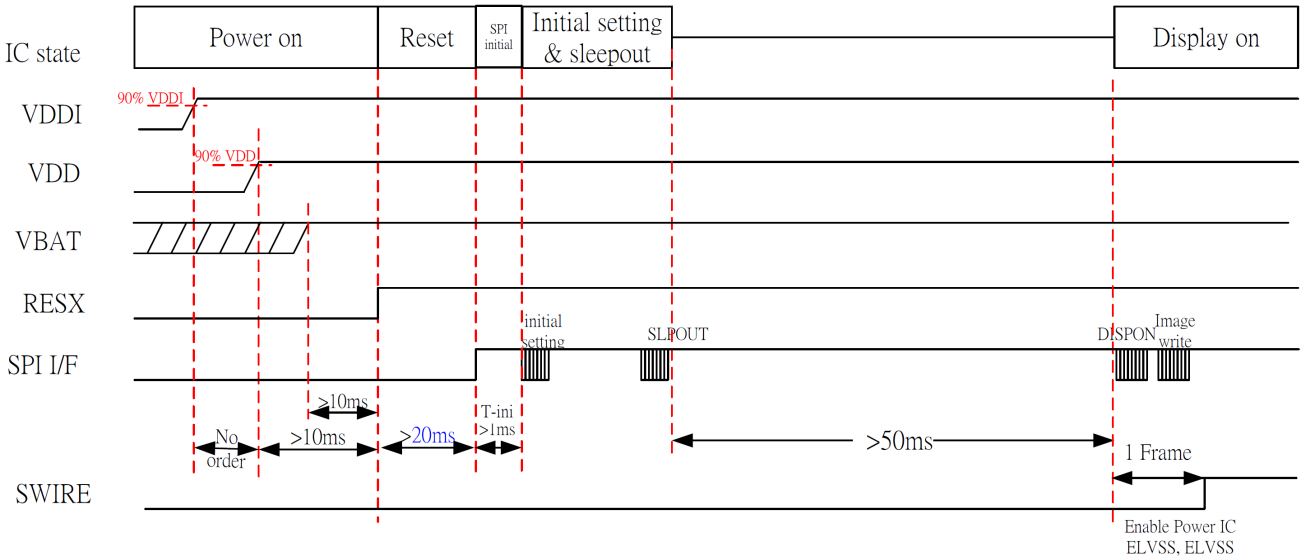



Power Off sequence



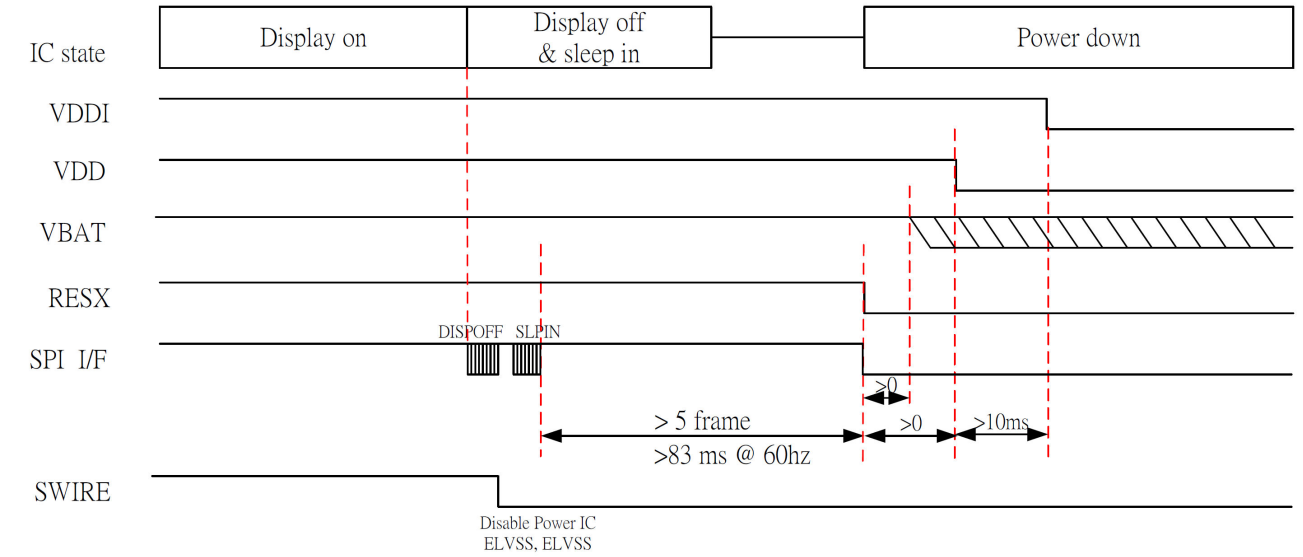
## Power On sequence

SPI Interface




## Power Off sequence

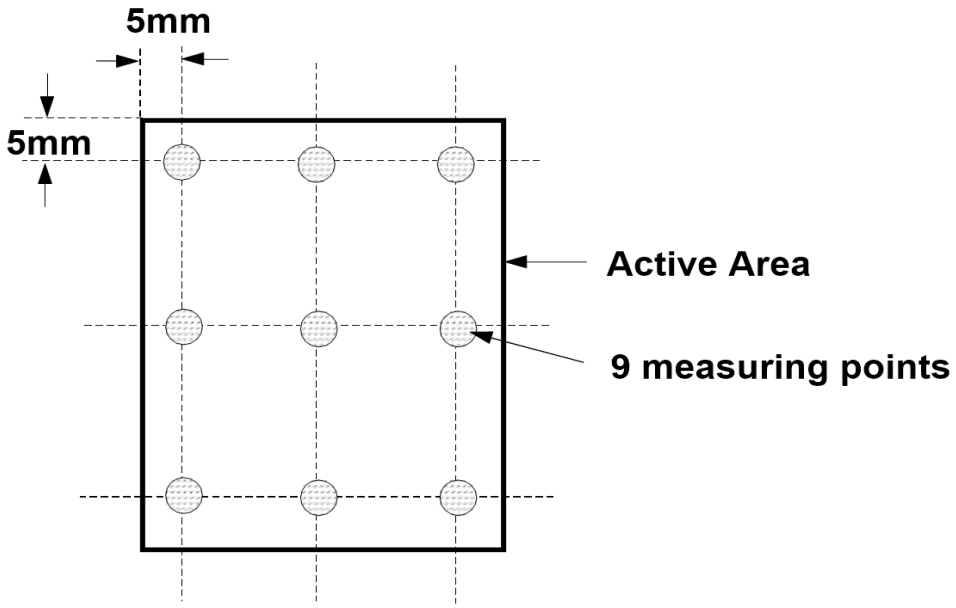
SPI Interface



# 9.Electro-optical characteristics

| Item | | Symbol | Temp | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| Brightness | | | 25℃ | Normal (White Mode) | 500 | 600 | TBD | cd/m² | Center brightness |
| Uniformity | | | 25℃ | Normal (White Mode) | 85 | 90 | - | % | (1) |
| Contrast ratio | | K | 25℃ | Φ=0°,θ=0° | 60,000 | | - | - | (1),(2) |
| Color of CIE coordinate | White | x | 25℃ | Φ=0° θ=0° | 0.275 | 0.295 | 0.315 | - | (1),(2),(3) |
| | | y | | | 0.295 | 0.315 | 0.335 | - | |
| | Red | x | | | 0.630 | 0.660 | 0.690 | - | |
| | | y | | | 0.310 | 0.340 | 0.370 | - | |
| | Green | x | | | 0.170 | 0.220 | 0.270 | - | |
| | | y | | | 0.680 | 0.730 | 0.780 | - | |
| | Blue | x | | | 0.115 | 0.140 | 0.165 | - | |
| | | y | | | 0.025 | 0.050 | 0.075 | - | |
| Color Gamut | | | 25℃ | vs. NTSC | 85 | 100 | - | % | |
| Life Time(5) | | | 25℃ | 50% Brightness drop @250cd/m², Full White | - | 30,000 | - | Hr | (4) |

Note 1): Uniformity Measuring Point

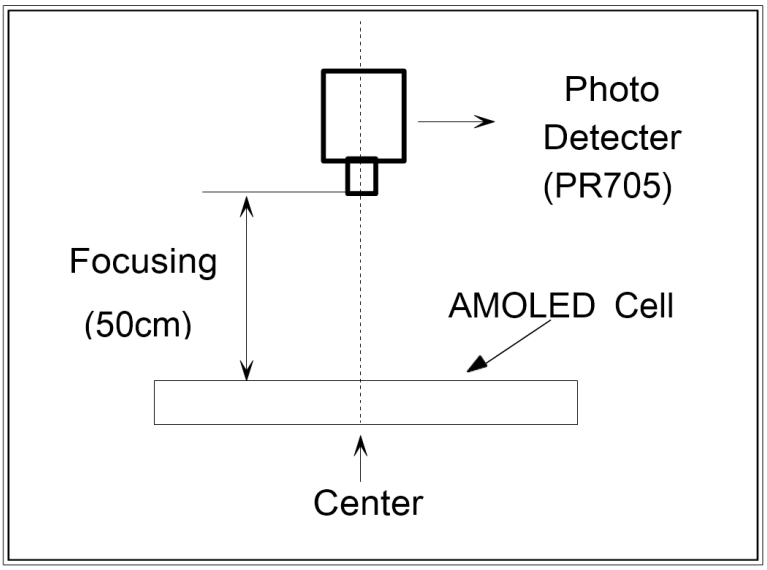



Uniformity = Lmin / Lmax * 100 [%]

Note 2): Definition of contrast ratio (K)

$$\text{Contrast Ratio(K)} = \frac{\text{Brightness of selected dot (White patterned area) at 250cd/m}^2}{\text{Brightness of non-selected dot (Black patterned area) at 250cd/m}^2}$$

Note 3): Optical measuring system： temperature regulated chamber




Note 4): Life Time

The elapsed time that the full white brightness decreases to the half of initial value

# 10. Standard Specification For Reliability

| No | Item | Condition | Cycles | Judgment Criterion |
|---|---|---|---|---|
| 1 | High Temperature Operation | 80℃/ 240hours | 10 | 1. No clearly visible defects or remarkable deterioration of display quality.However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted.<br>2. No function-related abnormalities. |
| 2 | Low Temperature Operation | -30℃/ 240hours | 10 | |
| 3 | High Temperature Storage | 85℃/ 240hours | 5 | |
| 4 | Low Temperature Storage | -40℃/ 240hours | 5 | |
| 5 | High Temperature Humidity Operation | 60℃/90%RH/ 240hours | 5 | |
| 6 | Thermal Shock | -40℃~85℃ / 100cycles | 5 | |

Note: The results must be measured after 2 hours later under room temperature keeping.

**- END -**