



#### P-CHANNEL ENHANCEMENT MODE MOSFET

### **Product Summary**

V <sub>(BR)DSS</sub>	R <sub>DS(on)max</sub>	I <sub>D</sub> T <sub>A</sub> = +25°C
-30V	14.5mΩ @ $V_{GS}$ = -10 $V$	-10.2A
-307	$25.5 \text{m}\Omega$ @ $V_{GS} = -4.5 \text{V}$	-7.7A

## **Description**

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## **Applications**

- Load Switch
- Power Management Functions
- DC-DC Converters

## **Features and Benefits**

- Low On-Resistance
- Low Input Capacitance
- Low Input/Output Leakage
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

#### **Mechanical Data**

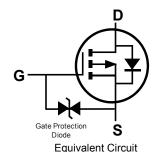
- Case: U-DFN2523-6
- Case Material: Molded Plastic, "Green" Molding Compound.
  UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe.
  Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.008 grams (Approximate)



Pin 1, 2 = Source Pin 3 = Gate Pin 4, 5, 6 = Drain







### **Ordering Information** (Note 4)

Part Number	Case	Packaging
DMP3018SFK-7	U-DFN2523-6	3,000/Tape & Reel
DMP3018SFK-13	U-DFN2523-6	10,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

## **Marking Information**

U-DFN2523-6





P7 = Product Type Marking Code 7P = Product Type Marking Code YM = Date Code Marking Y = Year (ex: B = 2014) M = Month (ex: 9 = September)

Date Code Kev

Date Code Rey												
Year	201	4	2015		2016	20	17	2018		2019	2	2020
Code	В		С		D	E	=	F		G		Н
M 41-		F. I.	NA				1	A	-	0-4	NI	
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



# **Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units		
Drain-Source Voltage	V <sub>DSS</sub>	-30	V		
Gate-Source Voltage	V <sub>GSS</sub>	±25	V		
Continuous Drain Current (Note 6) $V_{GS} = -10V$ Steady $T_A = +25^{\circ}C$ State $T_A = +70^{\circ}C$			I <sub>D</sub>	-10.2 -8.1	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	I <sub>D</sub>	-7.7 -6.1	А		
Maximum Continuous Body Diode Forward Current (N	I <sub>S</sub>	-3	Α		
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I <sub>DM</sub>	-80	Α		
Avalanche Current (Note 7)	I <sub>AS</sub>	-14	Α		
Avalanche Energy (Note 7)	E <sub>AS</sub>	104	mJ		

# Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)		$P_{D}$	1	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	123	°C/W
Total Power Dissipation (Note 6)		P <sub>D</sub>	2.2	W
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	55	°C/W
Total Power Dissipation (Note 6)	T <sub>C</sub> = +25°C	P <sub>D</sub>	17	W
Thermal Resistance, Junction to Case (Note 6)		$R_{ heta JC}$	7.2	°C/W
Operating and Storage Temperature Range		T <sub>J,</sub> T <sub>STG</sub>	-55 to +150	°C

## Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

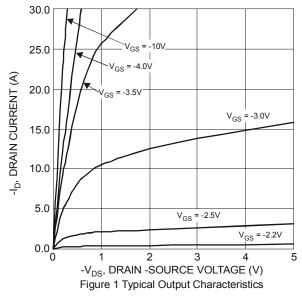
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage		-30	_	_	V	$V_{GS} = 0V$ , $I_D = -10mA$	
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	1	_	_	-1	μA	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V	
Zero Gate Voltage Drain Current T <sub>J</sub> = +150°C (Note 9)	I <sub>DSS</sub>	_	_	-100	μΑ	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±10	μA	$V_{GS} = \pm 25V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1	-1.6	-3	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
Static Drain-Source On-Resistance	D	_	9.5	14.5	mΩ	$V_{GS} = -10V, I_D = -9.5A$	
Static Dialii-Source Off-Resistance	R <sub>DS(ON)</sub>	_	15	25.5	11122	$V_{GS} = -4.5V$ , $I_{D} = -6.9A$	
Diode Forward Voltage	$V_{SD}$	_	-0.7	-1.2	V	$V_{GS} = 0V, I_{S} = -1A$	
On State Drain Current (Note 9)	I <sub>D(ON)</sub>	-20	_	_	Α	V <sub>DS</sub> ≤5V, V <sub>GS</sub> = -10V	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	C <sub>iss</sub>	_	2,207	4,414	pF	45)()(	
Output Capacitance	Coss	_	390	780		$V_{DS} = -15V, V_{GS} = 0V,$ f = 1MHz	
Reverse Transfer Capacitance	$C_{rss}$	_	343	686		- IIVIHZ	
Gate Resistance	Rg	_	8.4	20	Ω	$V_{DS}$ = 0V, $V_{GS}$ = 0V, f = 1MHz	
Total Gate Charge (V <sub>GS</sub> = -10V)	Qg	_	42.7	90			
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Qg	_	21.6	45	nC	V <sub>DS</sub> = -15V. In = -9.5A	
Gate-Source Charge	Qgs	_	7.9	16	IIC	$V_{DS} = -15V, I_{D} = -9.5A$	
Gate-Drain Charge	Q <sub>gd</sub>	_	10	20			
Turn-On Delay Time		_	7.35	15			
Turn-On Rise Time	t <sub>r</sub>	_	16.4	30		$V_{DD} = -15V$ , $V_{GS} = -10V$ ,	
Turn-Off Delay Time	t <sub>D(off)</sub>	_	67.2	110	ns	$R_{GEN} = 6\Omega$ , $I_D = -9.5A$	
Turn-Off Fall Time	t <sub>f</sub>	_	37.5	60			
Reverse Recovery Time	t <sub>rr</sub>	_	18.6	35	ns	1 0.54 45/44 4004/	
Reverse Recovery Charge	Qrr		8.6	17.5	nC	$I_S = -9.5A$ , di/dt = 100A/ $\mu$ s	

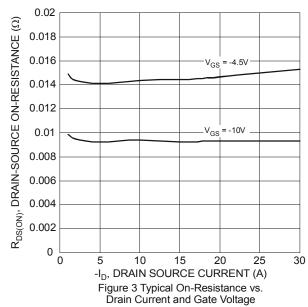
Notes:

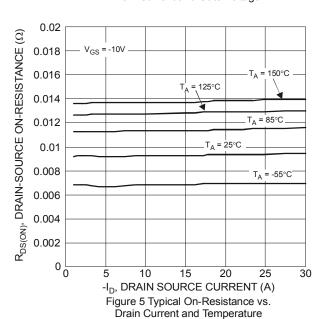
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
  UIS in production with L = 1mH, T<sub>J</sub> = +25°C.
  Short duration pulse test used to minimize self-heating effect.
  Guaranteed by design. Not subject to production testing.

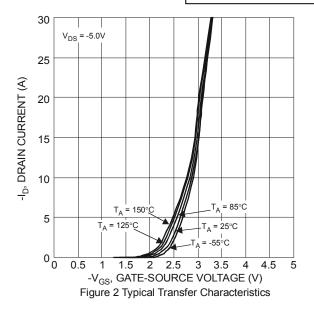


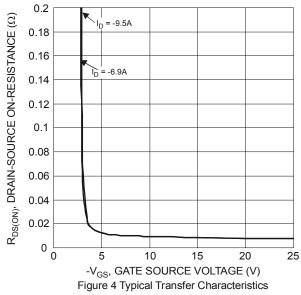












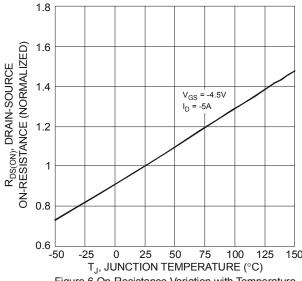
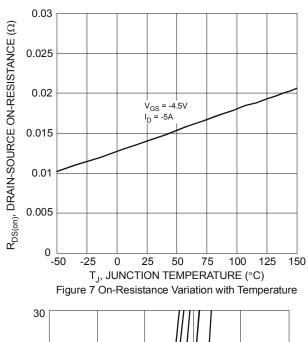
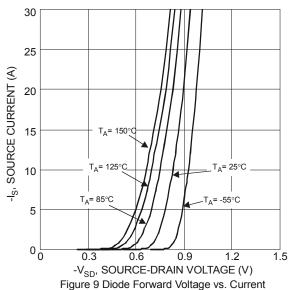
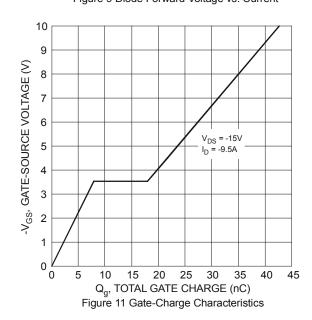


Figure 6 On-Resistance Variation with Temperature









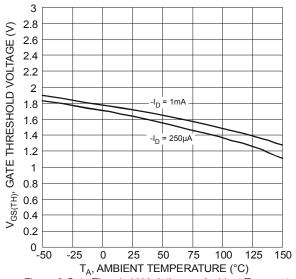
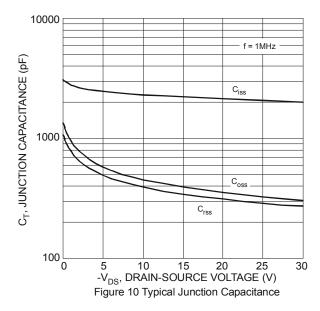
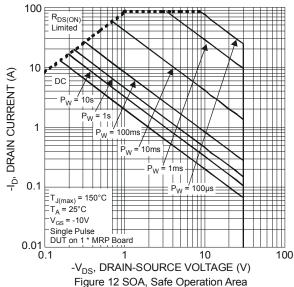
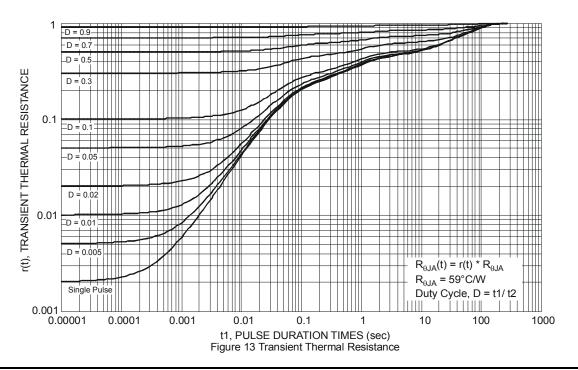


Figure 8 Gate Threshold Variation vs. Ambient Temperature



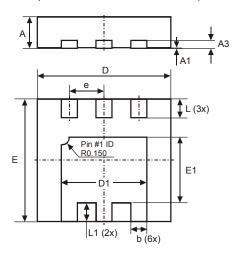






## **Package Outline Dimensions**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

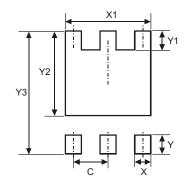


U-DFN2523-6							
Dim	Min	Max	Тур				
Α	0.57	0.63	0.60				
A1	0	0.05	0.02				
А3	_	0.15					
b	0.25	0.35	0.30				
D	2.45	2.55	2.50				
D1	1.55	1.65	1.60				
е	_	_	0.65				
Е	<b>E</b> 2.25 2.35 2.30						
E1	1.18	1.28	1.23				
L	0.30	0.40	0.35				
L1	0.30	0.40	0.35				
All D	All Dimensions in mm						

## **Suggested Pad Layout**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

#### U-DFN2523-6



Dimensions	Value (in mm)
С	0.650
Х	0.400
X1	1.700
Υ	0.650
Y1	0.450
Y2	1.830
Y3	2.700



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